

MAMBO

**Monolithic Active Pixel Matrix
with Binary cOunters**

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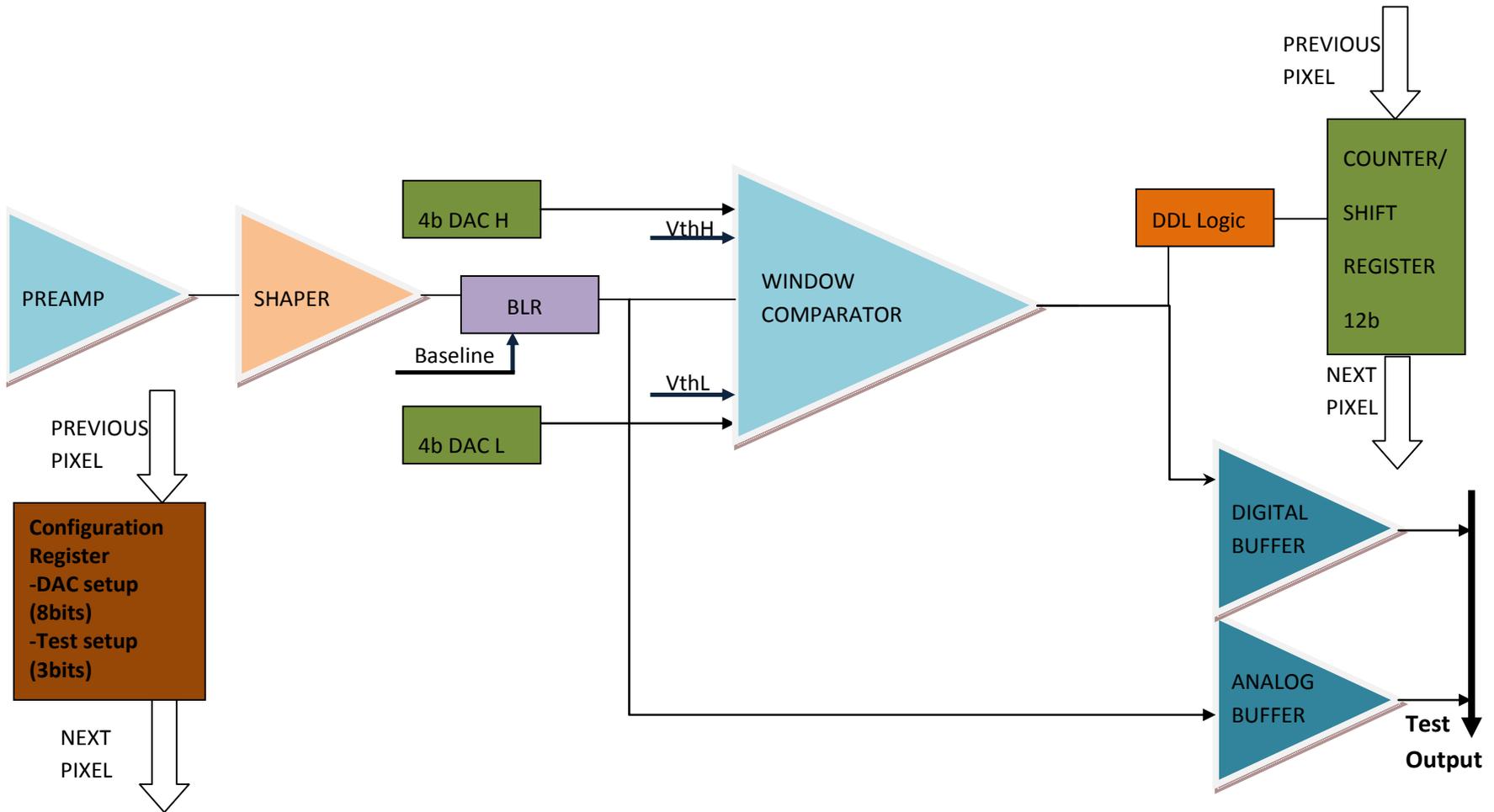
Fermi National Accelerator Laboratory

Presentation Outline

- MAMBO Electronics
 - Pixel design and layout
- MAMBO III development
 - T-Micro 3D Integration
- MAMBO IV development
 - Nested wells structure
- Conclusions

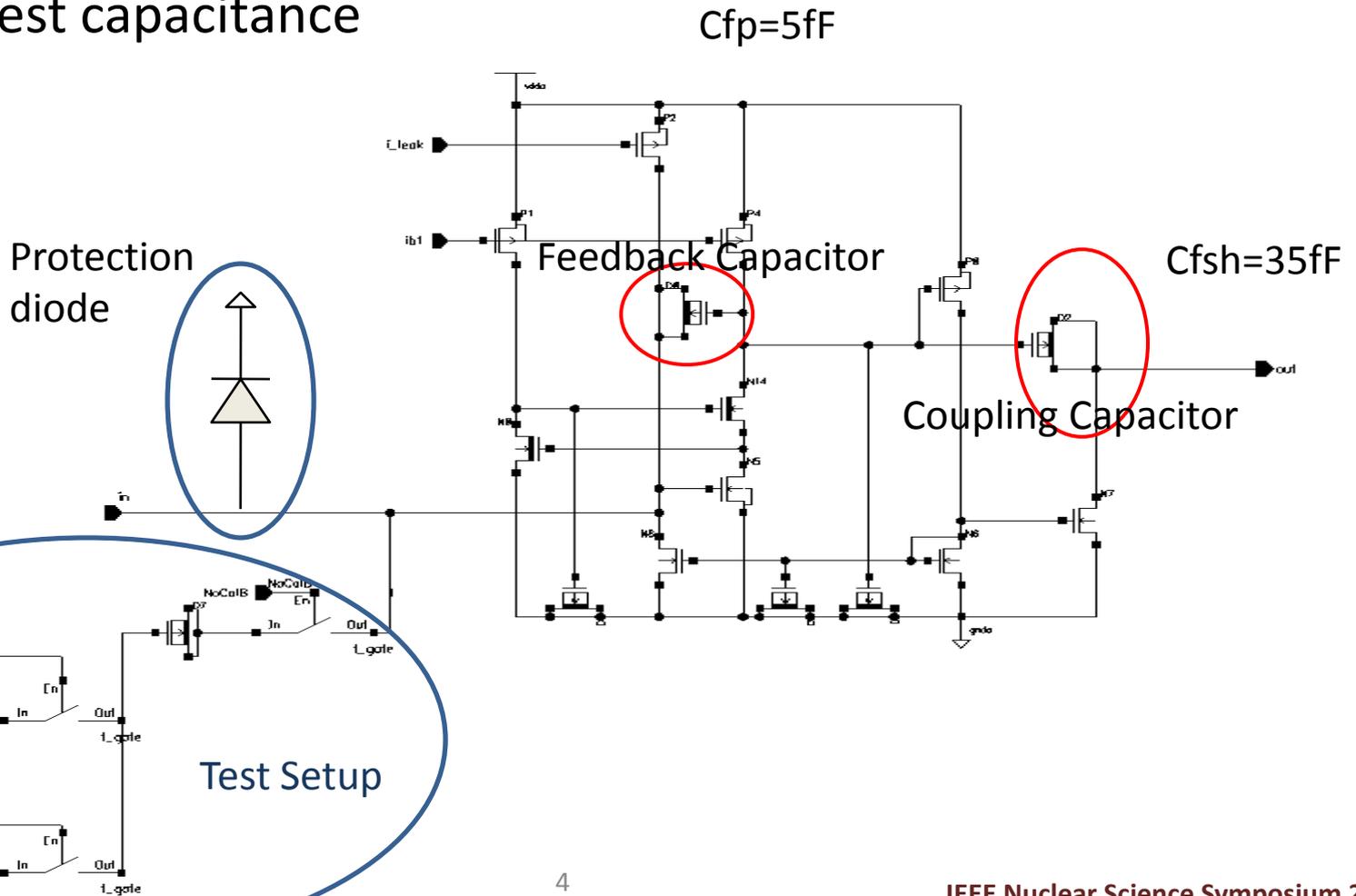
MAMBO Pixel Electronics

PIXEL Design



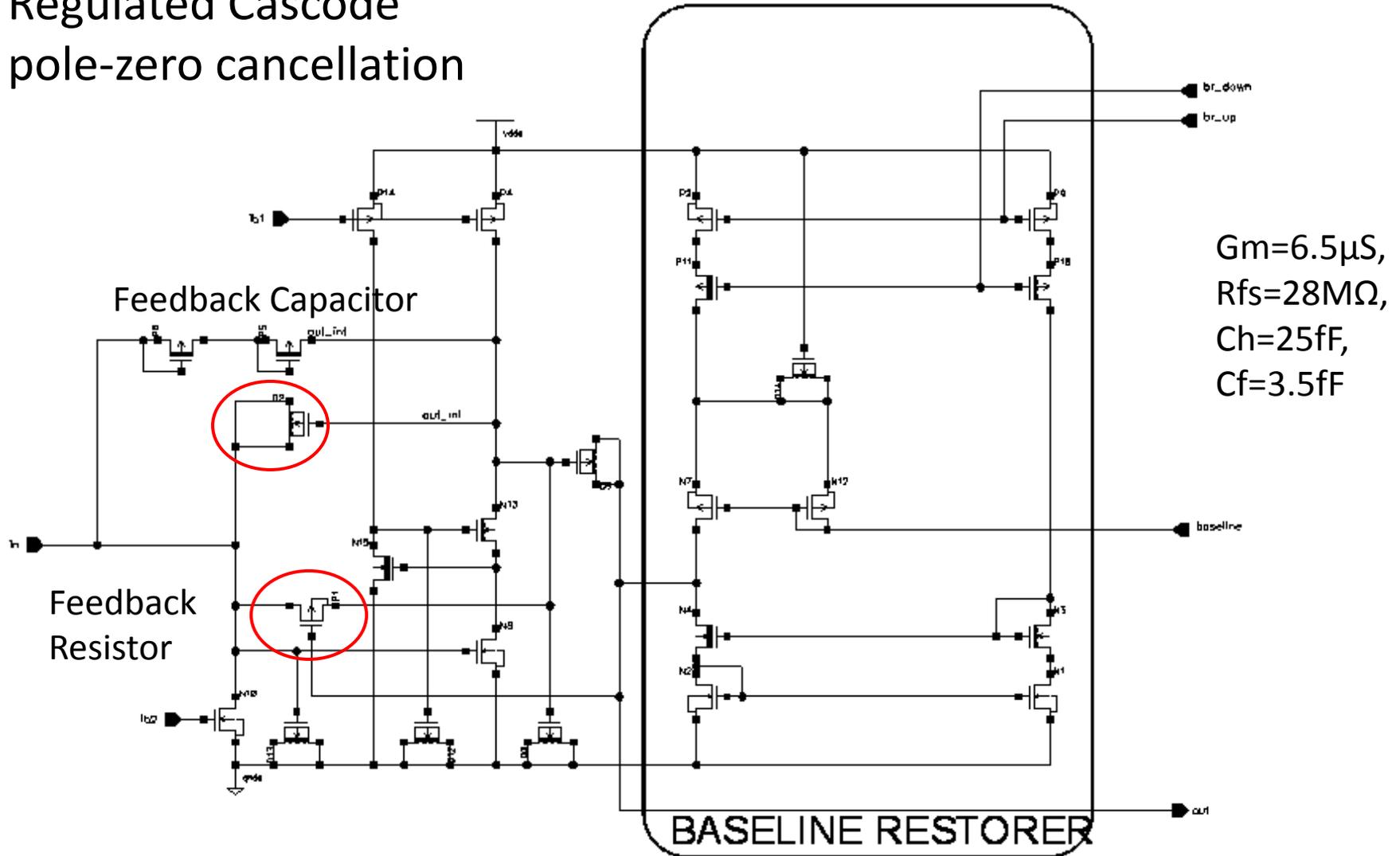
Preamplifier

- Regulated Cascode
- Leakage current compensation
- 1.7fF I/P test capacitance



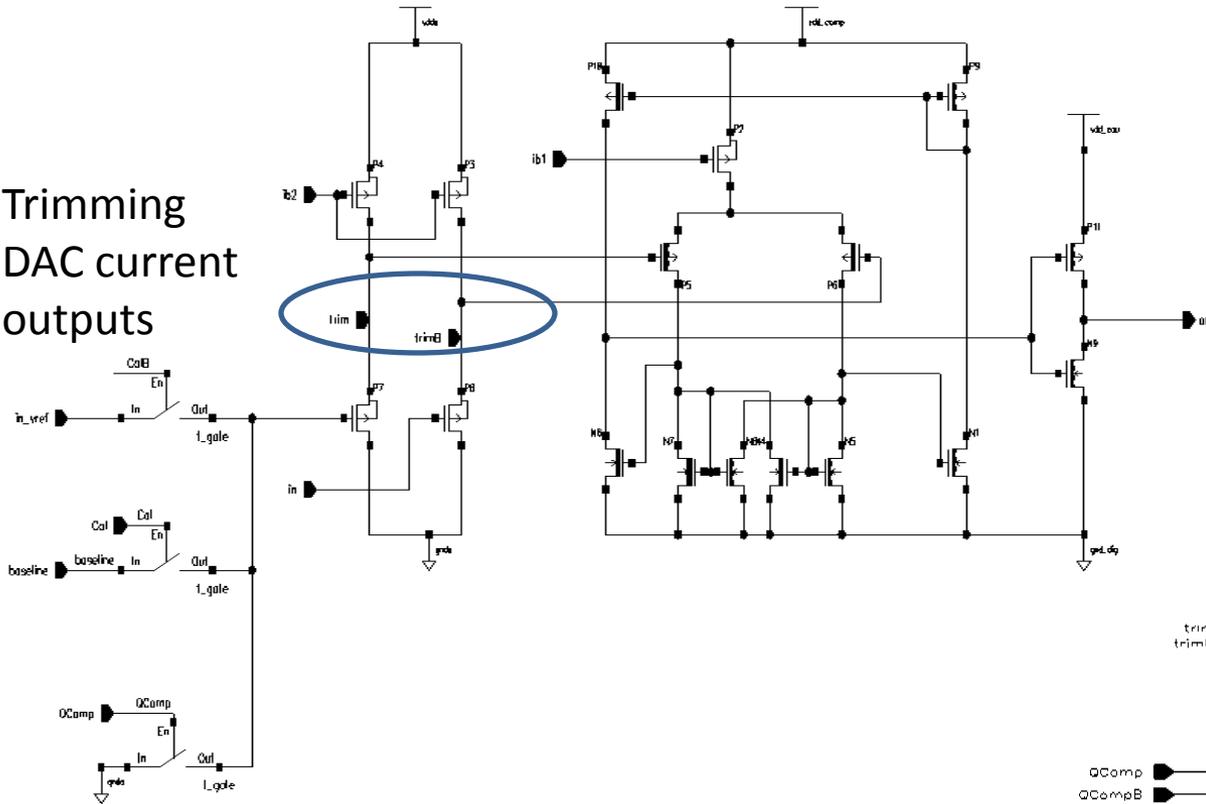
Shaper and Baseline Restorer

- Regulated Cascode
- pole-zero cancellation

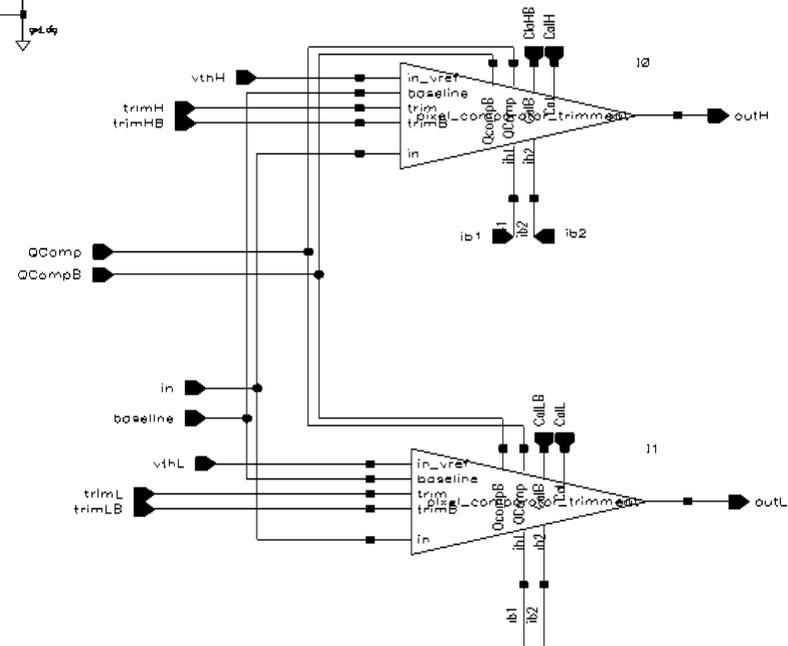


Window comparator

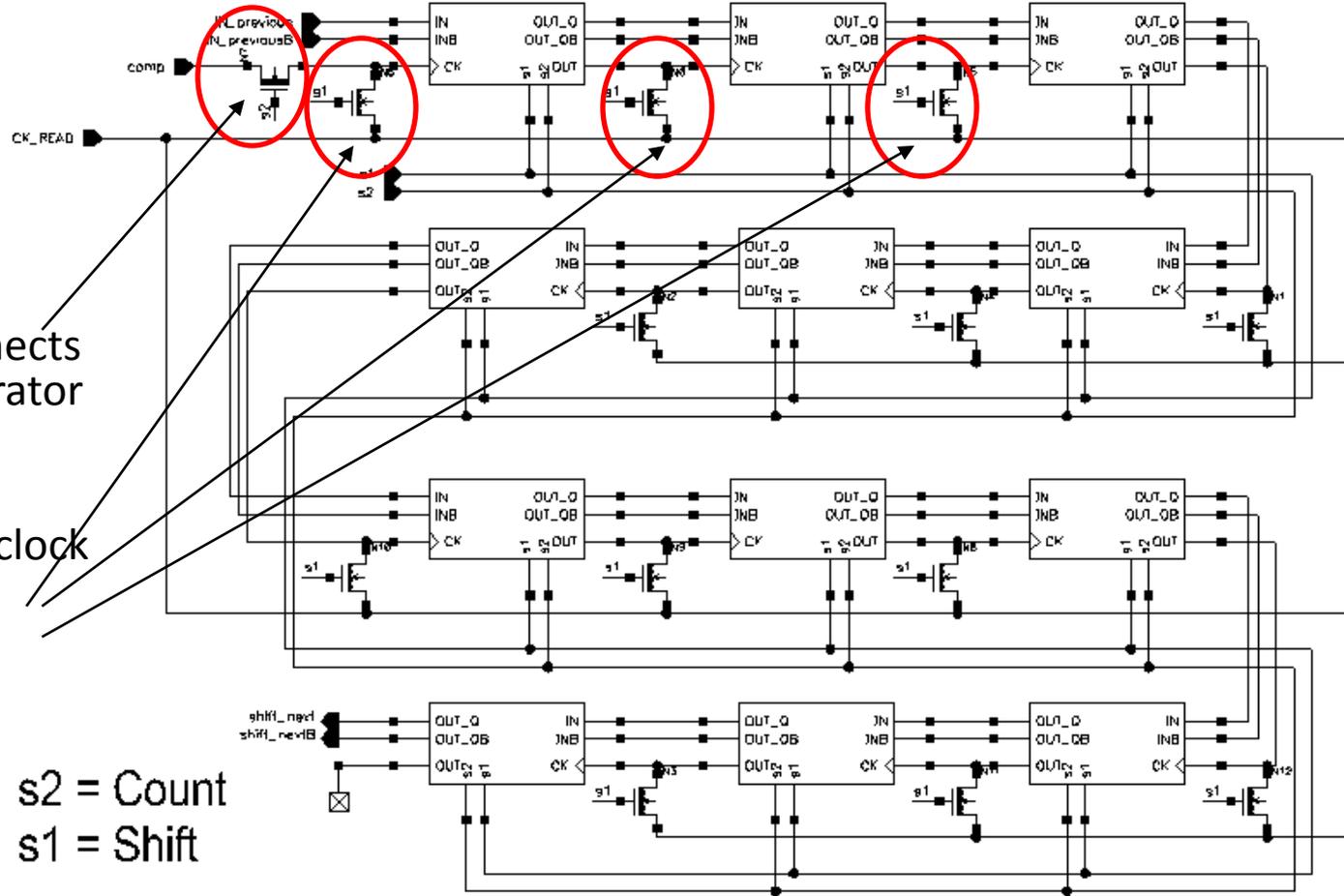
Trimming
DAC current
outputs



- Hysteresis Comparator
- Connected to in_vref during normal operation
- OR
- Connected to baseline for trimming
- OR
- Connected to gnd! when disabled



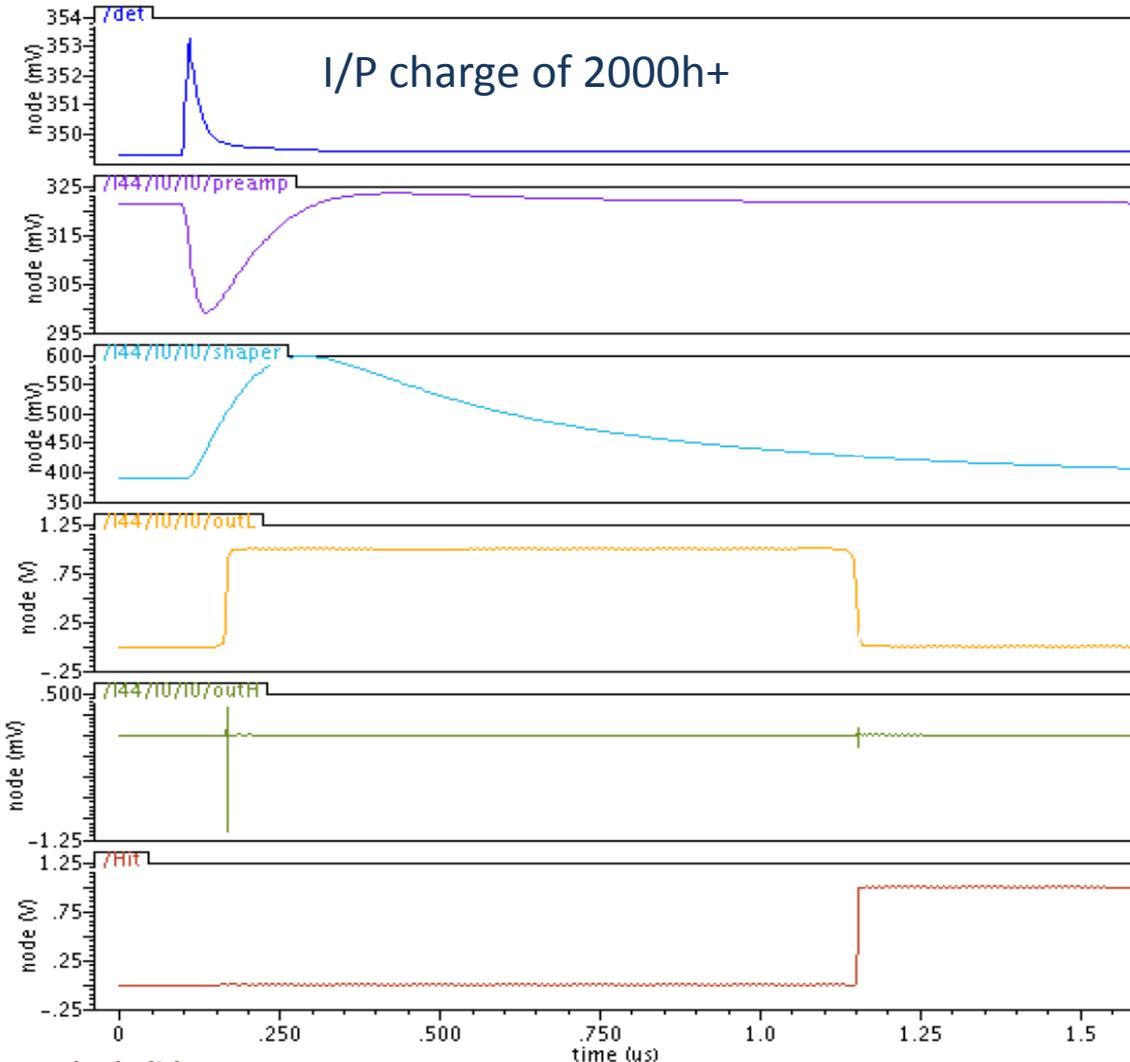
Counter /Shift Register



- 12 bit ripple counter
- Count switch disconnects counter from comparator while shifting
- CK_READ is external clock used for shifting data
- Shift switch applied shifting clock

Simulation result

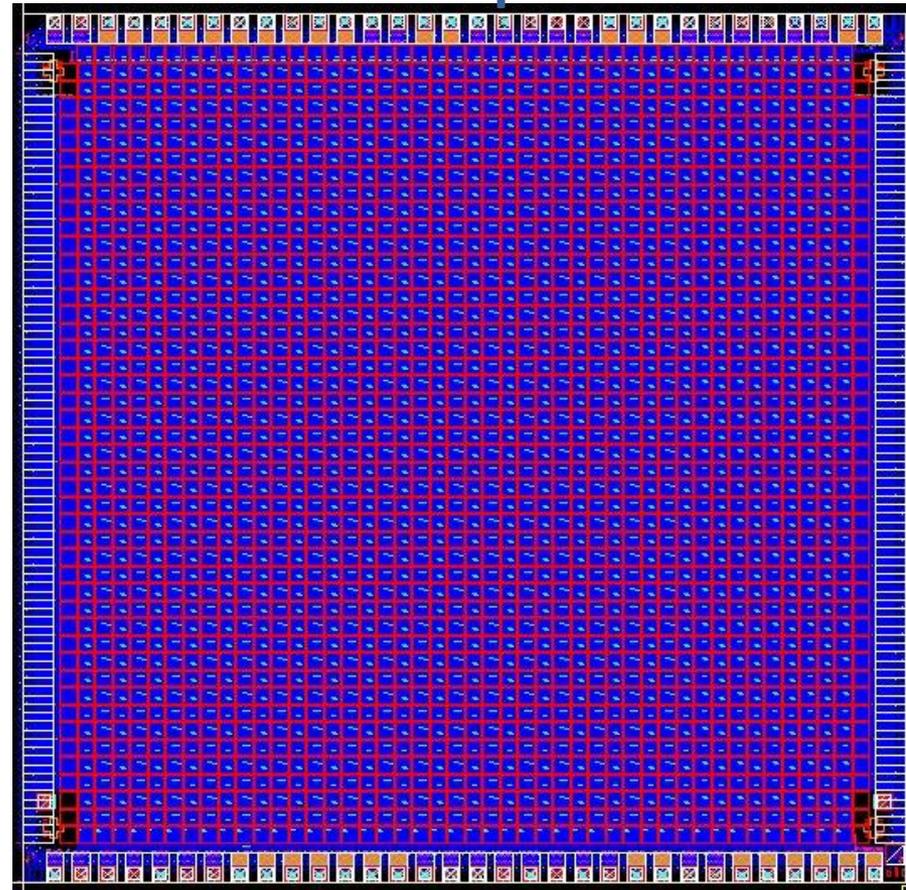
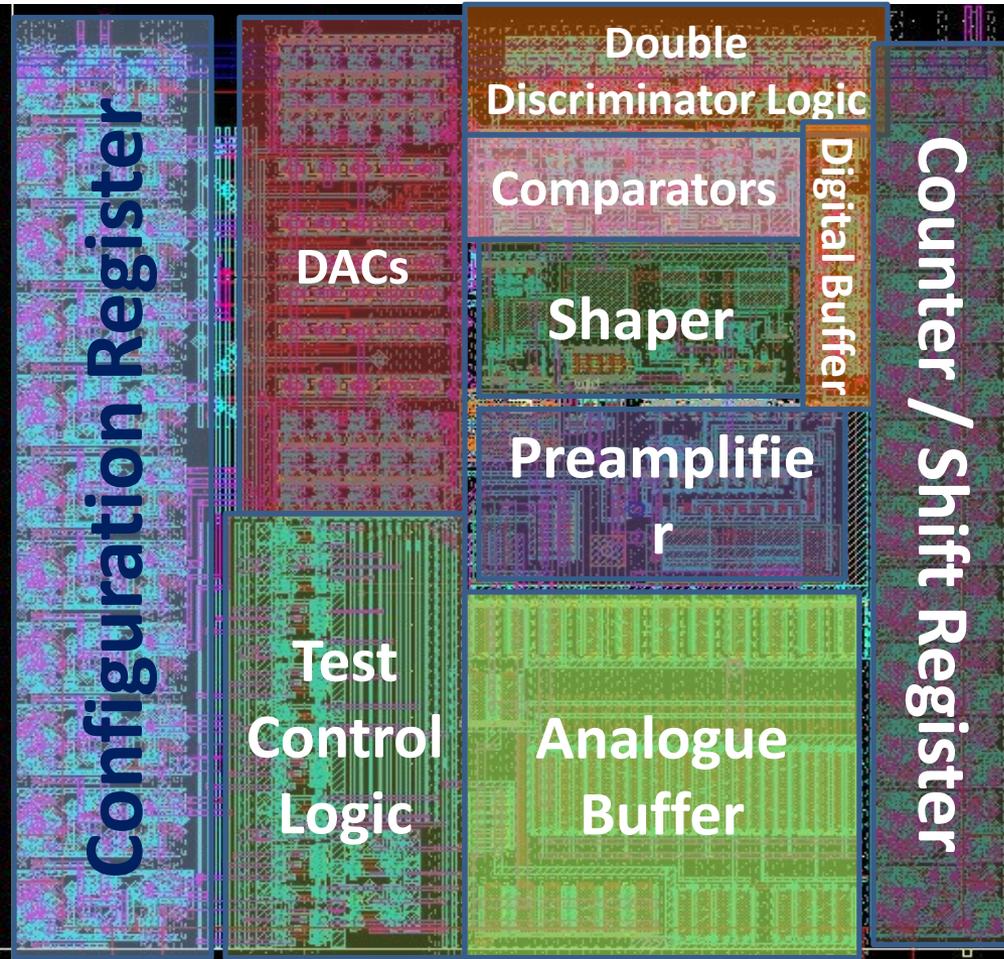
Transient Response



Input Range	From 500h+ to 4,000h+ for positive polarity
Sensitivity	100mV/1000h+
Shaping Time	200ns
Leakage current	Up to 200pA
Noise	~ 80 e-
Power dissipation per pixel	2.7μW

Pixel Layout

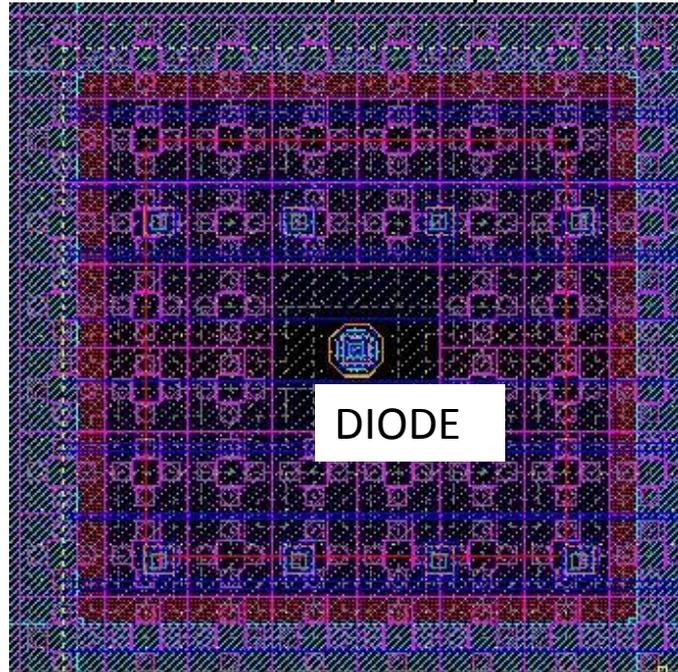
- Transistor count ~ 950



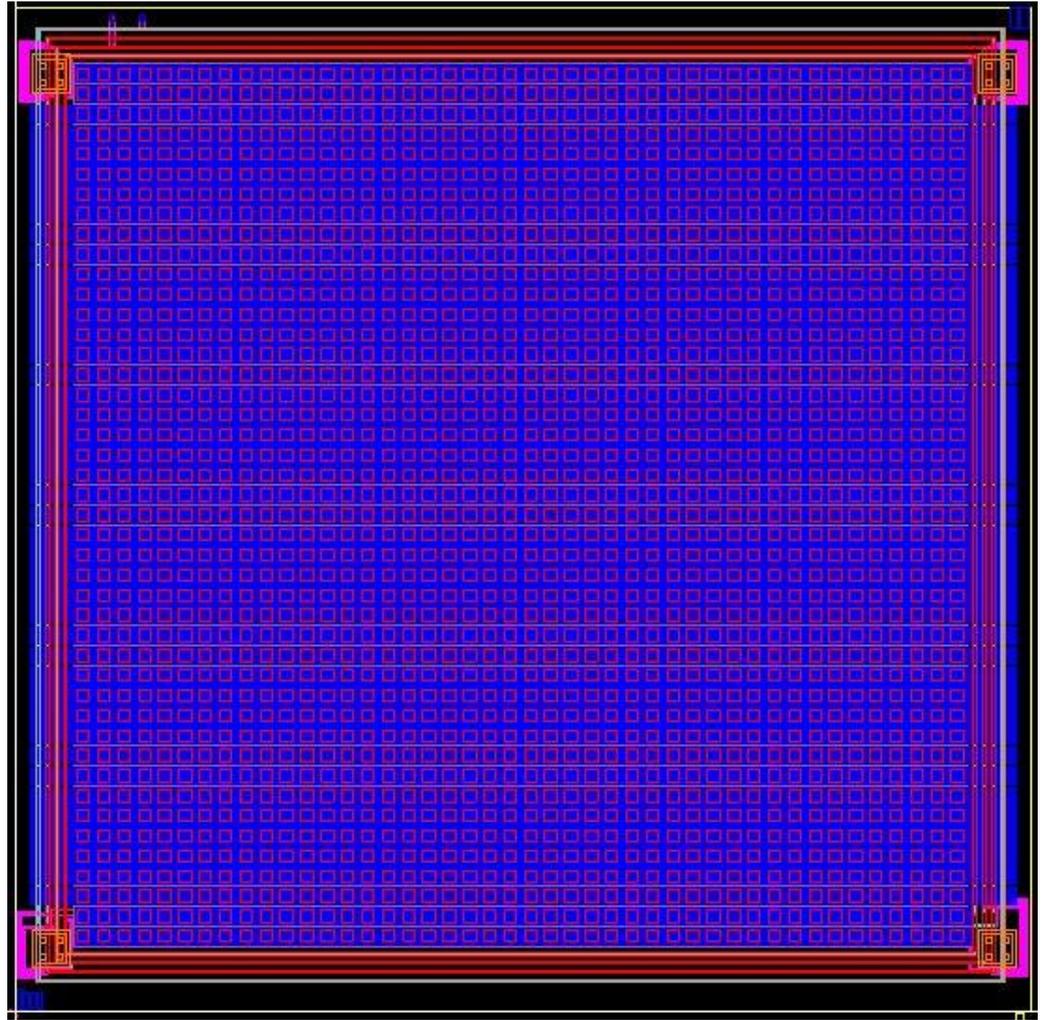
- 5mm x 5mm
- 1936 pixel matrix (44 x44)
- Each column has additional buffering of analog and digital signals
- Pads with back metal opening
- Alignment markers on all 4 corners

Diode Pixel

100 μ x 100 μ

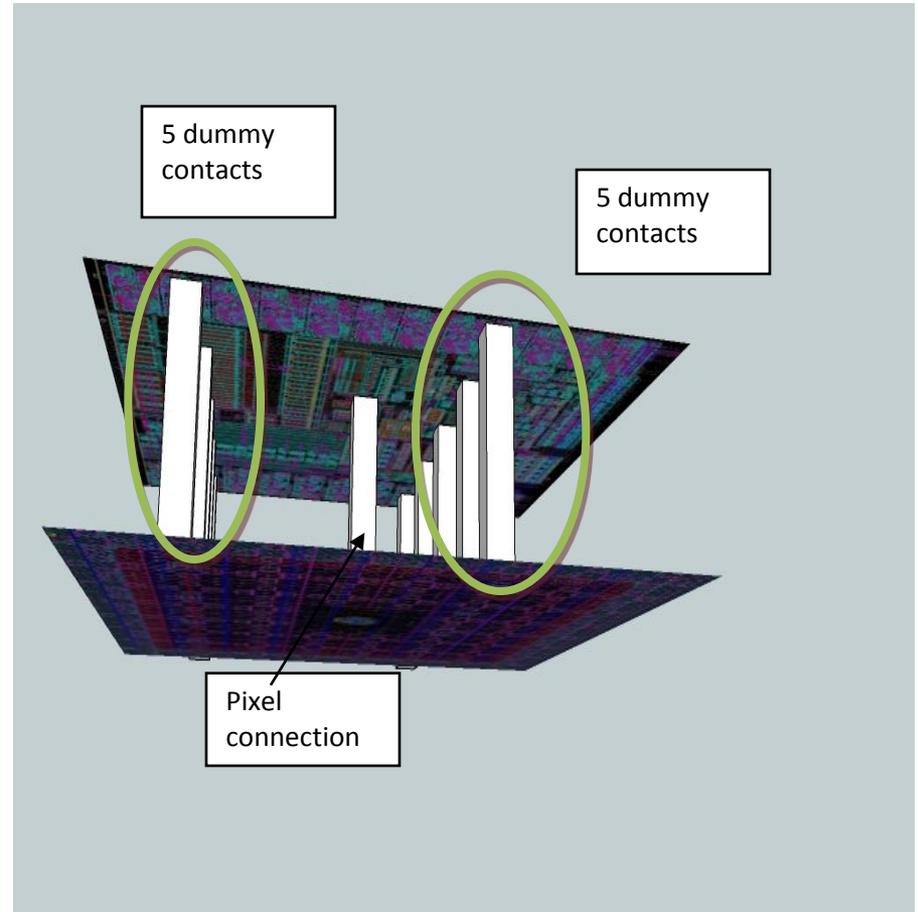
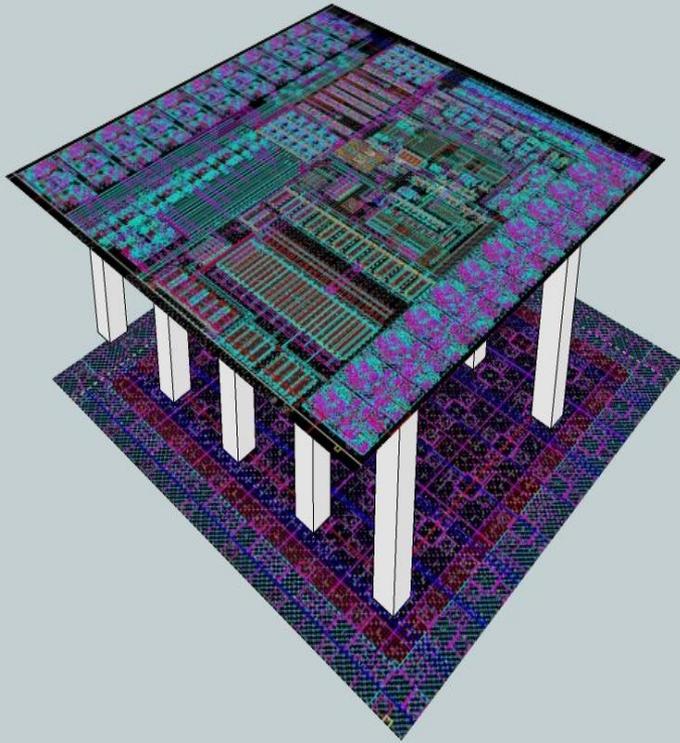


MAMBO bottom ASIC



- 5mm x 5mm
- 1936 pixel matrix (44 x44)
- 4 guard rings around the matrix
- No bond Pads contains only micro bump pads, aligned with the top chip.
- Alignment markers on all 4 corners

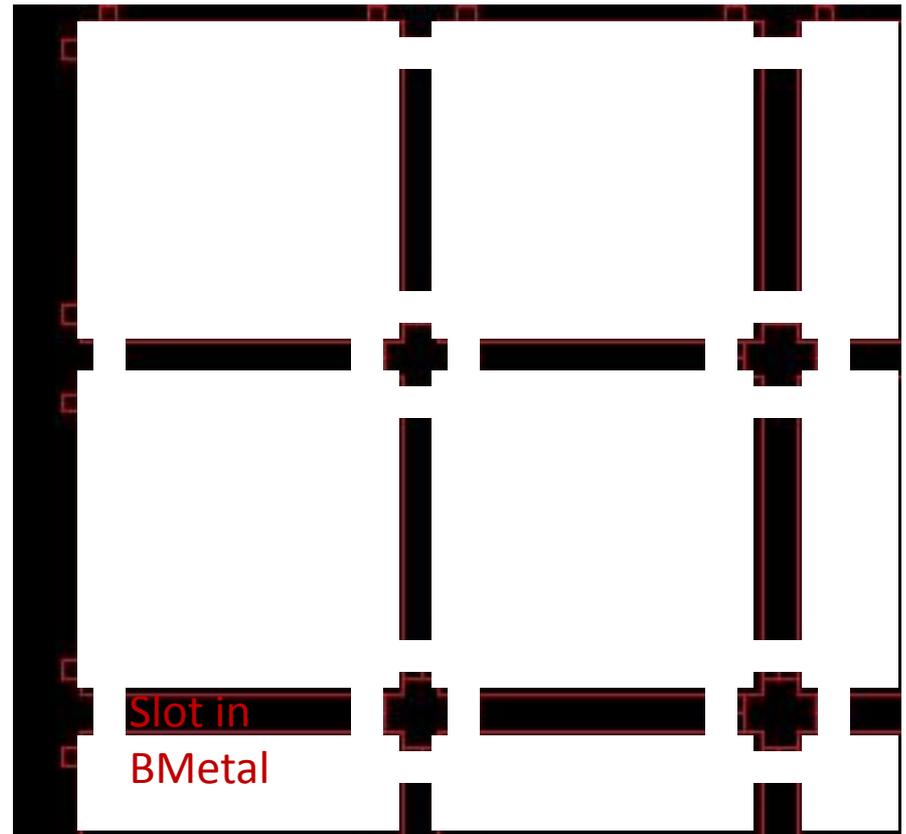
3D Model



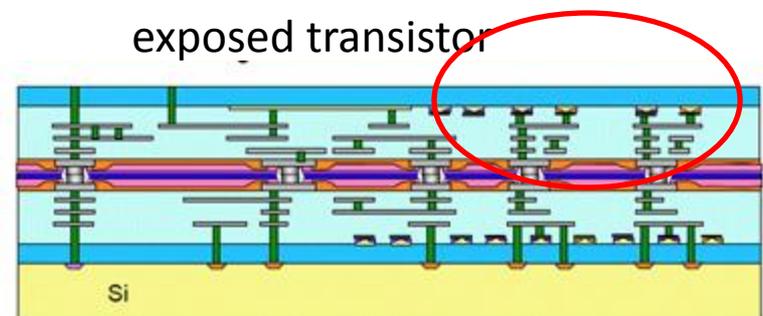
There is a single 3D bump contact to the diode and 10 additional dummy contacts to give us a contact density of 0.4% per pixel.

Protection

- After handle wafer is removed the bodies of transistors and sensitive nodes are exposed to electrical coupling from external environment
- Backplane connected to Analogue Ground per pixel
- Peripheral digital logic connected to Digital ground plane



Shielding per pixel using back metal

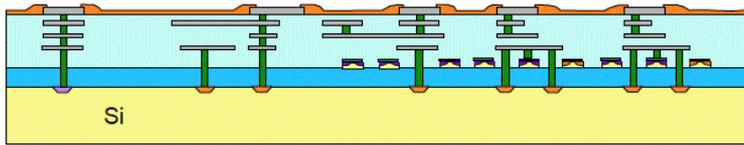


MAMBO III

T-Micro 3D Integration process

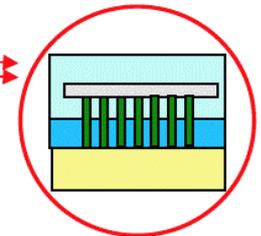
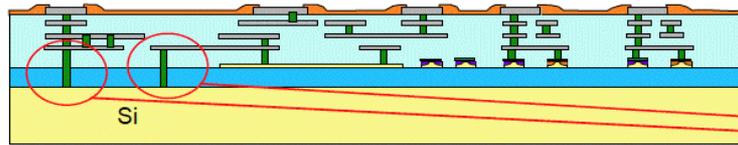
(1) Stack Process Flow (after finishing wafer process)

Lower Chip



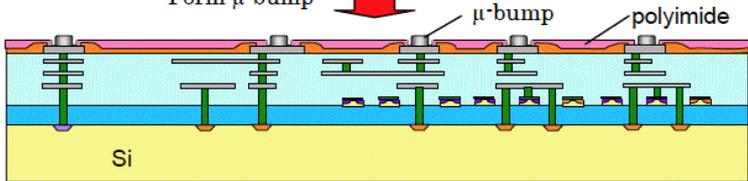
Upper Chip

(Layout must be done with mirror inverted)

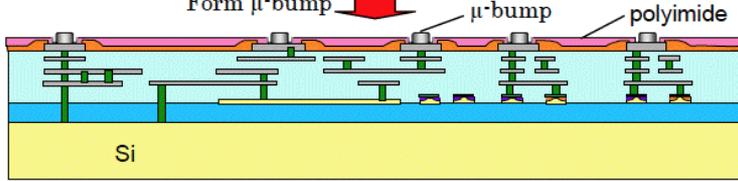


Use multi via structure for contact path between 1metam and bond pad dia./space 0.32/0.6 μ m
In left figure, single via is used for simplifying the cross section

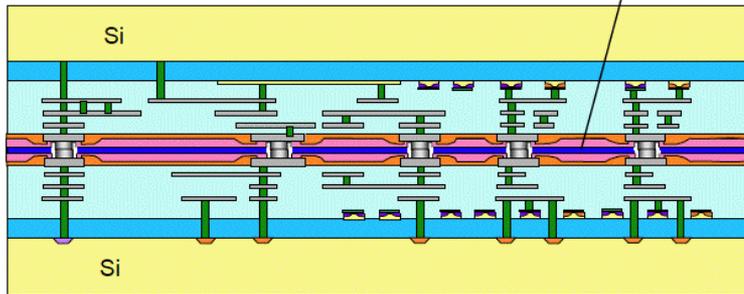
Form μ -bump



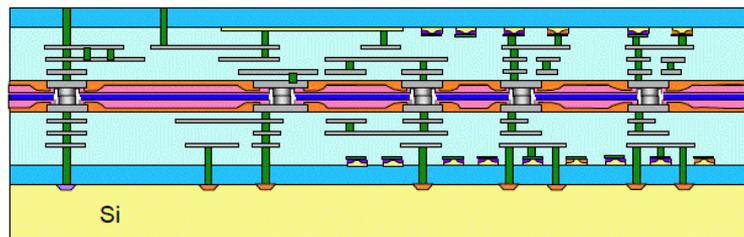
Form μ -bump



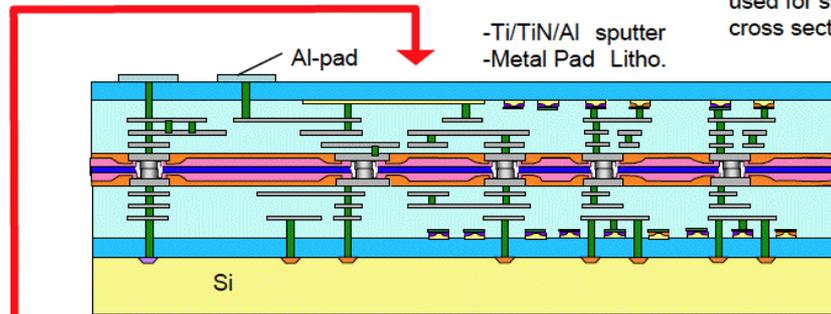
-Stack wafer with μ -bump and adhesive



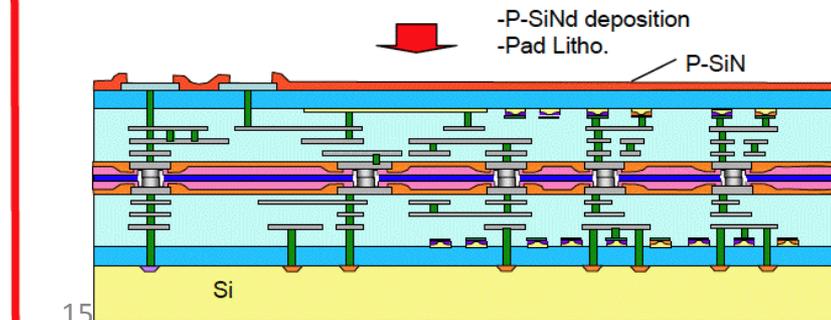
-Si etch
-SiO₂ slight etch



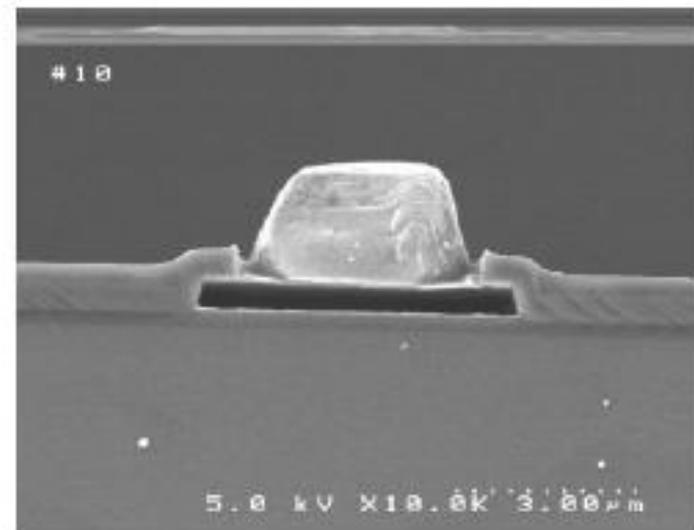
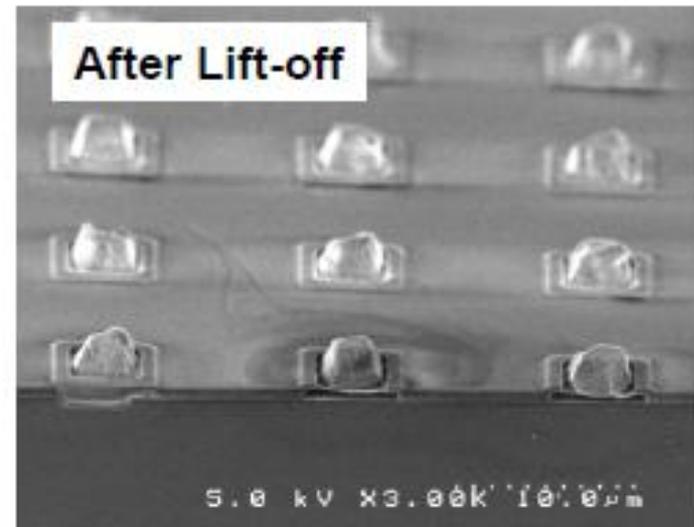
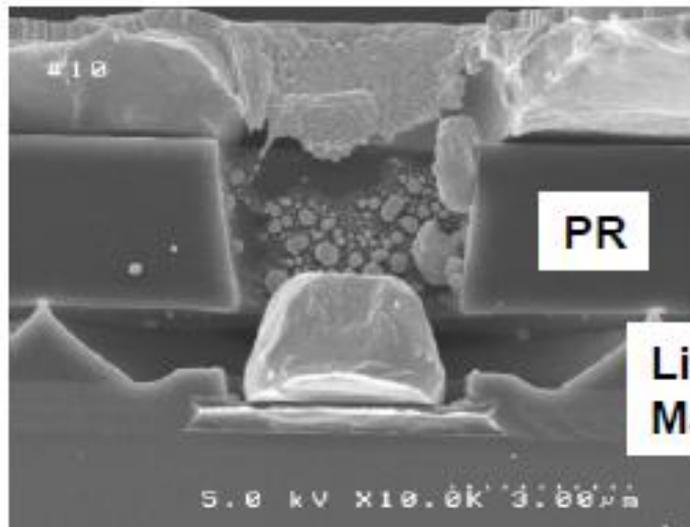
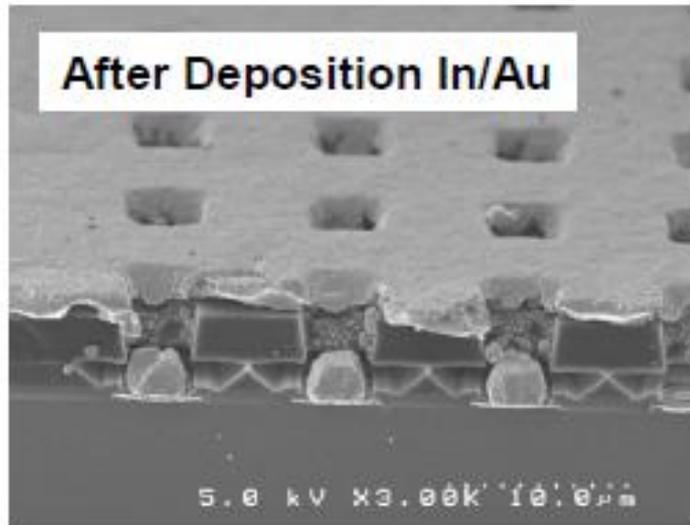
-Ti/TiN/Al sputter
-Metal Pad Litho.



-P-SiN deposition
-Pad Litho.

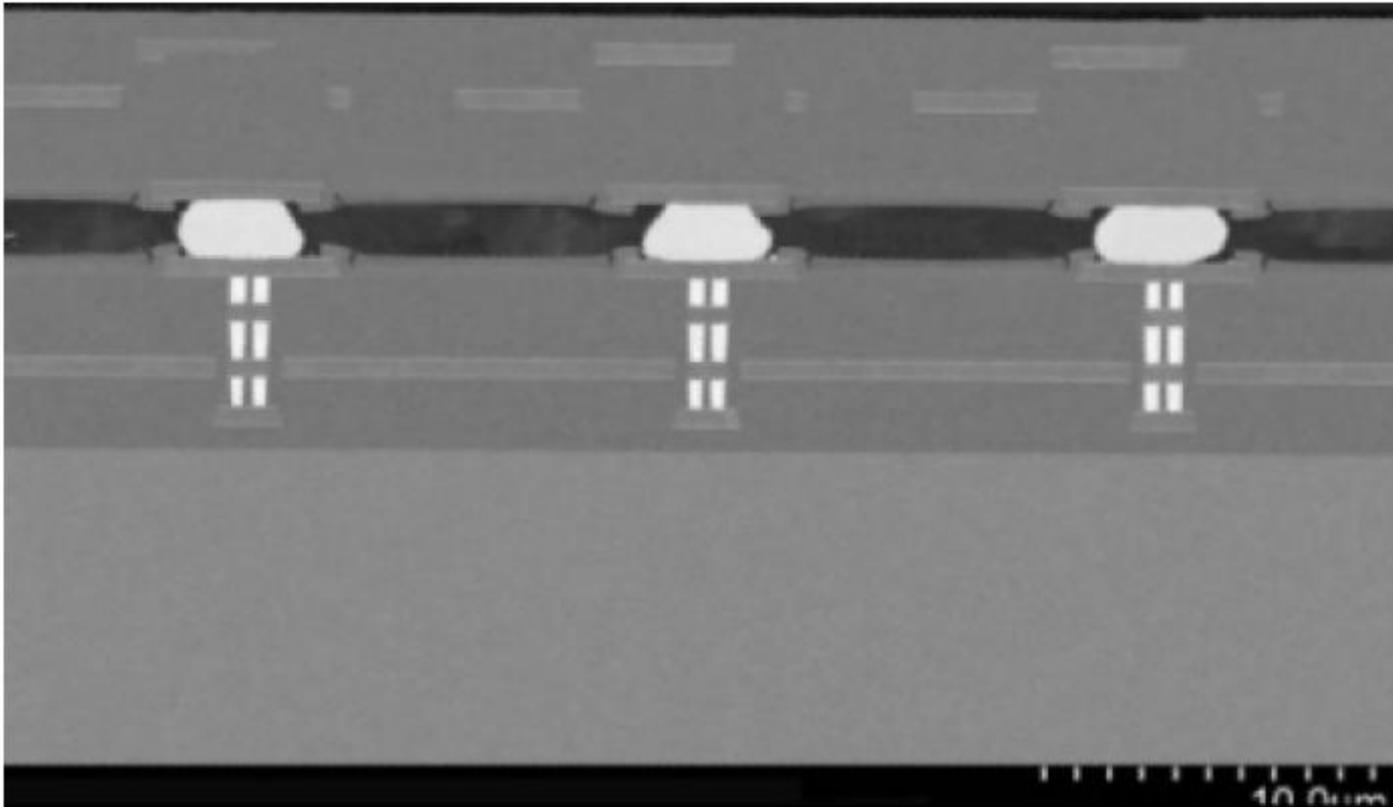


μ -bump process ($2\mu\times 2\mu$)



Cross sectional view:

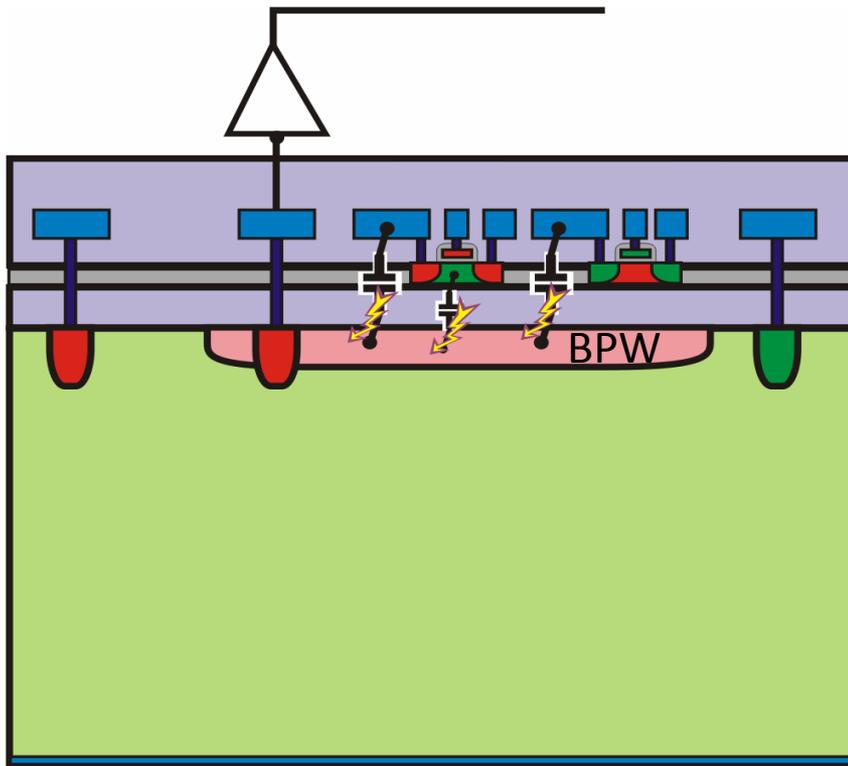
Test chip with adhesive



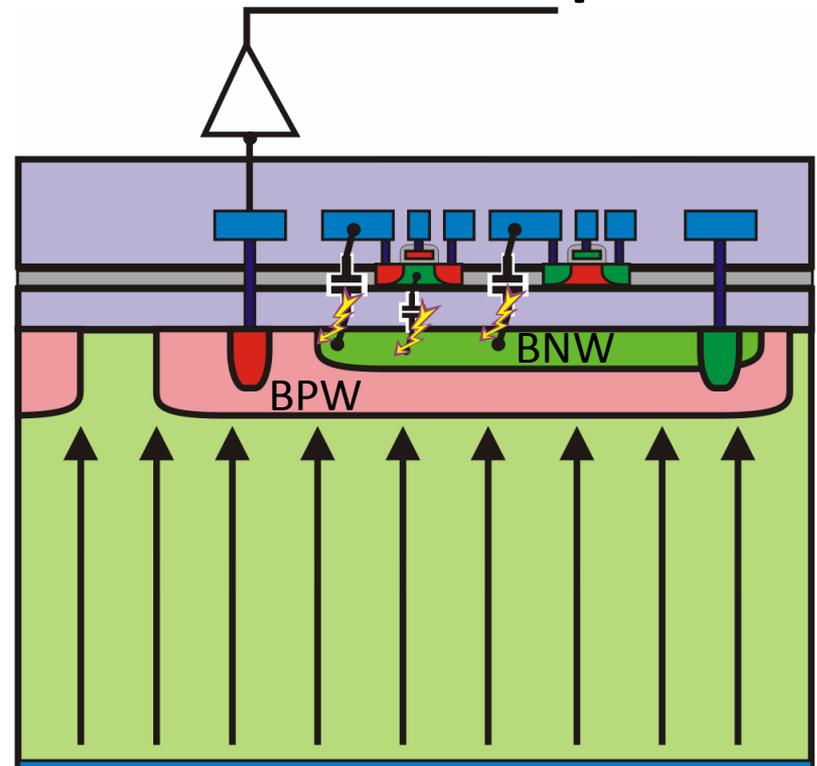
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MAMBO IV

Nested well structure concept



Direct coupling paths creating feedback to the input of an in-pixel amplifier, additionally multiple capacitive feedback paths are created that may lead to instability of the processing chain



In order to achieve:

- Efficient screening of capacitive couplings (BNW)
- homogenous electric field filling the whole detector volume (BPW)

Silvaco Simulations

Aggressor (metal line)

Pixel 1

Pixel 2

To amplifier

To ground

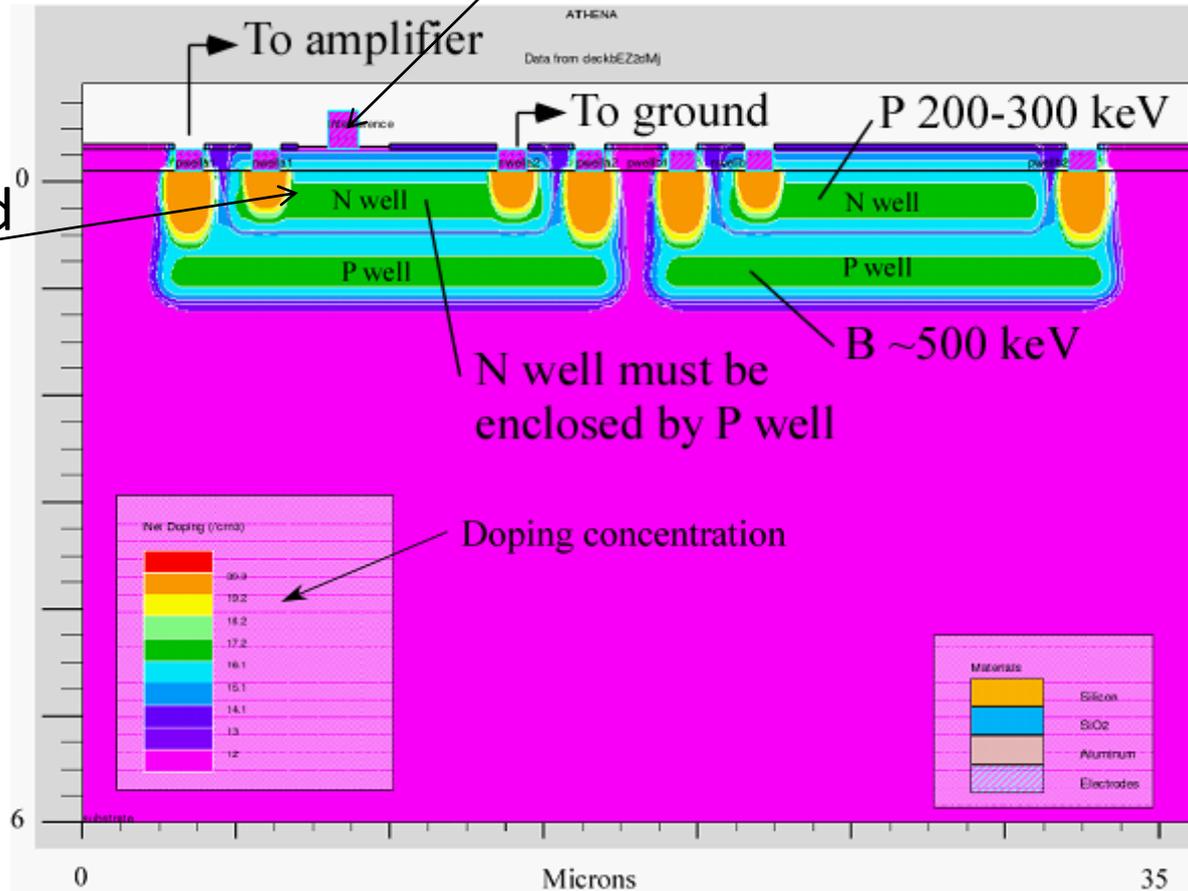
P 200-300 keV

Acts as an ac ground

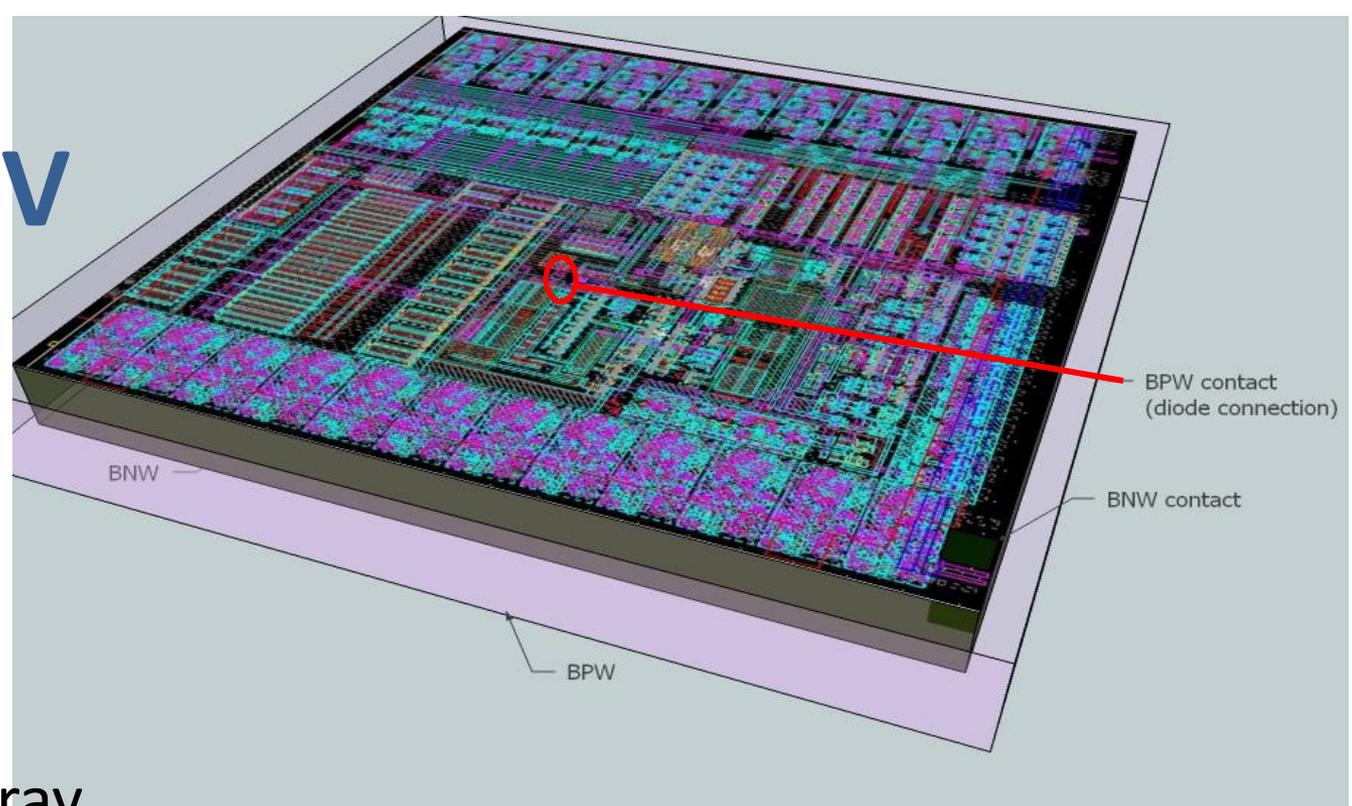
N well must be enclosed by P well

B ~500 keV

Doping concentration



MAMBO IV



- 41 x 42 pixel array
 - Addition of the nested wells should completely remove any coupling from the CMOS circuitry into the diodes in the substrate
 - Current pixel cell with added individual pixel testing capability is $105\mu\text{m} \times 105\mu\text{m}$
 - Pixel size easily reduced to $75 \times 75\mu\text{m}$ and 1 pf capacitance by removing individual pixel testing
 - The preamplifier and shaper designs had to be modified to accommodate a larger input capacitance.

Conclusions

- MAMBO is a counting ASIC with testing capability of each individual pixel
- MAMBO III submitted in Jan 2010
 - 2D fabrication May 2010
 - Technological problems with 3D μ bump bonding process
 - Requires process adjustments and repetition of deposition
- MAMBO IV submitted in Aug 2010
 - Process developed in collaboration with OKI for elimination of cross talk between detector and electronics

Thank you