

DCal: A Custom Integrated Circuit for Calorimetry at the International Linear Collider

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Abstract—A research and development collaboration has been started with the goal of producing a prototype hadron calorimeter section for the purpose of proving the Particle Flow Algorithm concept for the International Linear Collider. Given the unique requirements of a Particle Flow Algorithm calorimeter, custom readout electronics must be developed to service these detectors. This paper introduces the DCal or Digital Calorimetry Chip, a custom integrated circuit developed in a 0.25 μ m CMOS process specifically for this International Linear Collider project. The DCal is capable of handling 64 channels, producing a 1-bit Digital-to-Analog conversion of the input (i.e. hit/no hit). It maintains a 24-bit timestamp and is capable of operating either in an externally triggered mode or in a self-triggered mode. Moreover, it is capable of operating either with or without a pipeline delay. Finally, in order to permit the testing of different calorimeter technologies, its analog front end is capable of servicing Particle Flow Algorithm calorimeters made from either Resistive Plate Chambers or Gaseous Electron Multipliers.

I. INTRODUCTION

THE International Linear Collider (ILC), as it is currently specified, has a number of fairly stringent requirements[1][2][3]. Among them is a Jet Energy Resolution of better than $30\%/\sqrt{E_{\text{jet}}}$. Traditional calorimeters are sizable towers consisting of alternating layers of absorber plates to incite showers and active media to detect those showers. The energy of these detected showers is then summed over a broad dynamic range to determine the total energy that was deposited in the tower [4]. Unfortunately, traditional calorimeters do not respond equally to photons and hadrons ($e/h \neq 1$) and this leads to poor resolutions that are typically greater than $100\%/\sqrt{E_{\text{jet}}}$. Traditional calorimeters can, however, be tuned by adjusting the material and thickness of the absorber plates and active media, thereby equalizing the photon and hadron response and improving Jet Energy Resolution. However, to date, the best Jet Energy Resolution achieved with traditional technology has been the Zeus calorimeter which tuned its scintillator detector and uranium absorber plates resulting in a Jet Energy Resolution of $50\%/\sqrt{E_{\text{jet}}}$ [5]. This is still not good enough for the ILC. Therefore, with traditional technology inadequate to the task

required by the design, researchers must turn to new technologies.

Particle Flow Algorithms (PFAs) represent such a technology. Rather than attempting to sum up the total energy of all particles, regardless of origin, that pass through a tower, a PFA Calorimeter, as the name suggests, attempts to follow the flow of each shower caused by each individual particle. The large calorimeter tower of traditional designs with its broad dynamic range is replaced by a three dimensional array of small calorimeter segments, each with a much smaller dynamic range. Moreover, in a PFA calorimeter, calorimetry information is combined with tracking information to help separate showers caused by neutral and charged particles. The location of the shower, obviously, can be determined from the locations of the hit segments, much like track finding in a vertex detector. The total energy of the shower can be determined by summing the total energy deposited in the various segments hit by the shower. From an engineering perspective, PFA Calorimeters trade reduced segment size and increased output bandwidth for decreased dynamic range. In fact, with a calorimeter segment size reduced to approximately 1 cm^2 , the dynamic range of the segment can be reduced to only one bit.

The CALICE Collaboration has been established to investigate various calorimetry technologies for implementation in the ILC[6]. As part of that collaboration, a 1 m^3 section of PFA digital hadron calorimeter is being developed for eventual study in the Fermilab test beam. This section will have approximately 400,000 calorimetry segments, each approximately 1 cm^2 and stacked longitudinally 40 layers deep. At the present time, there are two leading candidates for PFA calorimeter technologies, Resistive Plate Calorimeters (RPCs) or Gaseous Electron Multipliers (GEMs). RPCs provide more signal magnitude and GEMs provide greater speed, but each is capable of providing highly segmented calorimetry data. Both technologies must be evaluated in the test beam.

The electronics required to read out a PFA device are very different from traditional calorimetry electronics. Each 1 cm^2 channel needs to be read out individually, discriminated to determined hits and then time-stamped for later reconstruction. All hit segments from a particular time slice need to be gathered as a "snapshot" of the calorimeter for that time slice. Because of the vast number of segments, statistics suggests that even under high luminosity an individual segment will not be hit very frequently. In the test beam, for example, analysis suggests that successive hits will be separated by more than a millisecond.

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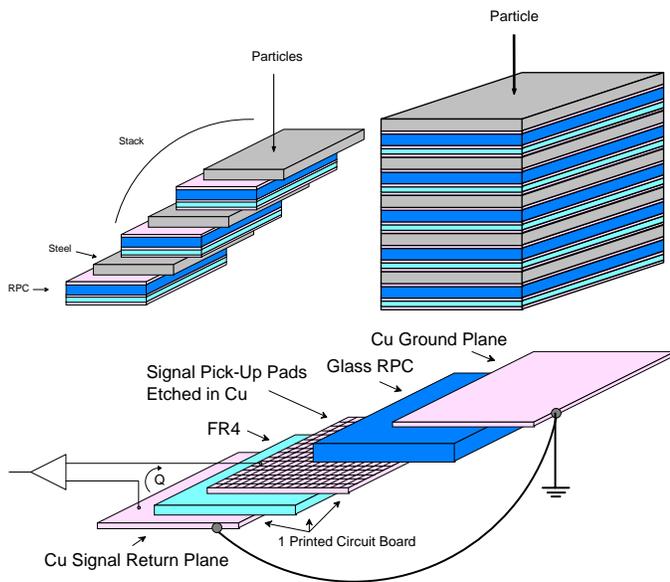


Fig. 1 - An abstraction of a PFA calorimeter. Each layer consists of a steel absorber plate, a GEM or RPC-based highly-segmented active layer, and a geometrically matched printed circuit board with custom readout electronics. Though the figure specifically refers to RPCs, either GEMs or RPCs could be used. For the purpose of the present discussion, GEMs and RPCs are interchangeable.

Fig. 1 shows an abstraction of a PFA calorimeter with its front end readout electronics. Each layer consists of an RPC or GEM layer geometrically matched to a printed circuit board with custom electronics for segment readout. Within each printed circuit board, every 8x8 array of calorimetry segments is controlled by a single custom integrated circuit, the DCal or Digital Calorimetry Chip.

The requirements for the chip are fairly straightforward. They are as follows:

1. The chip must service 64 identical channels of PFA calorimetry segments.
2. The chip must be able to handle either GEMs or RPCs.
3. For each channel, the chip must receive, amplify, and shape input signals and discriminate hits. For the whole array, the chip must tag each time slice with a 24-bit timestamp, and notify downstream electronics of all events.
4. As this is a prototype, it must be flexible. Therefore, it must be capable of generating its own internal triggers in response to the presence of hits or accepting external triggers regardless of the existence or absence of hits.
5. Similarly, the chip must be capable of using or bypassing an internal, 20-stage deep pipeline delay.
6. The chip must supply all of its own biases through a slow programming interface.
7. The chip must pack each triggered snapshot into a data frame and output that data frame in a serial stream as soon as possible.

8. When not outputting data frames, the chip must output status information and a synchronization word to aid communication with downstream electronics.
9. Above all, the readout architecture cannot be allowed to limit system performance.

The following sections will describe the DCal chip in detail and display the results of simulations and bench tests that verify its compliance with the system requirements.

THE DCal ARCHITECTURE

Fig. 2. shows a block diagram of the DCal Chip. RPC or GEM signals are picked up through the inputs and amplified, shaped and discriminated by the front end circuits which convert the analog inputs into asynchronous digital pulses of highly variable width. Unwanted channels are killed by the Mask Register. The Hit Catchers convert the various digital pulses into signals exactly one time slice wide and delayed by one time slice regardless of their original magnitude or time over threshold. A 24-bit time stamp register is tagged to every time slice. With the 100ns sample time expected in the test beam, this means that the register can run for more than a full second before time stamps begin to repeat themselves. The Pipeline Delay can hold signals for 20 time slices or it can be bypassed as the user desires. Data enters the 8-stage FIFO as a result of a trigger from the Trigger Control logic. The origin of that trigger can be internal or external to the chip, depending on the user's desires. Regardless of the triggers origin, once a time slice is triggered, the 88 bits of time slice data (24 bits of time stamp and 64 bits of hit/no hit information) are dropped into a data push architecture. That is, whenever there is data present in the FIFO, the FIFO and the Steering Logic work together to output that data through the Serializer. No external request is necessary. When no data is present in the FIFO, the Steering Logic and the Serializer are free to output synchronization and status information.

At the top of Fig. 2 is a slow control interface similar to an SPI interface. It uses the system clock, a control line to indicate when shifts are occurring, a serial input and a serial output. All commands in the slow controller contain a chip address that can be set through the DCal's pads or can be left unconnected to assume a default value. This permits point-to-point chip control or bussed chip control. The slow controller is capable of accessing all analog and digital values needed by the chip. This includes the front end biases, the discriminator thresholds (V_{th}), the calibration pulse height (Q_{in}), and all digital control signals. The slow control also accesses the Kill and Inject registers (Mask Registers) through which a user can mask off unwanted channels (kill) and/or connect one or more channels to an on-chip pulser circuit (inject) for calibration and testing. The actual pulsing of the pulser circuit is controlled via an external digital signal that can be connected to multiple chips, resulting in a highly reproducible system calibration test.

The analog front end is identical to that used in the FSSR2 [7] except that the 3-bit analog-to-digital conversion has been removed from the DCal. It operates with one of two possible gains that are programmable via a feedback capacitor in the

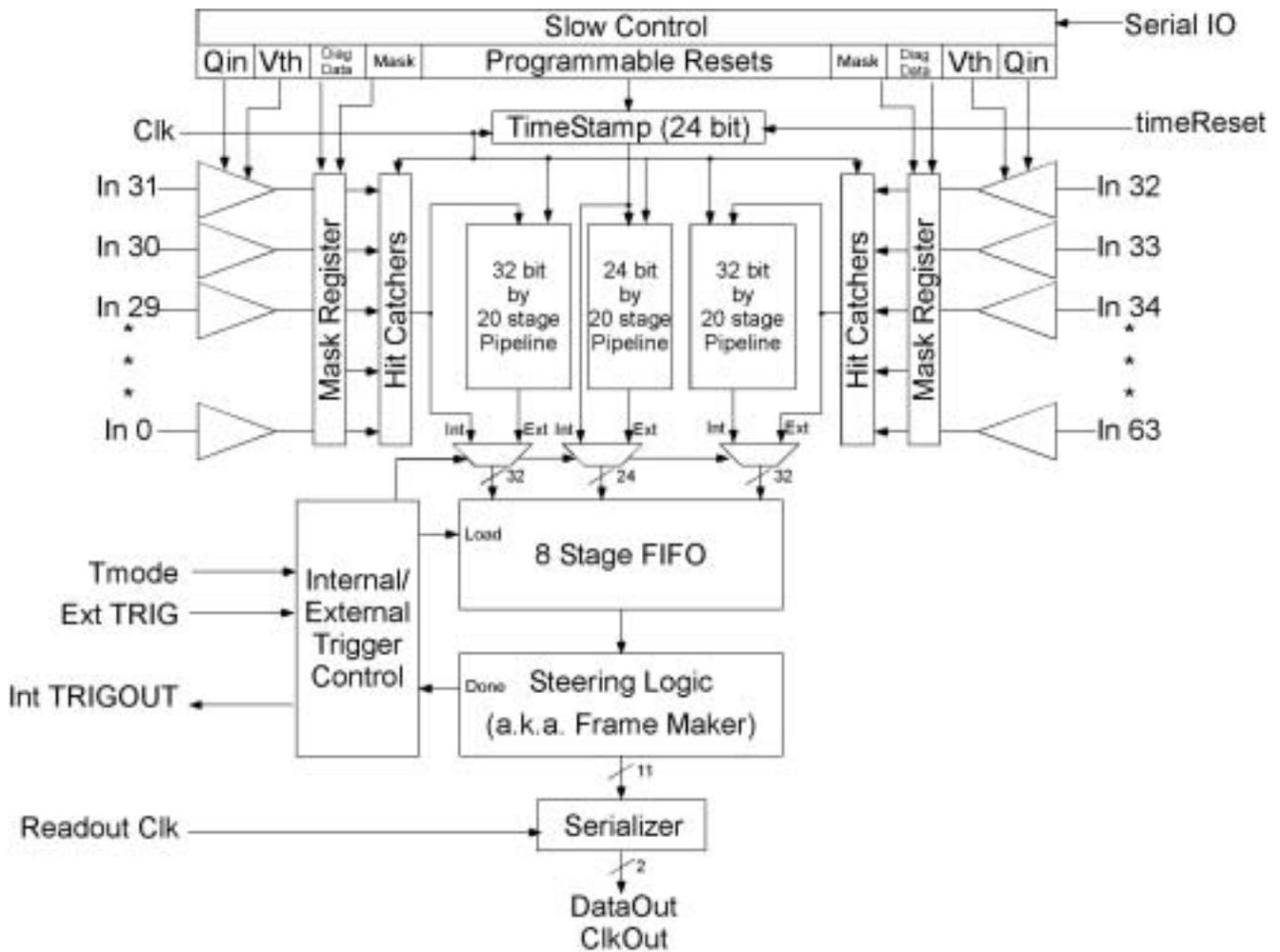


Figure 2 - The DCal Block Diagram

preamplifier which can be switched into our out of the circuit. The overall preamplifier feedback capacitor can therefore be set to 100fF or 150fF as the user desires. This programmable gain enables this front end to be usable by either RPC-based PFA calorimeters or GEM-based PFA calorimeters. The front end's CR-(RC)² shaper also has four programmable shaping times of 65ns, 85ns, 100ns, and 125ns. The front end has a baseline restorer circuit that can be enabled or bypassed as desired. The baseline restorer can be used to cancel baseline shifts in the shaper output that would affect the discriminator threshold. Each channel's discriminator is controlled by a single, universal threshold voltage value that is programmable through the slow controller. There is no capacity to adjust the threshold on a channel-for-channel basis.

The DCal Chip benefits tremendously from the fact that data is converted to digital information immediately and dealt with as digital data from that point onward. Therefore, for the most part, the circuits are simple, fast and small. They also consume almost no static power. These type of advantages have been discussed in recent presentations on trends in circuit design for physics experiments [8].

The Hit Catcher (shown in Fig. 3) is a simple circuit used to smooth out the variations present in the discriminator output of each channel. Hits can occur at any time in the sample

period. Moreover, differences in hit magnitude and channel recovery rate can result in differences in time-over-threshold. The PFA requires that each hit, no matter how small, be counted and that each hit, no matter how large be counted only once. The discriminator output is connected to the clock input of the first flip-flop. This ensures that only the rising edge of each hit is counted, thus guaranteeing that each hit is counted once and only once. The data input of the first flip-flop is connected to a universal "Accept" signal. This signal is programmable through the slow controller and provides the user with the ability to enable or disable front end signal processing for the entire chip. For example, turning off the Accept signal will prevent the chip from responding to noise hits that might result from programming the mask register. The second flip-flop converts the asynchronous input into a synchronous output pulse that lasts from one rising edge of a sample period to the next. The rest of the circuitry in Fig. 3 is reset circuitry that ensures that the digital dead time of the circuit is only two sample periods. This is much less than the channel dead time of RPCs in particular. It is also much less than the analog dead time of the front end. This helps to ensure that the read out architecture does not place limits on the overall system efficiency of the PFA calorimeter.

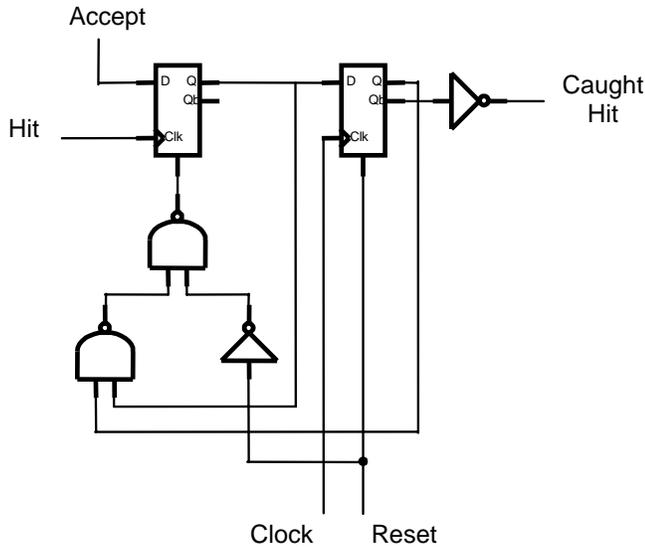


Fig. 3 - The Hit Catcher

The Internal/External Trigger Control is simple combinatorial logic. Internal Triggers are generated by fast, distributed OR signals taken either directly from the output of the Hit Catchers (if the Pipeline Delay is disabled) or taken from the output of the Pipeline Delay (if it is enabled). External Triggers come straight from a pad, and the selection of Internal versus External Triggers is programmed through the slow controller.

The DCal Chip outputs a serial bit stream that is organized into Output Words as shown in Fig. 4. Each word is 11 bits long and is output within one Sample Period. The first bit output is a sync bit and it is always a 1. The next eight bits are the unique data of the word. There are four Output Word types, and the last two bits of the Output Word indicate whether a word is Sync, Status, Time, or Hit. The Sync indicator is a 00, and the data portion of the Sync word is always eight zeros. Therefore, the entire 11 bits of the Sync Word (one 1 followed by eleven 0s) is, by definition, a unique signature that downstream electronics can use to facilitate communication. The Status Word contains several data flags such as Accept/Reject Status, Pipeline Enable/Disable Status, Trigger Internal/External Status, etc. In the absence of data, the Steering Logic and the Serializer output one Sync Word followed by one Status Word. When hit data is triggered into the 8-stage FIFO, it is output as an 11-word data frame following the next Sync Word. The first three words of the data frame are Time Words and the data portions of those words contain the 24-bit time stamp of the triggered word from most significant bit to least significant bit. The next

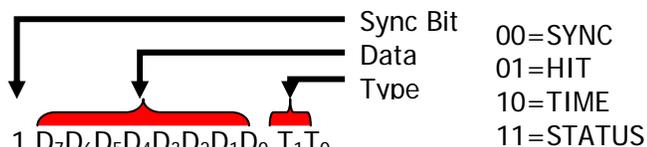


Fig 4 - The format of the Output Word

eight words are Hit Words and the data portions of those words contain the 64-bit hit/no hit snapshot of the 8x8 channels controlled by the DCal.

All data transitions both into and out of the 8-stage FIFO occur on the rising edge of the Sample Clock. Transitions into the FIFO occur 88 bits at a time (24 bits of time stamp plus 64 bits of snapshot). Transitions out of the FIFO occur 8 bits at a time over 11 Sample Periods. The efficiency of the chip as a function of luminosity turns on the depth of the FIFO. The greater the luminosity, the more frequently triggers occur and the faster the FIFO will fill. If the FIFO fills before it can be emptied, data is lost.

RESULTS AND CONCLUSIONS

Prior to fabrication, the DCal was simulated extensively using both Verilog and SPICE. Monte Carlo simulations with expected hit rates were used, but since a 1 kilohertz hit frequency is expected in the test beam, these simulations, though successful, did not exhaustively test the readout architecture. Directed simulations in which different channels were hit every N Sample Periods were also performed where N was varied over a broad range. Simulations such as this revealed that for ordered data, the maximum hit frequency tolerated by the readout architecture is extremely high, in excess of 9 MHz. Of course, ordered data is not expected in either the test beam or the ILC. Therefore, a combination of directed simulation with a Monte Carlo-like probability of hits on successive Sample Periods was performed to simulate a more realistic high luminosity scenario. Under this scenario, it was found that an aggregate hit frequency of 470 kHz over 2000 Sample Periods did not yield any errors. Moreover as the aggregate hit frequency was increased, i.e. as the

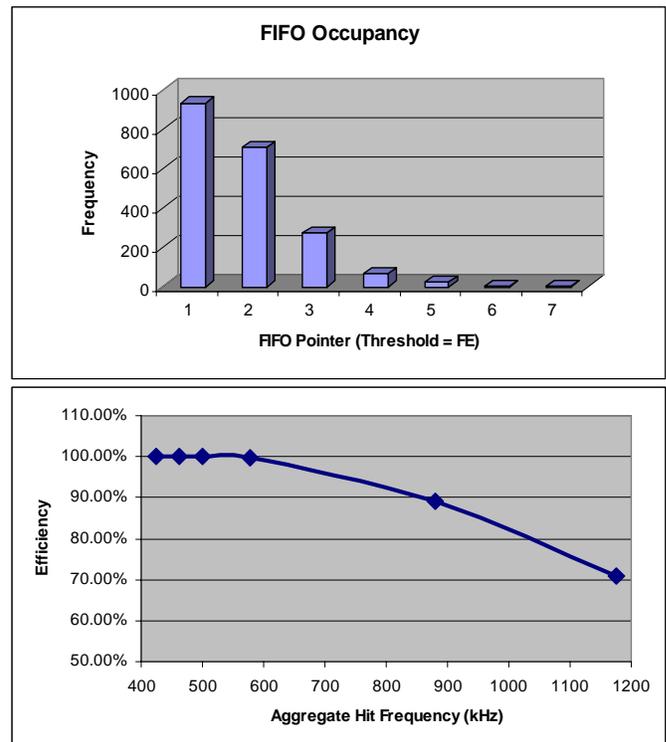


Fig. 5 - DCal Chip Efficiency

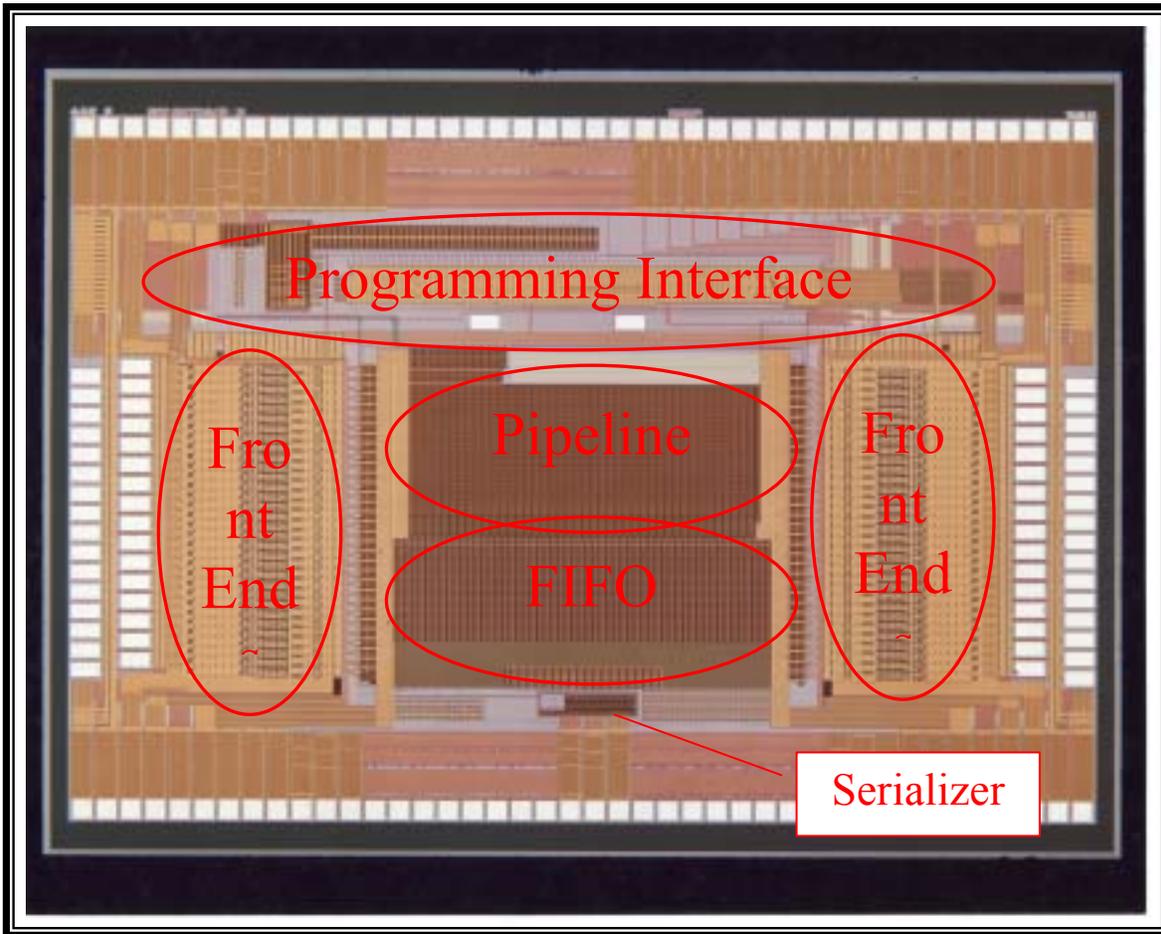


Fig. 6 - The DCal Chip

luminosity was increased, the efficiency of the DCal Chip rolled off smoothly as shown in Fig. 5. Also shown in Fig 5 is that for an aggregate hit frequency of 470 kHz, the average occupancy of FIFO stages falls off exponentially.

The chip was fabricated in a 0.25um CMOS process and bench test show that the chip performs as expected by simulation. A picture of the chip is shown in Fig. 6.

In conclusion, the chosen architecture is shown to be approximately 470 times as fast as needed for the expected hit rate in the test beam. Moreover, the limiting factor in efficiency is the Read Out FIFO which can be easily scaled. Since the occupancy of the stages of the FIFO fall off exponentially, modest increases to the FIFO depth should result in dramatic increases in chip performance at higher and higher luminosity. In short, the architecture seems applicable regardless of the beam structure of the ILC. The fact that the PFA permits this chip to convert to digital immediately is also promising for the ILC because of the reduced power consumption of digital circuits and because more power-reducing techniques, such as power cycling, can be applied to digital circuits.

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