SOI Detector with Drift Field due to Majority Carrier Flow - an Alternative to Biasing in Depletion

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***Abstract*—This paper reports on a SOI detector with drift field induced by the flow of majority carriers. It is proposed as an alternative method of detector biasing compared to standard depletion. N-drift rings in n-substrate are used at the front side of the detector to provide charge collecting field in depth as well as to improve the lateral charge collection. The concept was verified on a $2.5 \times 2.5\,\mathrm{mm}^2$ large detector array with 20 μm and 40 μm pixel pitch fabricated in August 2009 using the OKI semiconductor process. First results, obtained with a radioactive source to demonstrate spatial resolution and spectroscopic performance of the detector for the two different pixel sizes, will be shown and compared to results obtained with a standard depletion scheme. Two different diode designs, one using a standard p-implantation and one surrounded by an additional BPW implant will be compared as well.**

***Index Terms*—SOI, radiation detection, monolithic active pixel, drift field, unidepletion**

I. Introduction

SOI (Silicon on Insulator) technology using a high resistivity handle wafer offers unique opportunities for particle detection and the construction of compact and monolithic pixel sensors. KEK has organized various MPW (Multi Project Wafer) runs using a modified OKI process in the past and has demonstrated the feasibility of the concept [1]. This process is based on a high resistivity n-type handle of up to 1kOhm-cm material and p-type implants that penetrate the buried oxide (BOX) to form collecting diodes. These diode implantations can be made very small (on the order of 1 um diameter), which result in a very low input capacitance of about 3 fF. The process also offers n-implantations through the BOX.

A. Standard Depletion versus Drift Biasing

In the standard configuration (illustrated in Fig. 1), the detector is depleted by applying positive voltage at the n-backside with respect to the p-diode implantation at the front side. The depletion zone, and hence the volume from which charge is collected at the front side diode, grows with the applied backside voltage. To achieve a fully depleted detector (assuming a standard $\sim 300\,\mu$m thickness) voltages of 100 V and more are needed. However, application of high backside voltage results in the presence of lateral potential gradients under the BOX. Issues with the CMOS electronics, known as back gate effects, have been observed [2]. This back-gating causes threshold shifts in the CMOS transistors. As a consequence minor changes in the biasing settings of the pixel electronics as well as a complete failure of the signal processing chain have been observed [3].

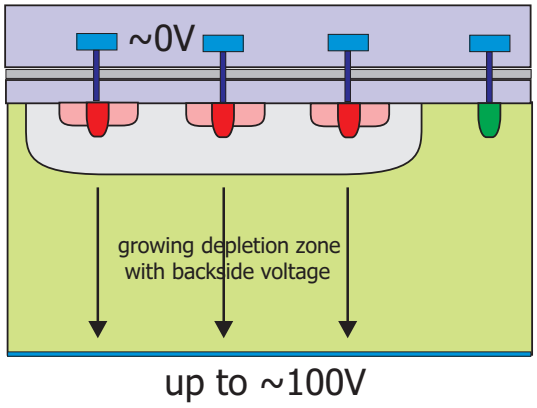

Fig. 1. Illustration of biasing a detector in the standard depletion scheme by applying a voltage at the backside with respect to the potential at the front side diode implantation.

As an alternative biasing scheme, primarily to enhance standard MAPS detectors, a scheme in which the drift field results from the flow of majority carriers, called the unidepleted scheme, has been proposed for standard CMOS process [4]. We propose using this method of detector biasing in a SOI process and extend the concept by generating a vertical drift field in addition to the lateral field at the front side. The implementation of the concept is illustrated in Fig. 2. The n-type substrate is contacted at the backside as well as the front side. By applying a different potential on both electrodes a drift field is generated that provides charge collection towards the front side of the detector. It is important to note that the drift field is generated by flow of the majority carriers, in this case electrons in n-substrate. Holes, resulting from ionization, are collected by the p-implants that are biased appropriately with respect to the front side n-implants. The n-type implants are realized as rings inside which the p-type diodes are seated. Laterally, the rings function like lenses to further improve charge collection. It will be shown that backside voltages of about 10 V are sufficient for operating of the detector in drift

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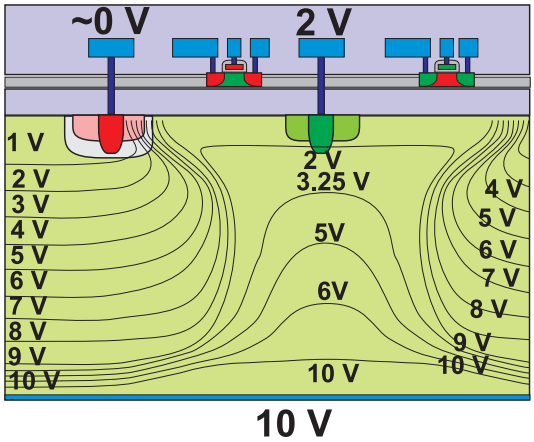

Fig. 2. Illustration of biasing a detector in the drift scheme using 10 V at the backside and 2 V at n-rings on the front side.

scheme. This greatly reduces the back gate effect, eliminating it's the impact, as well as generally reducing the net electric field across the BOX.

B. Silvaco simulations of the SOI detector in drift and depletion scheme

To show the advantages of the drift biasing, 2-dimensional Silvaco simulations of the SOI detector have been performed. Fig. 3 shows the potential distribution obtained from an ATLAS simulation using a 250 μm thick handle wafer with $8.4 \cdot 10^{12}\,\mathrm{cm}^{-3}$ phosphorus doping. In the simulation the backside is biased at 10 V, the p-diode implant is reset to 0.2 V, and the n-implants at the front side are biased at 2 V. The simulation clearly shows the vertical drift field from the backside through the entire detector volume towards the collecting p-diode situated in the middle of the pixel. Close to the front side, the lateral focusing effect can be observed as well.

Fig. 4 shows the potential distribution of the same detector configuration using the standard depletion scheme. For the simulation the potential of the n-rings at the front side has been set to the same potential as the backside (10 V) to eliminate the drift field. Only a small fraction of the detector is depleted at 10 V, and holes will primarily be collected only from a depth of about 20-30 μm.

One important figure of merit of the drift scheme is the charge collection time, which can be tuned by the applied drift potential. Assuming a constant electrical field E=U/d inside the detector and a the carrier velocity to be v=μE, the maximum charge collection time (meaning charge collected from the backside) can be computed according to:

$$U = \frac{d^2}{t \cdot \mu} \tag{1}$$

with U being the applied drift voltage, d the detector thickness and μ being the carrier mobility. For a detector thickness of 250 μm drift voltages of 10-15 V are enough to provide a charge collection time on the order of 100 ns, considered sufficient for most applications. Note that the charge collection time would be improved by about a factor of 3 by using p-type handle material and collecting electrons instead of holes. This can also reduce the necessary drift potential significantly.

A second important factor in the drift scheme is the current that is needed to bias the detector. This biasing current can be computed by simply following Ohms Law and is dictated by the resistivity of the detector material and the applied drift potential. For a 500 Ω-cm handle material and a drift voltage of 13 V, the resulting biasing current per $20 \times 20\,\mu$m pixel area is as low as 4 μA, equivalent to 1 A per cm^2. It becomes clear that only a process using high resistivity handle wafer can be used to generate a vertical drift field. For low resistivity CMOS substrate the biasing current would be intolerably high. We expect a resistivity of up to 1 kΩ-cm for the OKI process, but dedicated handle materials could go up to several kΩ-cm.

To summarize, applying the drift scheme in OKI-SOI technology enables the fabrication of true monolithic, compact devices that offer a reasonably thick detection layer at low bias voltages, and hence do not suffer from negative back gate effects. A large sensitive volume is especially attractive for applications that use low energy X-ray radiation. Also, modern tracking applications demand the use of thin devices down to 50 μm thickness. In this case a collecting drift field all the way through the substrate could provide excellent tracking

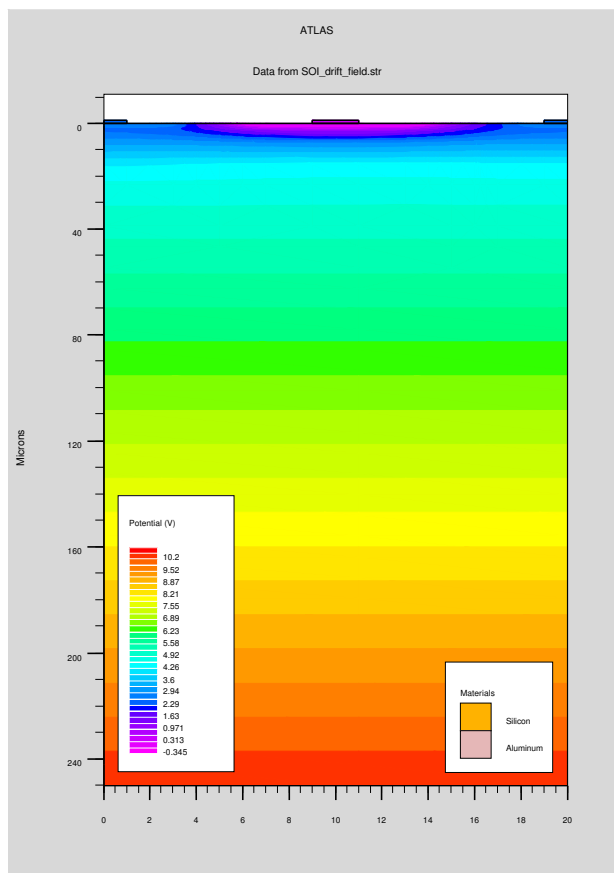

Fig. 3. Silvaco (ATLAS) simulation of a 250 μm thick detector applying drift scheme with 10 V at the backside.

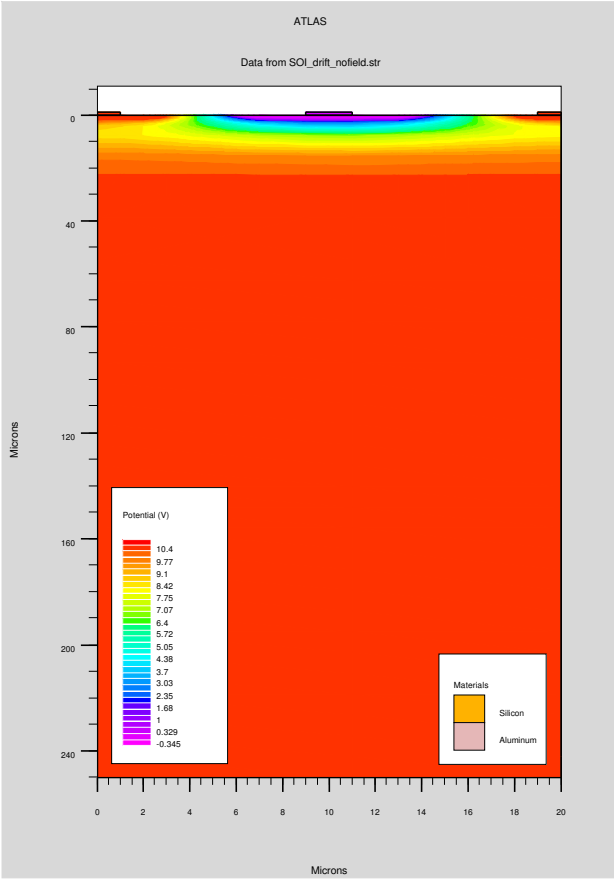

Fig. 4. Silvaco (ATLAS) simulation of a 250 μm thick detector in standard depletion scheme with 10 V at the backside.

performance while keeping the biasing voltage and current, and therefore power, at a manageable lower level.

II. First realization of the drift concept in the OKI-SOI process

The novel biasing scheme has been realized on the August 2009 OKI run organized by KEK. This submission uses Czochralski material for the handle wafer. A 2.5mm x 2.5mm large sensor array has been fabricated. Pixels with two different sizes, 20 μm and 40 μm, were implemented within the sensor matrix to allow comparative studies. Simple small-size p-implants, as well as p-implants with a surrounding lightly doped p-well, BPW (buried p-well), that has been recently introduced to the process, were used as collecting diodes. An overview of the chip is given in Fig. 5.

To have full access in studying the detector properties, the readout chain has been kept as simple as possible. A 3T (3-transistor) pixel scheme has been chosen, as shown in Fig. 6. A low threshold voltage source-tied pmos transistor is used as a source follower. Since the pixel size offers ample space to incorporate a 3T scheme, transmission gates are used for the reset (reducing charge injection onto the input node) and select switch. The biasing of the source follower is done at the end of each column, where additional multiplexers are situated to select one pixel of the matrix for readout at a time.

A clamping diode (ppn) is implemented to protect the input node, and can be enabled by using an appropriate clamping voltage V_{clamp}. In the measurements presented in this paper the clamping voltage was kept floating.

Fig. 7 shows the CADENCE layout of the 40 μm pixel cell. A minimum size p-diode implant of 1.2 μm diameter is located in the center of the pixel. Shown as well is a minimal BPW implantation of 3.6 μm diameter surrounding the p-diode. The 40 μm pixel cell has 2 drift rings, one at a distance of 10 μm around the diode and the second surrounding the pixel 20 μm from the center. The structure in between the rings is a diffusion implant (within the CMOS substrate) to modulate and study any cross current between the n-rings. It is not used and is kept floating for the measurements presented in this paper. The 20 μm pixel version corresponds to the inner 20 μm part of the 40 μm pixel with one drift ring.

Since the drift rings at the front side are biased at different potential to generate a lateral drift field and they are n-implants

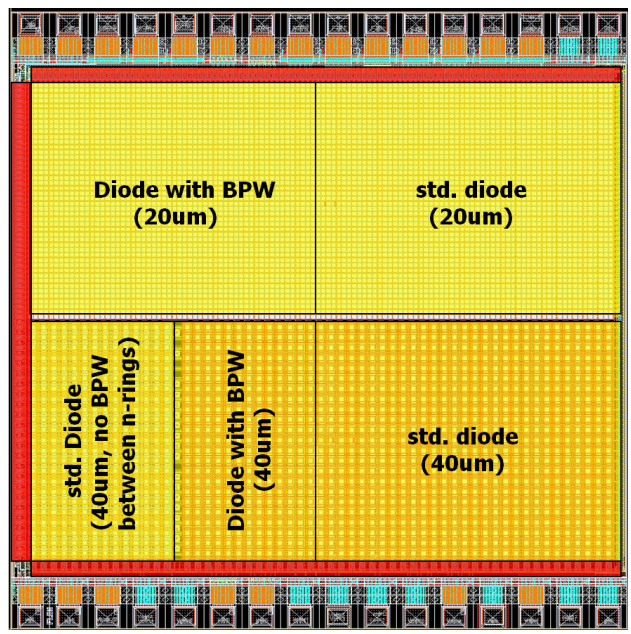

Fig. 5. Overview of the different pixel variations (with and without BPW, 20 μm and 40 μm pixel pitch) realized on the 2.5 mm × 2.5 mm large chip.

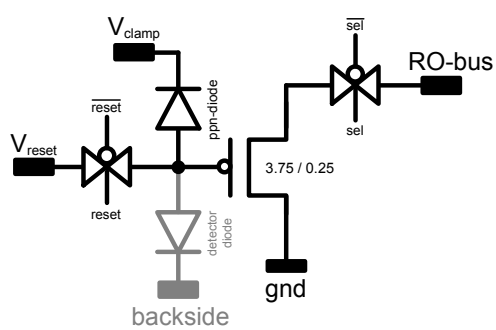

Fig. 6. Pixel schematic following a traditional 3T scheme (source follower, reset and select) with an optional clamping diode to protect the input node.

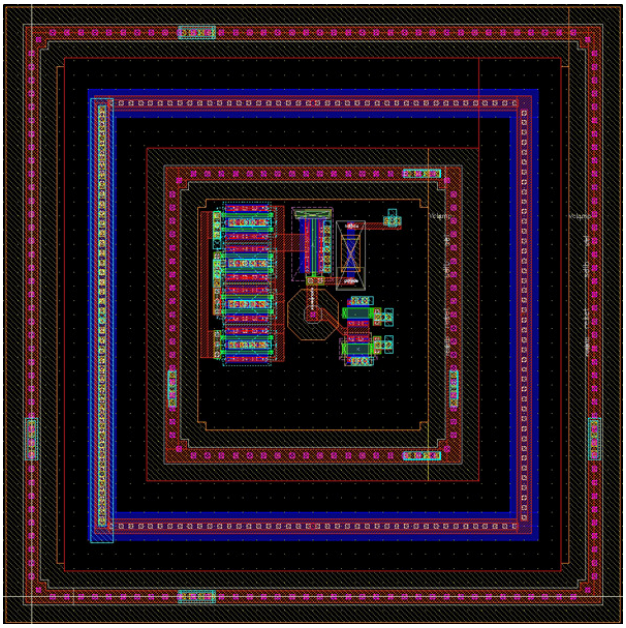

Fig. 7. Layout of the 40 μm pixel cell with 2 drift rings.

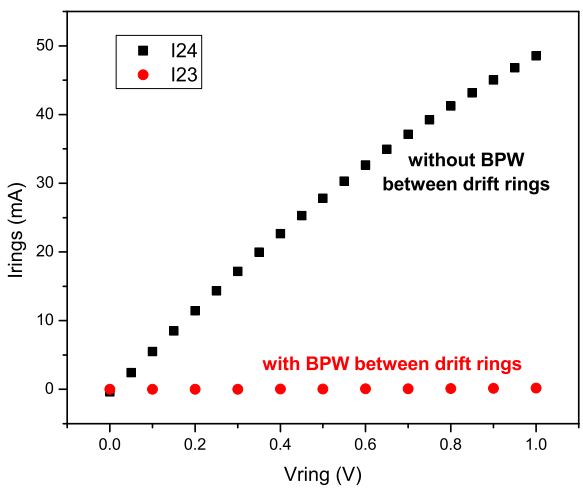

Fig. 8. Cross current (for 322 pixels) between the two drift rings in the 40 μm pixel, with and without the use of BPW as a p-stop.

in n-substrate, a large cross current can occur. To avoid this, the BPW implant is used to act as a p-stop to isolate the rings close to the interface of the BOX. Fig. 8 shows the measured cross current for a set of 322 pixels with and without the use of BPW for isolation. Without the BPW a cross current of about 150 μA per pixel occurs which is intolerably high, compared to the drift biasing on the order of a few μA through the detector. However, using BPW eliminates the cross current and demonstrates the feasibility of using multiple drift ring structures in the OKI process. This offers the design of much larger pixels while still obtaining good charge collection by using multiple drift rings biased accordingly.

III. First Results

The drift chip has been operated successfully and tested using an Iron-55 radioactive source, which emits X-rays with an energy of about 6 keV. Very first measurements will be presented in this section.

A. Operating conditions

The matrix is read out pixel by pixel using two independent output channels for the 20 μm and the 40 μm part. After the matrix is reset row wise, two successive frames are taken with a time interval of about 2.6 ms and correlated double sampling is performed to eliminate kTC noise. Averaging over 25 successive frames, continuous pedestal and noise computation is performed on a pixel by pixel bases.

Unless noted otherwise, the detector is operated in drift scheme, with 3 V at the backside, 1.5 V at drift ring for the 20 μm pixel, and 1 V and 2 V for the drift rings of the 20 μm pixel. The favored biasing would demand a much higher backside voltage of up to about 10 V. However, an increased leakage current is observed that saturates the pixel during the accumulation time when the backside voltage exceeds 3 V. A gentle cooling using a peltier element at the backside of the test board reduces the chip temperature from 30.5 °C to 15.2 °C and shows a significant reduction of the leakage current. However, even at 15.2 °C, the maximum backside voltage to operate the detector is about 3 V. The observed high leakage current does not appear in the standard depletion mode. A very plausible explanation for this observation is that the backside of the detector generates an increased amount of charge carriers. After completion of the process fabrication, the wafers are thinned to 260 μm and then aluminum coated without any advanced backside treatment. Any damage or imperfection at the backside will hence contribute to an increased charge carrier generation. In the depletion scheme charge is collected (primarily) within the depleted volume which, especially at low backside voltage, by far does not reach to the backside. In the drift scheme, however, charge is collected from the entire volume which includes any carrier generation directly at the backside. We assume that more aggressive cooling will reduce this leakage current and enable much higher drift voltages in future. Results presented here will, however, be limited to 3 V at the backside.

B. ^{55}Fe radiogram and flatfields

A micro photograph of the chip wire bonded to a test board is shown in Fig. 9. To demonstrate spatial resolution and principle operation of the detector, a tungsten mask with an engraved Fermilab logo is placed on top of the chip and is irradiated with an ^{55}Fe source. Hits are counted if the pixel signal after pedestal subtraction exceeds 8 times the pixel noise. The obtained radiogram is shown in Fig. 10. The grey scale of the radiogram ranges from 0 to 80 hits, indicated by black and white, respectively. The Fermilab logo as well as the fringe of the mask itself are clearly reproduced. The two parts of the chip that host the 20 μm pixel and 40 μm pixel sections are clearly distinguishable. In the layout of the 40 μm detector

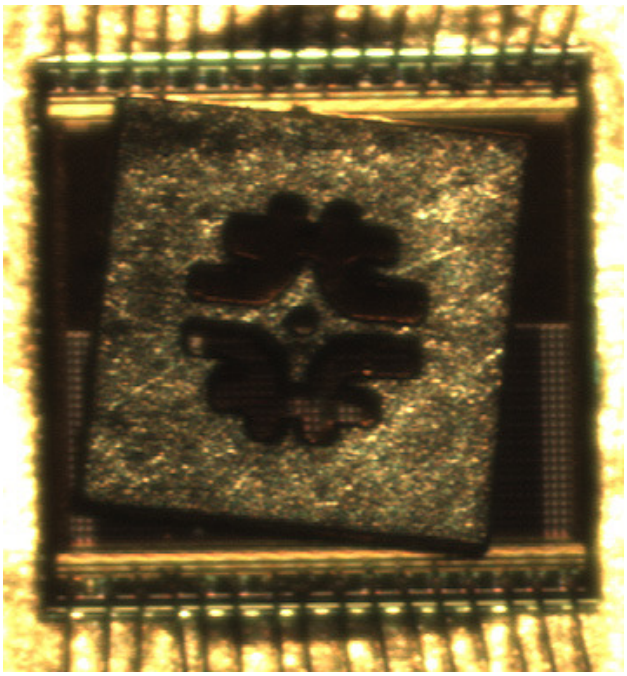

Fig. 9. Micro photography of the $2.5\,\mathrm{mm} \times 2.5\,\mathrm{mm}$ large chip, a tungsten mask with an engraved Fermilab logo is placed on top.

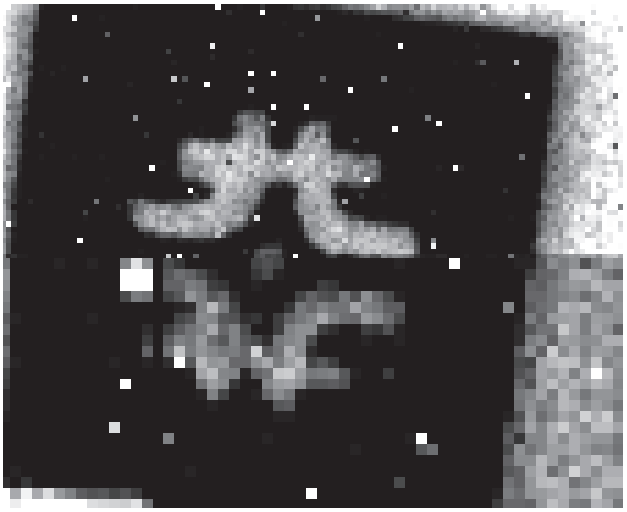

Fig. 10. ^{55}Fe radiogram obtained with the tungsten logo mask. The grey scale ranges from 0 to 80 hits, indicated by black and white, respectively.

part (see Fig. 5) one blank column is inserted for isolation purposes between the standard diode (abbr. std. Diode), having no BPW between the drift rings and the diode with BPW. This blank column can be identified in the radiogram. Also, the outermost left portion of the 40 μm part (std. Diode without BPW) is not biased optimally and is, hence, overexposed in the radiogram. It appears that some pixels register a certain amount of hits even though they are covered up by the tungsten mask. These are not hot pixels, as will be explained later on. These hits will be referred to as ghost hits in the following.

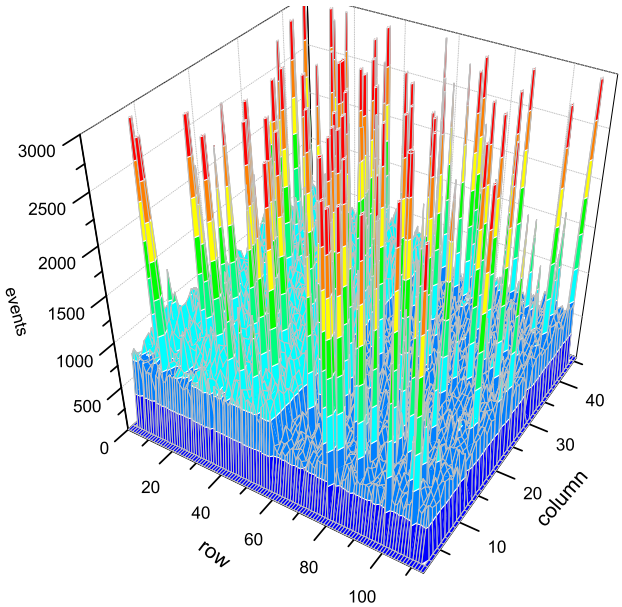

Fig. 11. Flatfield exposure of the 20 μm pixel part using ^{55}Fe operated in standard depletion with 3 V at the backside.

A flatfield (accumulated over 800 thousand frames) has been recorded without the tungsten mask, for both biasing schemes, drift and depletion. Fig. 11 shows the flatfield of the 20 μm pixel part in standard depletion with 3 V at the backside. An increased number of hits are observed in some pixels (ghost hits, here seen as spikes), as have already been noticed in the radiogram. There is also a distinct hit rate between the matrix parts that use the normal diode implantation (average around 600 hits) and that use the additional BPW implantation surrounding the p-diode (average around 800 hits). When biasing the detector in drift scheme, with the flatfield shown in Fig. 12, the difference in hit rate for BPW and normal diode disappears. The average hit per pixel increases to about 1200 hits, which is significantly higher than in the depletion scheme. This supports the fact that, in the drift scheme charge is collected from a larger volume, and hence the number of hits observed in a certain time is higher. Very pronounced is the reduction of the number of pixels that show ghost hits. The origin of the ghost hits, however, is unclear at the moment, as well as the fact that their occurrence significally decreases when using the drift biasing. The behavior of the 40 μm pixel part when biased in drift or depletion scheme is similar to that of the 20 μm version.

C. ^{55}Fe *spectrum and influence of BPW on the input capacitance*

The spectral distribution of the acquired signals is shown in Fig. 13. The spectrum shows signals from the 20 μm part that uses BPW implant. Besides signals that are originated from the iron source, a distinct peak is observed at lower energies (at about 50 mV, equivalent to approximately 500 e^-). These events are due to the ghost hits that have already been observed in the flatfields and radiogram. The ghost hit part

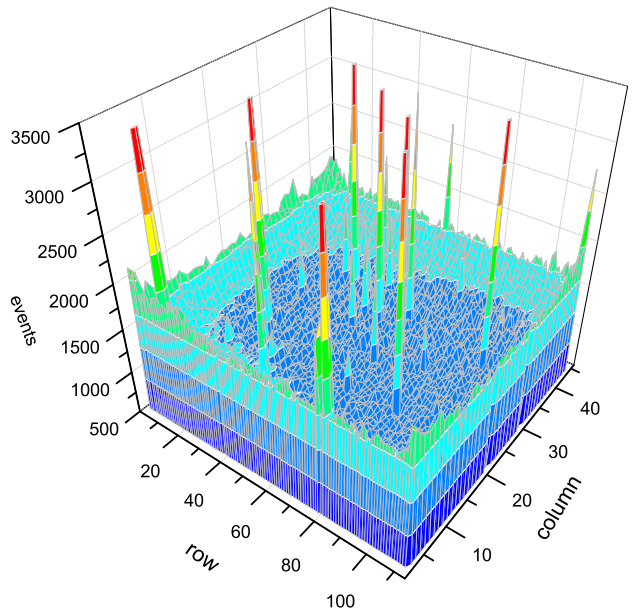

Fig. 12. Flatfield exposure of the 20 μm pixel part using ^{55}Fe operated in drift scheme with 3 V at the backside and 1.5 V at the n-rings.

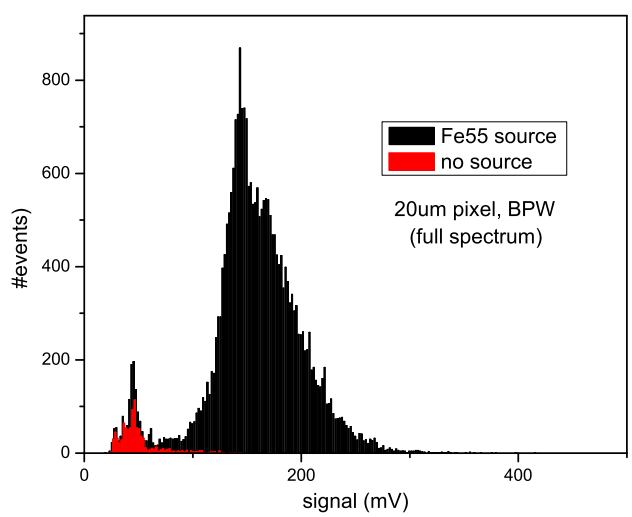

Fig. 13. Full ^{55}Fe-spectrum for the 20 μm pixel part.

of the spectrum remains if the radioactive source is removed (shown in red in Fig. 13).

The spectrum in Fig. 13 is obtained after cluster reconstruction. Clusters are reconstructed by searching for seeds and then summing over adequate neighboring pixels. Pixels are considered as seed candidates in order of their signal to noise ratio and are accepted by an 8 σ noise cut. Neighboring pixels are added to the cluster if their signal exceeds 3 times the pixel noise. The average electronic pixel noise is around 20-30 e^-.

The cluster size distribution after reconstruction is shown in Fig. 14 for the 20 μm (left) and the 40 μm (right) pixel part. For the smaller 20 μm pixel, almost no single pixel clusters

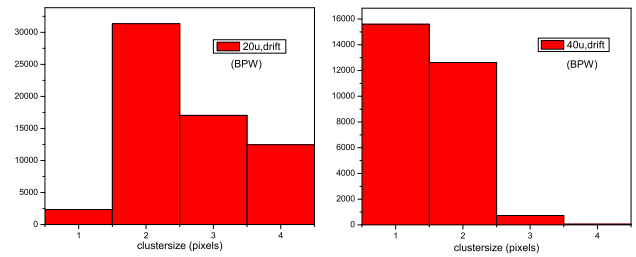

Fig. 14. Cluster size distribution for 20 μm (left) and 40 μm (right) pixels applying an 8 σ seed and 3 σ neighbor cut.

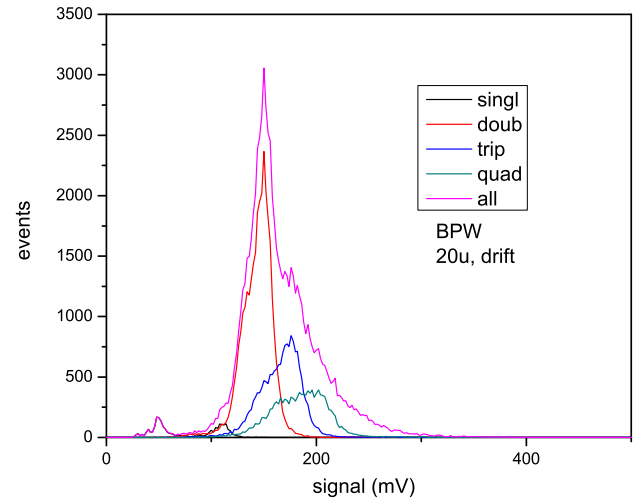

Fig. 15. ^{55}Fe-spectrum split up into contributions from different cluster sizes (1-4 pixels) as well as the full spectrum.

(singles) appear. Most likely are clusters consisting of 2 pixels (doublets), but also 3 (triplets) and 4 pixel cluster (quadruples) occur. In case of the 40 μm pixel pitch basically only singles and doublets occur, with a slight preference for singles. This observation is reasonable since charge charing for the larger pixel size is less likely.

To analyze the iron spectrum in more detail, the spectrum is split up into contributions from singles, doublets, triplets and quadruples and plotted individually in Fig. 15. An increase in peak energy is observed with cluster size. This may be interpreted as partial charge collection, which is plausible considering the weak drift field of only 1.5 V that is applied between the back and the front side. The increase in peak energy with cluster size is one reason for the iron peak in the full spectrum (all cluster sizes) being much wider than dictated by the electronic noise.

Each individual peak (for doublets, triplets and quadruples) is fitted using a Gaussian distribution. Fig. 16 shows the peak energy as a function of cluster size. The analysis is done separately for the normal and BPW diode of the 20 μm part. One observes a very similar increase of collected charge with cluster size for both diode versions. This has been discussed above. Moreover, the standard diode provides a systematically higher signal of about 21 % compared to the BPW version. This observation is reasonable since the charge gain is given

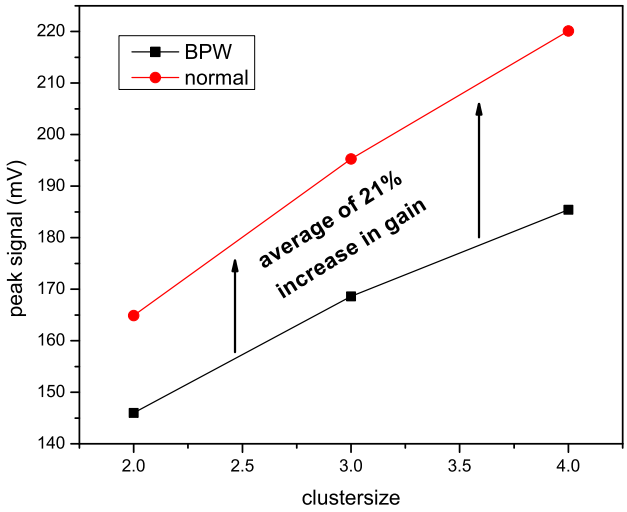

Fig. 16. Comparison of peak energy for p-diode using minimum surrounding BPW and without any BPW (normal).

by the input capacitance. The additional BPW around the p-diode increases the input capacitance and therefore decreases the gain. In general, a very low input capacitance of about 3 fF is observed. This figure includes the diode implantation itself, as well as the source follower input transistor and any parasitic routing.

IV. Conclusion and Outlook

A SOI detector using a drift biasing scheme has been proposed and has been realized using the OKI process on high resistivity substrate. The detector has been successfully operated in drift mode and tested with an ^{55}Fe radioactive source emitting 6 keV X-rays.

The achieved input capacitance of the pixel cell is about 3 fF. This is very low, and hence offers a very high charge conversion gain for detection of impinging radiation. At the same time a low electronic noise of about 20 e^- is obtained. Overall, this provides an excellent signal to noise ratio.

Due to limitations of the drift bias voltage at the moment (1-2 V), the drift scheme could not be fully explored and the first results are not fully conclusive to clearly favor the drift scheme over the standard depletion scheme. When using the current submission with a basically untreated backside, cooling beyond the current operation at room temperature should significantly reduce the leakage current and enable operation at higher drift voltages, and eventually show the full potential of the proposed scheme. This will be explored in the near future. On a longer time scale, new process options with advanced backside treatment might become available and will open new opportunities for future submissions using this concept.

Acknowledgment

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