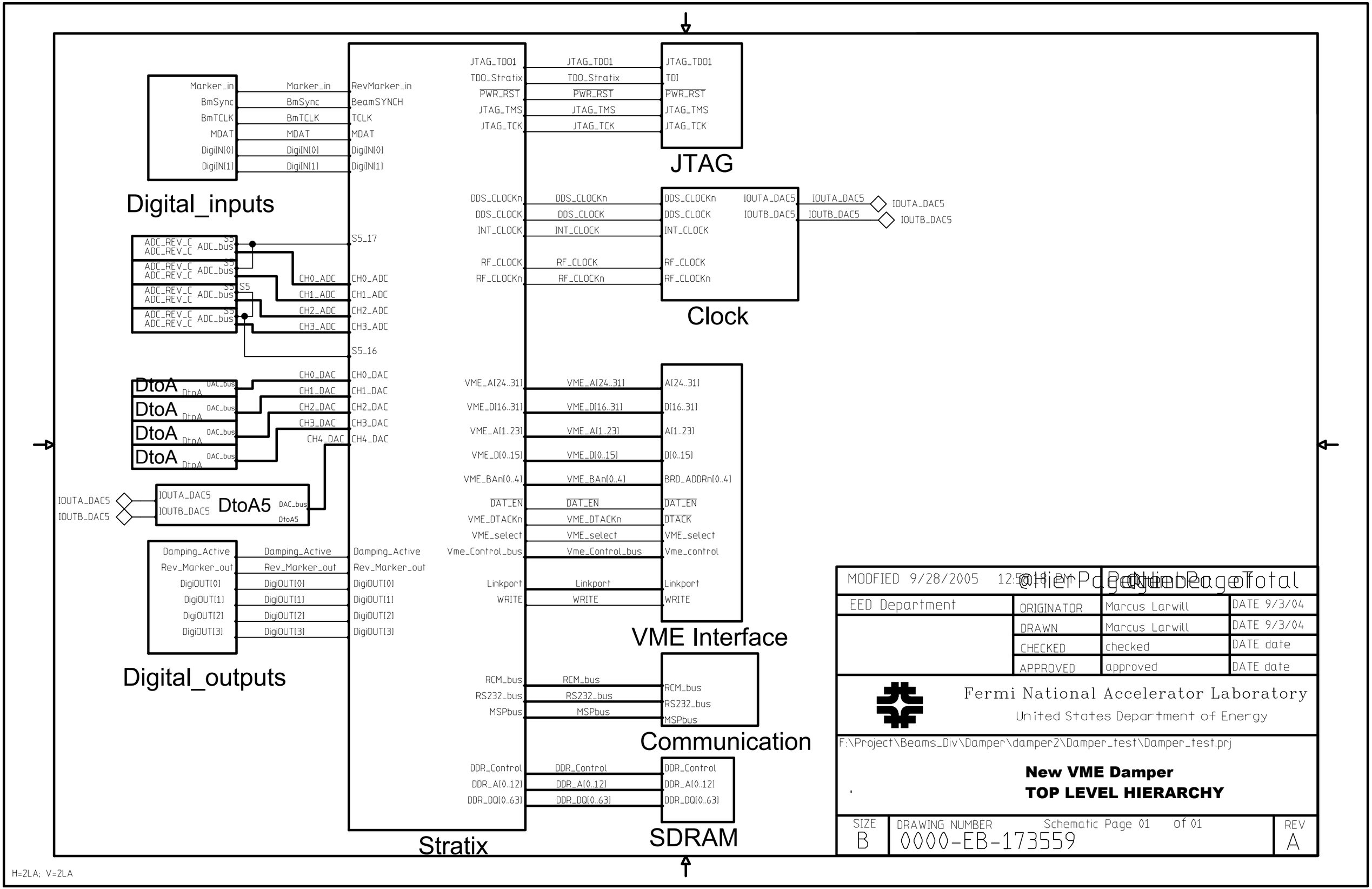

Digital_inputs
Marker_in
BmSync
BmTCLK
MDAT
DigiIN[0]
DigiIN[1]
RevMarker_in
BeamSYNCH
TCLK
S5_17
S5_16
ADC_REV_C
ADC_bus
S5
CH0_ADC
CH1_ADC
CH2_ADC
CH3_ADC
DtoA
DtoA5
DAC_bus
CH0_DAC
CH1_DAC
CH2_DAC
CH3_DAC
CH4_DAC
IOUTA_DAC5
IOUTB_DAC5
Digital_outputs
Damping_Active
Rev_Marker_out
DigiOUT[0]
DigiOUT[1]
DigiOUT[2]
DigiOUT[3]
Stratix
JTAG_TDO1
TDO_Stratix
PWR_RST
JTAG_TMS
JTAG_TCK
JTAG
TDI
DDS_CLOCKn
DDS_CLOCK
INT_CLOCK
RF_CLOCK
RF_CLOCKn
Clock
VME_A[24..31]
VME_D[16..31]
VME_A[1..23]
VME_D[0..15]
VME_BAn[0..4]
DAT_EN
VME_DTACKn
VME_select
Vme_Control_bus
Linkport
WRITE
A[24..31]
D[16..31]
A[1..23]
D[0..15]
BRD_ADDRn[0..4]
DTACK
Vme_control
VME Interface
RCM_bus
RS232_bus
MSPbus
Communication
DDR_Control
DDR_A[0..12]
DDR_DQ[0..63]
SDRAM
MODFIED 9/28/2005
EED Department
ORIGINATOR Marcus Larwill DATE 9/3/04
DRAWN Marcus Larwill DATE 9/3/04
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
F:\Project\Beams_Div\Damper\damper2\Damper_test\Damper_test.prj
New VME Damper
TOP LEVEL HIERARCHY
SIZE B
DRAWING NUMBER 0000-EB-173559
Schematic Page 01 of 01
REV A
H=2LA; V=2LA