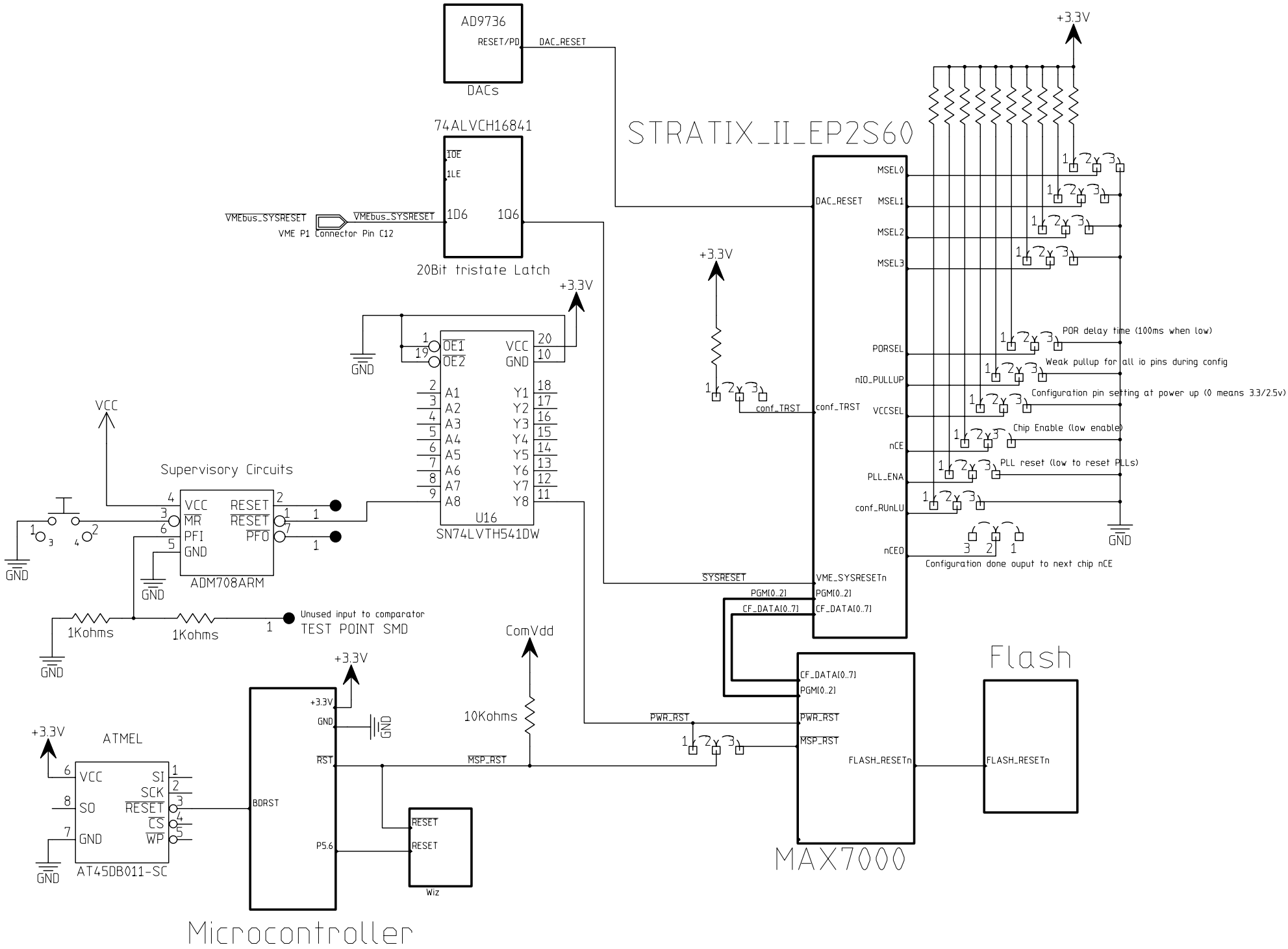
AD9736
RESET/PD
DAC_RESET
DACs
74ALVCH16841
1OE
1LE
1D6
1Q6
VMEbus_SYSRESET
VME P1 Connector Pin C12
20Bit tristate Latch
STRATIX_II_EP2S60
+3.3V
MSEL0
MSEL1
MSEL2
MSEL3
DAC_RESET
PORSEL
nIO_PULLUP
VCCSEL
nCE
PLL_ENA
conf_RUnLU
nCEO
conf_TRST
VME_SYSRESETn
PGM[0..2]
CF_DATA[0..7]
POR delay time (100ms when low)
Weak pullup for all io pins during config
Configuration pin setting at power up (0 means 3.3/2.5v)
Chip Enable (low enable)
PLL reset (low to reset PLLs)
Configuration done ouput to next chip nCE
GND
OE1
OE2
VCC
A1
A2
A3
A4
A5
A6
A7
A8
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
U16
SN74LVTH541DW
Supervisory Circuits
RESET
PFI
PFO
ADM708ARM
1Kohms
Unused input to comparator
TEST POINT SMD
ComVdd
10Kohms
SYSRESET
PWR_RST
MSP_RST
FLASH_RESETn
MAX7000
Flash
ATMEL
SI
SCK
SO
CS
WP
AT45DB011-SC
BDRST
P5.6
Wiz
Microcontroller