Output name	description	destination	U64 pin assignment	old address/data bit assignment	new address device	new format	Data String format								
ADrvG0	Squid A output gain	U76, LTC6910	PIN_1	E2/0-2	A	3 bit gain: 0-7	Phonon A								
ADrvG1	Squid A output gain		PIN_100				FeG DrvG PolS								
ADrvG2	Squid A output gain		PIN_99				xxxx x210 x210 xx10								
AFeG0	Squid A frontend gain	U75, LTC6910	PIN_98	4A/0-12		3 bit gain: 0-7									
AFeG1	Squid A frontend gain		PIN_97												
AFeG2	Squid A frontend gain		PIN_96												
APolSlct0	Squid A Polarity select	U73, ADG619	PIN_92	E1/4		feedback polarity		A0:	0: grounded	1:positive	0:neg	1:open			
APolSlct1	Squid A Polarity select	U74, ADG619	PIN_95					A1:	0	0:feedback	1:feedback	1:loop			
BDrvG0	Squid B output gain	U87, LTC6910	PIN_33	E2/4-6	B	3 bit gain: 0-7	Phonon B								
BDrvG1	Squid B output gain		PIN_34				FeG DrvG PolS								
BDrvG2	Squid B output gain		PIN_35				xxxx x210 x210 xx10								
BFeG0	Squid B frontend gain	U95, LTC6910	PIN_28	4B/0-12		3 bit gain: 0-7									
BFeG1	Squid B frontend gain		PIN_29												
BFeG2	Squid B frontend gain		PIN_30												
BPolSlct0	Squid B Polarity select	U93, ADG619	PIN_26	E1/5		feedback polarity		A0:	0: grounded	1:positive	0:neg	1:open			
BPolSlct1	Squid B Polarity select	U94, ADG619	PIN_27					A1:	0	0:feedback	1:feedback	1:loop			
CDrvG0	Squid C output gain	U38, LTC6910	PIN_72	E2/8-10	C	3 bit gain: 0-7	Phonon C								
CDrvG1	Squid C output gain		PIN_71				FeG DrvG PolS								
CDrvG2	Squid C output gain		PIN_70				xxxx x210 x210 xx10								
CFeG0	Squid C frontend gain	U36, LTC6910	PIN_69	4C/0-12		3 bit gain: 0-7									
CFeG1	Squid C frontend gain		PIN_68												
CFeG2	Squid C frontend gain		PIN_67												
CPolSlct0	Squid C Polarity select	U26, ADG619	PIN_61	E1/6		feedback polarity		A0:	0: grounded	1:positive	0:neg	1:open			
CPolSlct1	Squid C Polarity select	U35, ADG619	PIN_66					A1:	0	0:feedback	1:feedback	1:loop			
DDrvG0	Squid D output gain	U57, LTC6910	PIN_50	E2/12-14	D	3 bit gain: 0-7	Phonon D								
DDrvG1	Squid D output gain		PIN_57				FeG DrvG PolS								
DDrvG2	Squid D output gain		PIN_58				xxxx x210 x210 xx10								
DFeG0	Squid D frontend gain	U56, LTC6910	PIN_47	4D/0-12		3 bit gain: 0-7									
DFeG1	Squid D frontend gain		PIN_48												
DFeG2	Squid D frontend gain		PIN_49												
DPolSlct0	Squid D Polarity select	U55, ADG619	PIN_39	E1/7		feedback polarity		A0:	0: grounded	1:positive	0:neg	1:open			
DPolSlct1	Squid D Polarity select	U62, ADG619	PIN_42					A1:	0	0:feedback	1:feedback	1:loop			
QetABCS	QET A/B bias DAC	U97	PIN_7	1A/1B	8	16 bit serial data string	Qet Bias Phonon A & B	A0:	0	1	0	1			
QetABSDat			PIN_6		AD5555	14 bit Dac	A1/A0/D13-D0	A1:	0	0	1	1			
QetABLdDac			PIN_8		2 output	LdDac low/high transition			no output	Qet A	Qet B	Both			
QetCDCS	QET C/D bias DAC	U28	PIN_76	1C/1D	9	16 bit serial data string	Qet Bias Phonon C & D	A0:	0	1	0	1			
QetCDSDat			PIN_75		AD5555	14 bit Dac	A1/A0/D13-D0	A1:	0	0	1	1			
QetCDLdDac			PIN_77		2 output	LdDac low/high transition			no output	Qet C	Qet D	Both			
QBiasCS	FET I/O bias DAC	U103	PIN_20	70/71	7	16 bit serial data string	Q Bias Inner & Outer	A0:	0	1	0	1			
QBiasSDat			PIN_21		AD5555	14 bit Dac	A1/A0/D13-D0	A1:	0	0	1	1			
QBiasLdDac			PIN_19		2 output	LdDac low/high transition			no output	Q O	Q I	Both			
SClk	2 output DAC serial clock	U97, 28, 103	PIN_18			QetAB, QetCD, Qbias serial Clock, rising edge clock									
RS	2 output DAC reset	U97, 28, 103	PIN_44												
SqABLdDac	Squid A&B DAC	U78	PIN_2	Squid Bias A/B: 2A, 2B	E	16 bit serial data string	Cntr-Dac/A2/A1/A0/D11-D0	A0:	0	1	0	1	0	1	0	1
SqABSClk			PIN_4	Squid Lockpoint A/B: 3A, 3B	AD5328	falling edge clock		A1:	0	0	1	1	0	0	1	1
SqABSDat			PIN_5	Driver Offset A/B: 5A, 5B	8 output	12 bit Dac		A2:	0	0	0	0	1	1	1	1
SqABSync			PIN_3			LdDac falling edge			Sq A Bias	Fb A Null	Fb B Null	Sq B Bias	Lckpnt A	Lckpnt B	Voffst A	Voffst B
SqCDLdDac	Squid C&D DAC	U46	PIN_78	Squid bias C/D: 2C, 2D	F	16 bit serial data string	Cntr-Dac/A2/A1/A0/D11-D0	A0:	0	1	0	1	0	1	0	1
SqCDSClk			PIN_82	Squid Lockpoint C/D: 3C, 3D	AD5328	falling edge clock		A1:	0	0	1	1	0	0	1	1
SqCDDat			PIN_83	Driver Offset C/D: 5C, 5D	8 output	12 bit Dac		A2:	0	0	0	0	1	1	1	1
SqCDSync			PIN_81			LdDac falling edge			Sq D Bias	Sq C Bias	Lckpnt D	Lckpnt C	Fb C Null	Voffst D	Voffst C	Fb D Null
VZSClk	LED, Zap and Test sig DAC	U40	PIN_52	LED: 72	5	16 bit serial data string	A1/A0/*PD/*Ldac/D11-D0	A0:	0	1	0	1				
VZSDat			PIN_53	Zap: 73	AD5324	12 bit Dac		A1:	0	0	1	1		PD	0: off	
VZSync			PIN_51		4 output	falling edge clock			Led 1	Led 2	Zap V	Test Dac		Ldac	0: all 4	1:addressed dac only
						Dac update rising edge sync										
SrcSlctA	Source signal monitor	U86	PIN_15	E1/12	1		Signal Source	0:feedback monitoring								
SrcSlctB	Feedback/Vary Gain Amp	U85	PIN_16	E1/13			xxxD xxxC xxxB xxxA	1:Vary gain amp								
SrcSlctC		U37	PIN_73	E1/14												
SrcSlctD		U44	PIN_74	E1/15												
QETAHtEn	QET heat pulse enable	U70	PIN_88	E0/4	3		Qet Heat Enable	0: 5V Qet heat								
QETBHtEn		U70	PIN_89	E0/5			xxxD xxxC xxxB xxxA	1: Qet Bias								
QETCHtEn		U61	PIN_86	E0/6												
QETDHtEn		U61	PIN_87	E0/7												
TestEn	Connects test signal to feedback	U25	PIN_56	E1/8-11	4		Test Fet Led Led	0:closed loop, 1:open loop w/test								
FETHtEn	FET Heater	U52	PIN_38	FE			xxxT xxxF xxx2 xxx1	0: off, 1: on								
LEDEn1	LED 1 current enable	U39	PIN_54	E4/12				0: off, 1: on								
LEDEn2	LED 2 current enable	U48	PIN_55	E4/13				0: off, 1: on								
ZapEnA	Zap enable controls	U84	PIN_90	E0/12	2		Zap	0: Zap squid								
ZapEnB		U84	PIN_91	E0/13			xxxD xxxC xxxB xxxA	1: Normal Squid op								
ZapEnC		U43	PIN_84	E0/14												
ZapEnD		U43	PIN_85	E0/15												
PwrRst	chip set up inputs	U12	PIN_62													
SetUpClk		U49	PIN_64													
SetUpDat		U65	PIN_40													
SetUpRtn		U58	PIN_41													