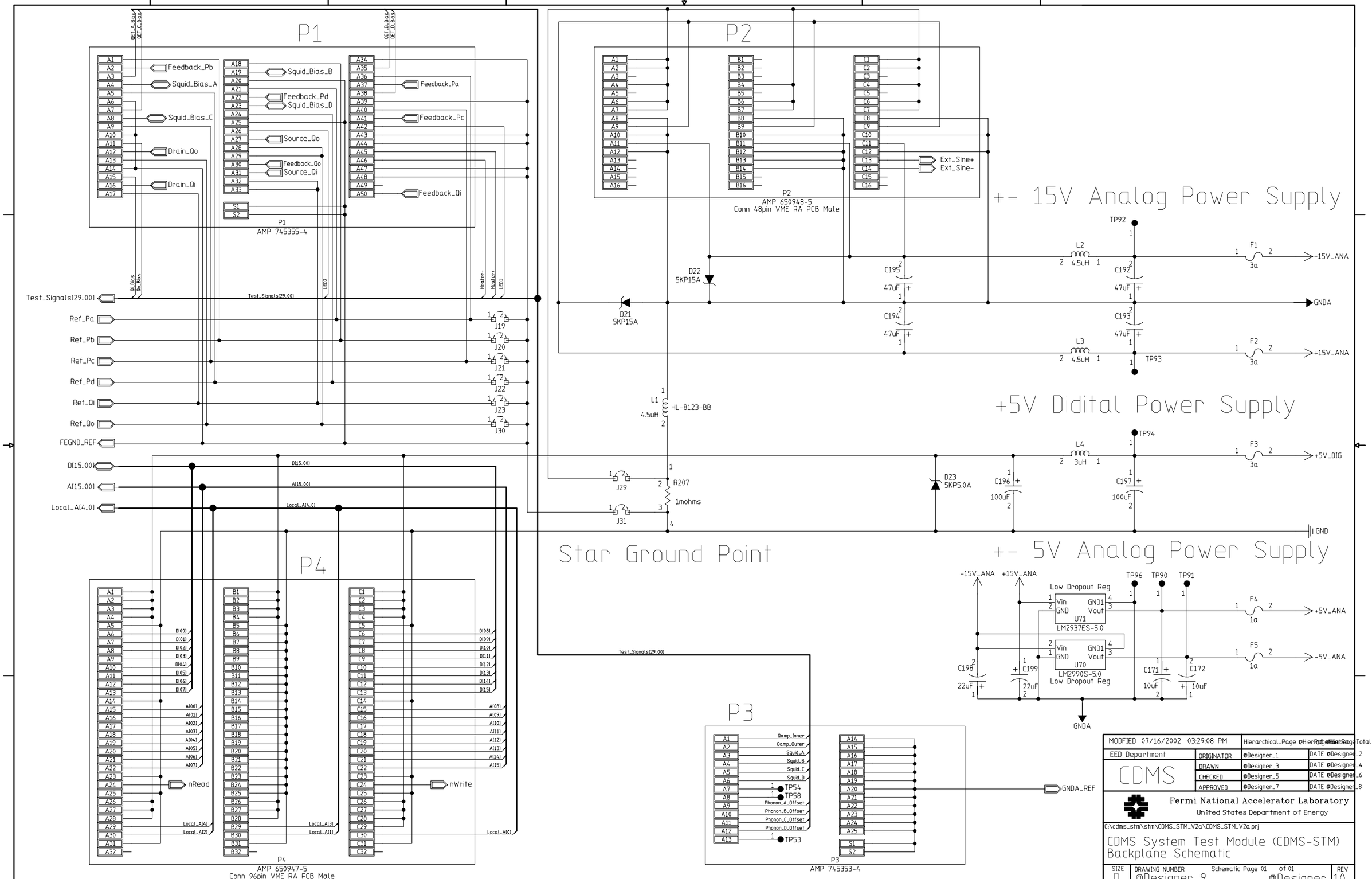
P1
P1
AMP 745355-4
Feedback_Pb
Squid_Bias_A
Squid_Bias_C
Drain_Qo
Drain_Qi
Squid_Bias_B
Feedback_Pd
Squid_Bias_D
Source_Qo
Feedback_Qo
Source_Qi
Feedback_Pa
Feedback_Pc
Feedback_Qi
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Ref_Pb
Ref_Pc
Ref_Pd
Ref_Qi
Ref_Qo
FEGND_REF
D[15..00]
A[15..00]
Local_A[4..0]
P2
P2
AMP 650948-5
Conn 48pin VME RA PCB Male
Ext_Sine+
Ext_Sine-
+- 15V Analog Power Supply
D22
5KP15A
D21
5KP15A
C195
C194
C192
C193
L2
4.5uH
L3
4.5uH
F1
3a
F2
3a
TP92
TP93
-15V_ANA
GNDA
+15V_ANA
+5V Didital Power Supply
L1
HL-8123-BB
R207
1mohms
J29
J31
L4
3uH
F3
3a
TP94
+5V_DIG
D23
5KP5.0A
C196
100uF
C197
100uF
GND
Star Ground Point
+- 5V Analog Power Supply
-15V_ANA
+15V_ANA
Low Dropout Reg
U71
LM2937ES-5.0
U70
LM2990S-5.0
Low Dropout Reg
TP96
TP90
TP91
F4
1a
F5
1a
+5V_ANA
-5V_ANA
C198
22uF
C199
22uF
C171
10uF
C172
10uF
GNDA
P4
P4
AMP 650947-5
Conn 96pin VME RA PCB Male
nRead
nWrite
P3
P3
AMP 745353-4
Qamp_Inner
Qamp_Outer
Squid_A
Squid_B
Squid_C
Squid_D
TP54
TP58
Phonon_A_Offset
Phonon_B_Offset
Phonon_C_Offset
Phonon_D_Offset
TP53
GNDA_REF
MODFIED 07/16/2002 03:29:08 PM
EED Department
CDMS
ORIGINATOR @Designer_1
DRAWN @Designer_3
CHECKED @Designer_5
APPROVED @Designer_7
DATE @Designer_2
DATE @Designer_4
DATE @Designer_6
DATE @Designer_8
Fermi National Accelerator Laboratory
United States Department of Energy
C:\cdms_stm\stm\CDMS_STM_V2a\CDMS_STM_V2a.prj
CDMS System Test Module (CDMS-STM)
Backplane Schematic
SIZE D
DRAWING NUMBER @Designer_9
Schematic Page 01 of 01
REV @Designer_10