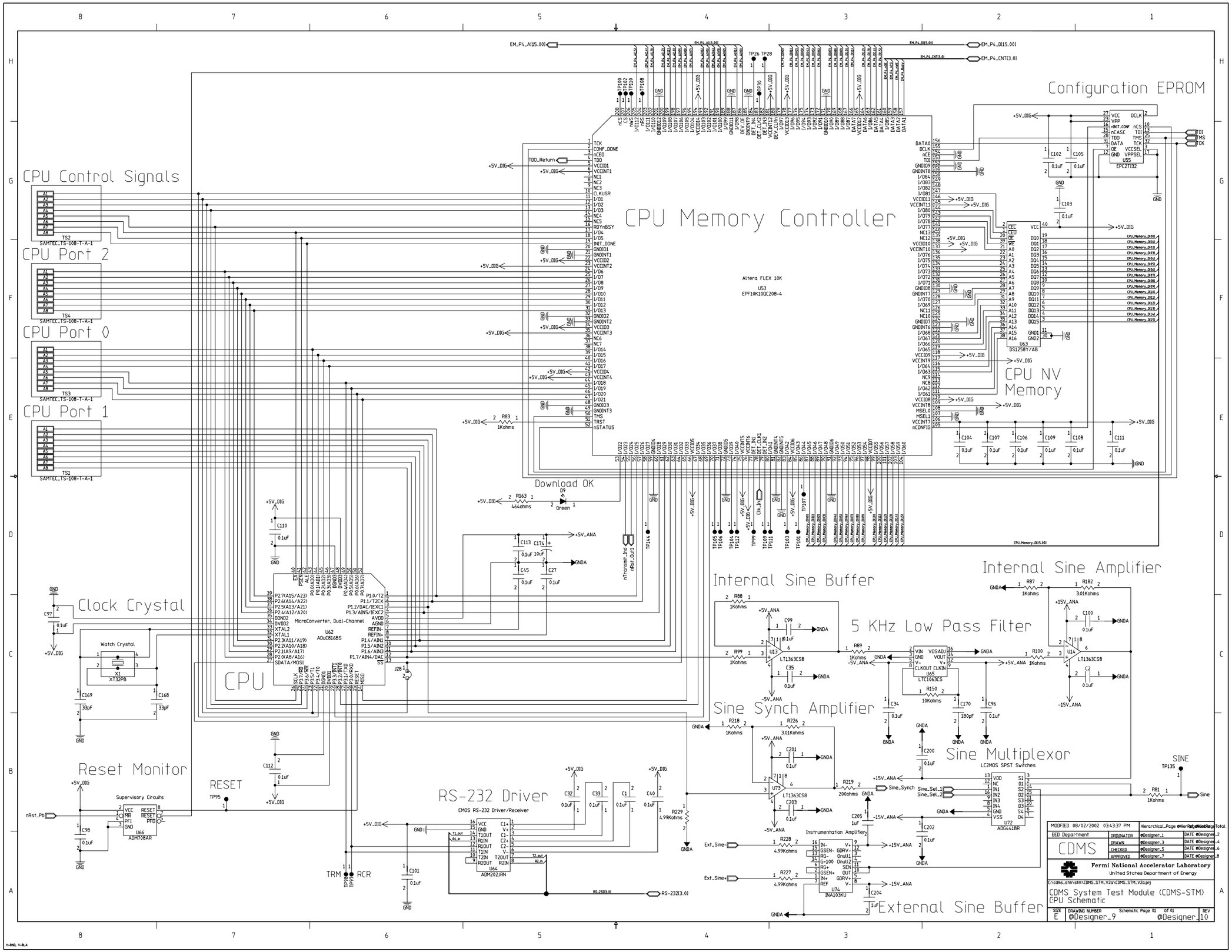
CPU Control Signals
CPU Port 2
CPU Port 0
CPU Port 1
CPU Memory Controller
Altera FLEX 10K
U53
EPF10K10QC208-4
Configuration EPROM
U55
EPC2TI32
CPU NV Memory
U63
DS1258Y/AB
Download OK
Clock Crystal
Watch Crystal
CPU
U62
ADuC816BS
MicroConverter, Dual-Channel
Reset Monitor
Supervisory Circuits
U66
ADM708AR
RESET
RS-232 Driver
CMOS RS-232 Driver/Receiver
U64
ADM202JRN
Internal Sine Buffer
Sine Synch Amplifier
5 KHz Low Pass Filter
U65
LTC1063CS
Internal Sine Amplifier
Sine Multiplexor
LC2MOS SPST Switches
U72
AD7441BR
Instrumentation Amplifier
U74
INA103KU
External Sine Buffer
SINE
MODIFIED 08/02/2002 03:43:37 PM
EED Department
CDMS
Fermi National Accelerator Laboratory
United States Department of Energy
CDMS System Test Module (CDMS-STM)
CPU Schematic
DRAWING NUMBER
@Designer_9
@Designer_10