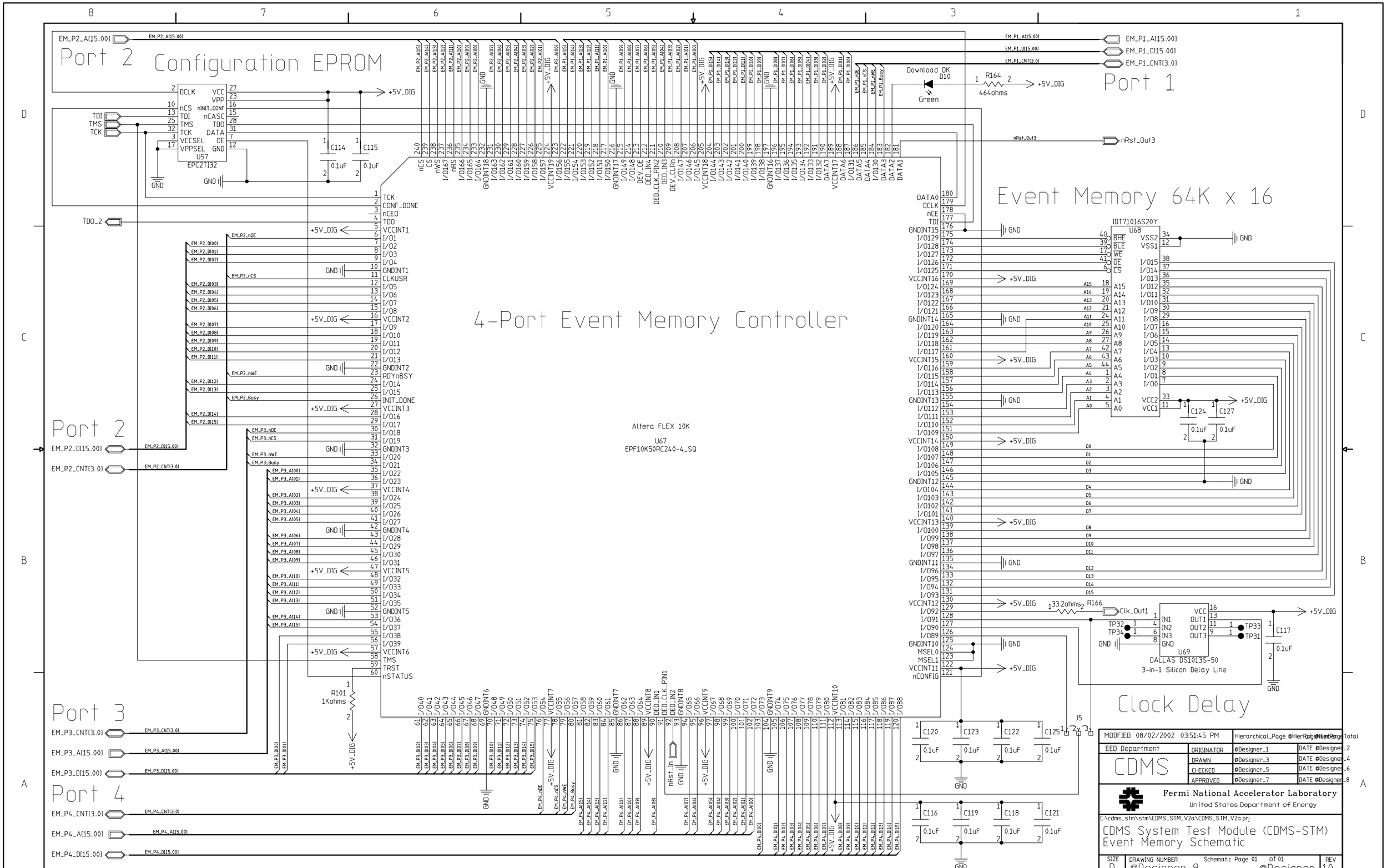
Port 2
Configuration EPROM
U57
EPC2TI32
Port 1
Download OK
D10
Green
R164
464ohms
Event Memory 64K x 16
IDT71016S20Y
U68
4-Port Event Memory Controller
Altera FLEX 10K
U67
EPF10K50RC240-4_SQ
Port 2
Port 3
Port 4
R101
1Kohms
Clock Delay
R166
33.2ohms
U69
DALLAS DS1013S-50
3-in-1 Silicon Delay Line
MODIFIED 08/02/2002 03:51:45 PM
EED Department
CDMS
Fermi National Accelerator Laboratory
United States Department of Energy
C:\cdms_stm\stm\CDMS_STM_V2a\CDMS_STM_V2a.prj
CDMS System Test Module (CDMS-STM)
Event Memory Schematic
SIZE D
DRAWING NUMBER @Designer_9
Schematic Page 01 of 01
REV @Designer_10