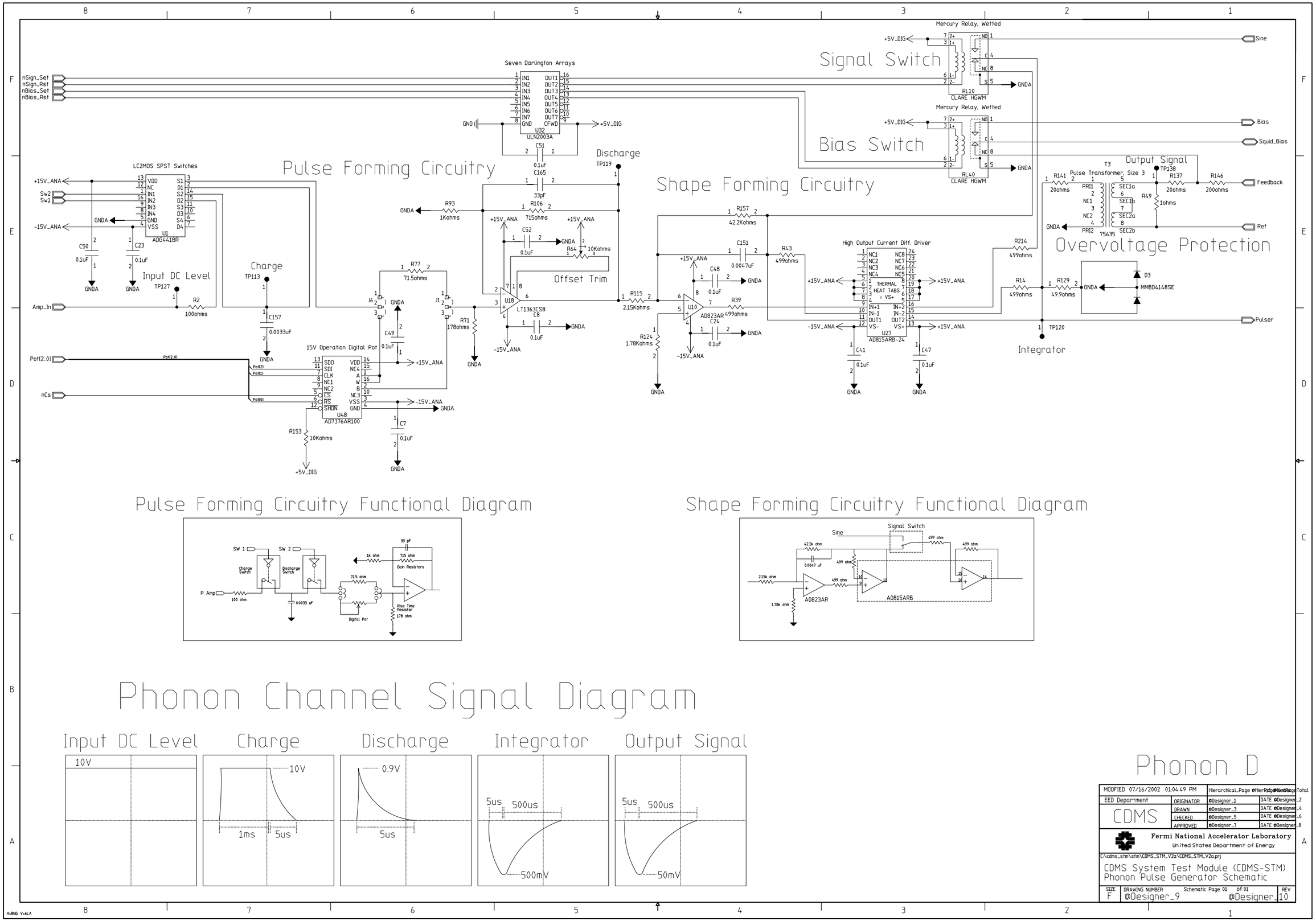
Pulse Forming Circuitry
Shape Forming Circuitry
Signal Switch
Bias Switch
Overvoltage Protection
Mercury Relay, Wetted
Seven Darlington Arrays
LC2MOS SPST Switches
Input DC Level
Charge
Discharge
Offset Trim
15V Operation Digital Pot
High Output Current Diff. Driver
Output Signal
Integrator
Pulse Transformer, Size 3
Sine
Bias
Squid_Bias
Feedback
Ref
Pulser
nSign_Set
nSign_Rst
nBias_Set
nBias_Rst
Amp_In
Pot[2..0]
nCs
Pulse Forming Circuitry Functional Diagram
Shape Forming Circuitry Functional Diagram
Phonon Channel Signal Diagram
Input DC Level
Charge
Discharge
Integrator
Output Signal
10V
1ms
5us
0.9V
500us
500mV
50mV
Phonon D
MODIFIED 07/16/2002 01:04:49 PM
EED Department
CDMS
ORIGINATOR
DRAWN
CHECKED
APPROVED
Fermi National Accelerator Laboratory
United States Department of Energy
C:\cdms_stm\stm\CDMS_STM_V2a\CDMS_STM_V2a.prj
CDMS System Test Module (CDMS-STM)
Phonon Pulse Generator Schematic
SIZE F
DRAWING NUMBER @Designer_9
Schematic Page 01 of 01
REV 10