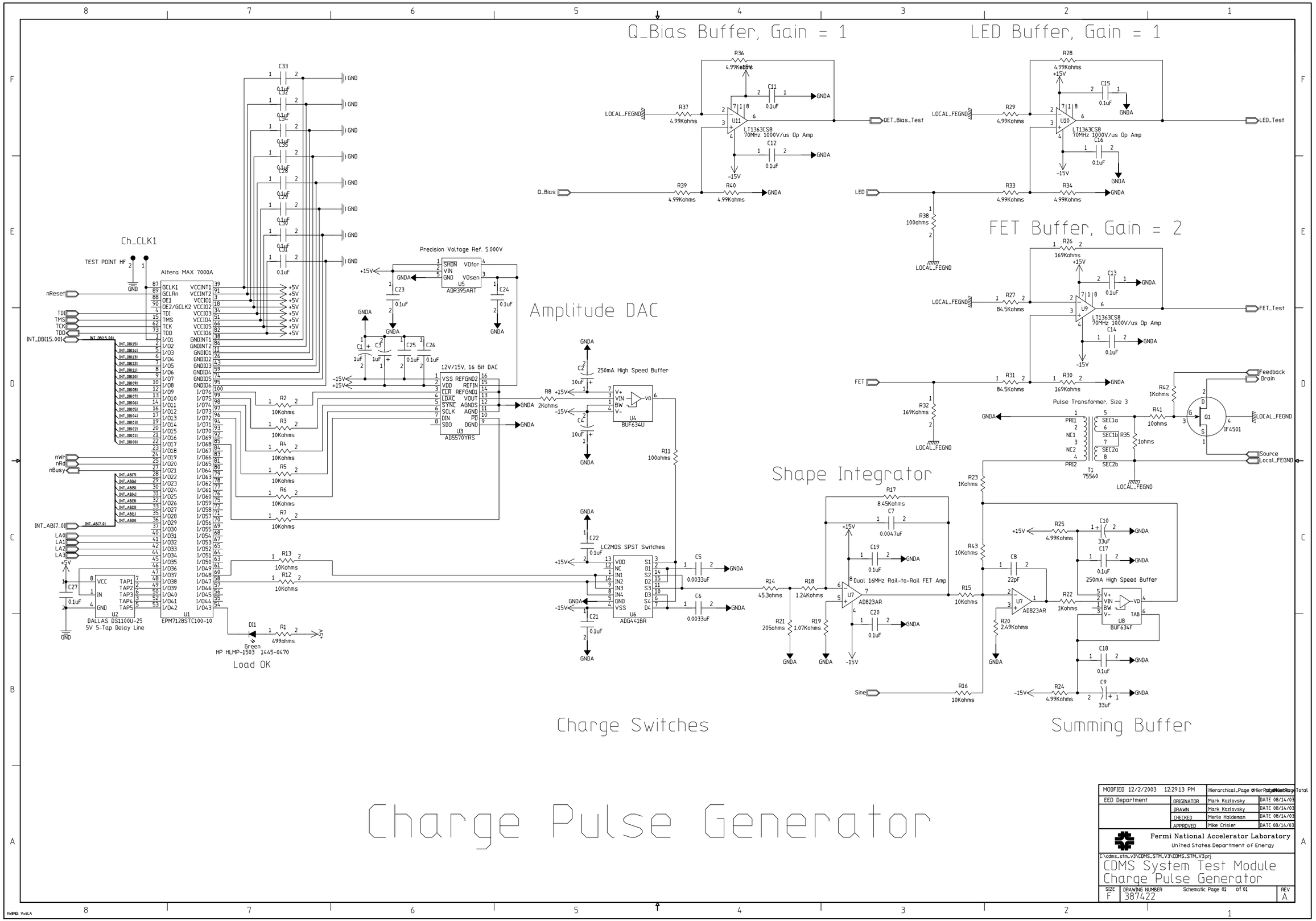
Q_Bias Buffer, Gain = 1
LED Buffer, Gain = 1
FET Buffer, Gain = 2
Amplitude DAC
Shape Integrator
Charge Switches
Summing Buffer
Ch_CLK1
Load OK
Charge Pulse Generator
Altera MAX 7000A
Precision Voltage Ref. 5.000V
12V/15V, 16 Bit DAC
250mA High Speed Buffer
LC2MOS SPST Switches
Dual 16MHz Rail-to-Rail FET Amp
Pulse Transformer, Size 3
LT1363CS8
70MHz 1000V/us Op Amp
MODIFIED 12/2/2003 12:29:13 PM
EED Department
ORIGINATOR Mark Kozlovsky DATE 08/14/03
DRAWN Mark Kozlovsky DATE 08/14/03
CHECKED Merle Haldeman DATE 08/14/03
APPROVED Mike Crisler DATE 08/14/03
Fermi National Accelerator Laboratory
United States Department of Energy
C:\cdms_stm_v3\CDMS_STM_V3\CDMS_STM_V3.prj
CDMS System Test Module
Charge Pulse Generator
SIZE F
DRAWING NUMBER 387422
Schematic Page 01 of 01
REV A