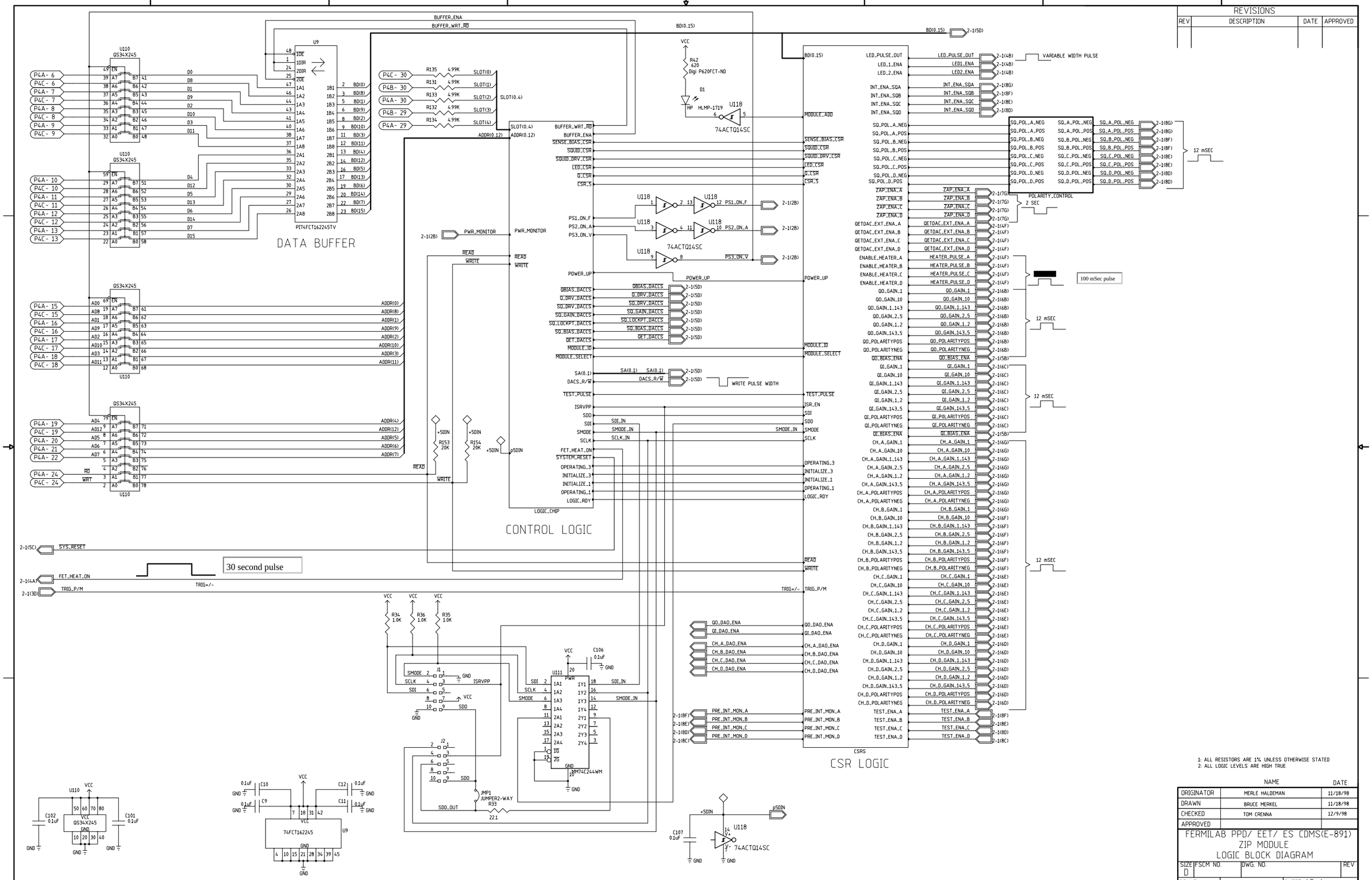
DATA BUFFER
CONTROL LOGIC
CSR LOGIC
30 second pulse
100 mSec pulse
VARIABLE WIDTH PULSE
WRITE PULSE WIDTH
POLARITY_CONTROL
2 SEC
12 mSEC
1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
NAME
DATE
ORIGINATOR
MERLE HALDEMAN
11/18/98
DRAWN
BRUCE MERKEL
11/18/98
CHECKED
TOM CRENNA
12/9/98
APPROVED
FERMILAB PPD/ EET/ ES CDMS(E-891)
ZIP MODULE
LOGIC BLOCK DIAGRAM
SIZE
D
FSCM NO.
DWG. NO.
REV
SCALE
SHEET 13-1