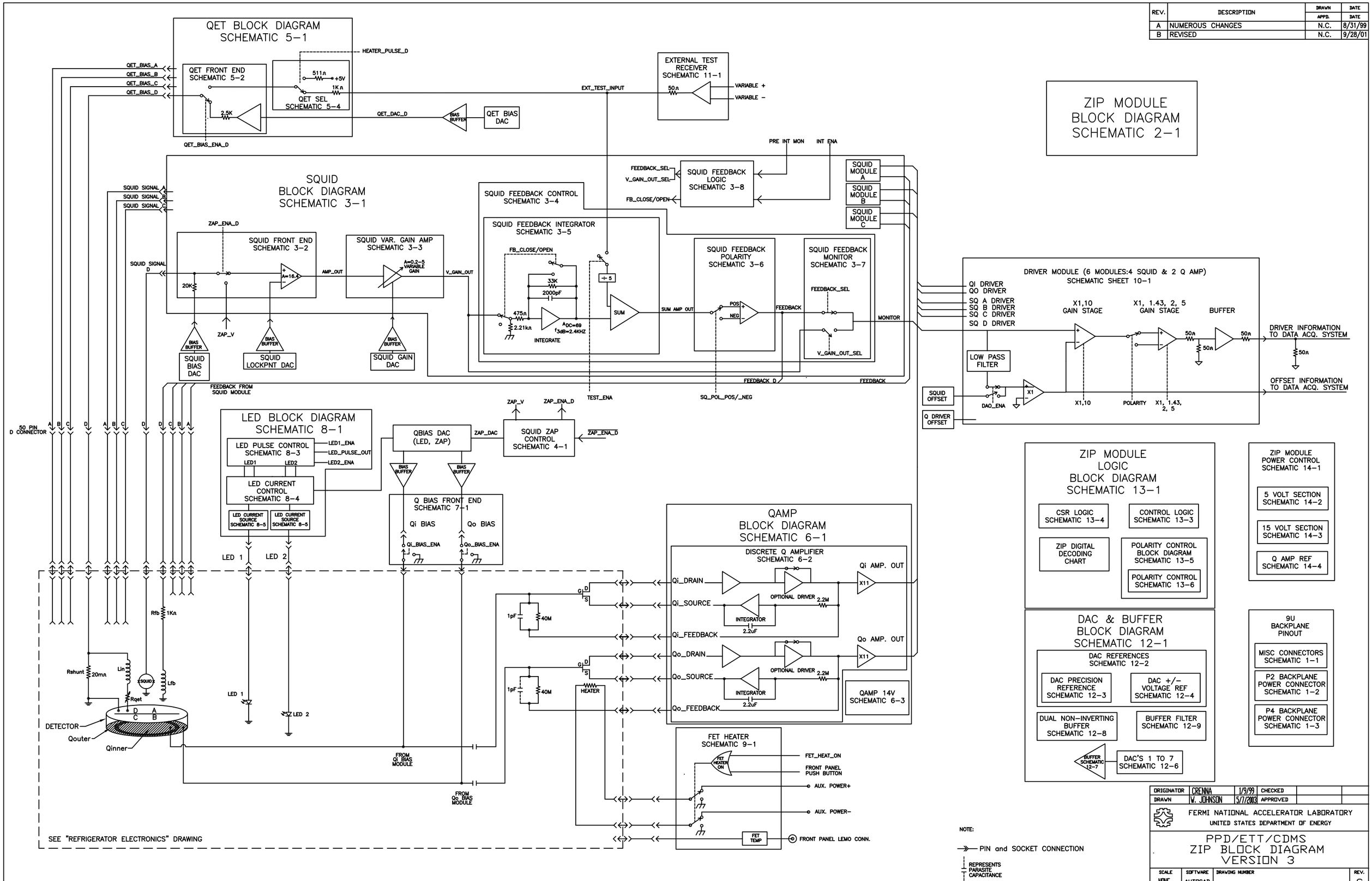
REV.	DESCRIPTION	DRAWN / APPD.	DATE / DATE
A	NUMEROUS CHANGES	N.C.	8/31/99
B	REVISED	N.C.	9/28/01



ORIGINATOR	CRENNA	1/9/99	CHECKED
DRAWN	W. JOHNSON	5/7/2003	APPROVED

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

PPD/ETT/CDMS
ZIP BLOCK DIAGRAM
VERSION 3

SCALE	SOFTWARE	DRAWING NUMBER	REV.
NONE	AUTOCAD		C

PART 1: SECTION, SUBSECTION DECODING

SECTION DAC/CSR name	SUBSECTION DAC/CSR	SUBSECTION NAME	section/subsection address	section decoding
Module Info	ID		xx00	zip logic
section 0	RESET		xx0F	zip logic
QET DAC	DAC 0	Sensor Bias A	xx1A	zip logic
section 1	DAC 1	Sensor Bias B	xx1B	zip logic
	DAC 2	Sensor Bias C	xx1C	zip logic
	DAC 3	Sensor Bias D	xx1D	zip logic
Squid Bias DAC	DAC 0	Squid Bias A	xx2A	zip logic
section 2	DAC 1	Squid Bias B	xx2B	zip logic
	DAC 2	Squid Bias C	xx2C	zip logic
	DAC 3	Squid Bias D	xx2D	zip logic
Squid Lock DAC	DAC 0	Squid Lock A	xx3A	zip logic
section 3	DAC 1	Squid Lock B	xx3B	zip logic
	DAC 2	Squid Lock C	xx3C	zip logic
	DAC 3	Squid Lock D	xx3D	zip logic
Squid Gain DAC	DAC 0	Squid Gain A	xx4A	zip logic
section 4	DAC 1	Squid Gain B	xx4B	zip logic
	DAC 2	Squid Gain C	xx4C	zip logic
	DAC 3	Squid Gain D	xx4D	zip logic
Squid Driver DAC	DAC 0	Squid Driver A	xx5A	zip logic
section 5	DAC 1	Squid Driver B	xx5B	zip logic
	DAC 2	Squid Driver C	xx5C	zip logic
	DAC 3	Squid Driver D	xx5D	zip logic
Q Driver DAC	DAC 0	Q O Driver	xx60	zip logic
section 6	DAC 1	Q I Driver	xx61	zip logic
	DAC 2	Test Voltage	xx62	zip logic
	DAC 3			zip logic
Q Bias DAC	DAC 0	Q O Bias	xx70	zip logic
section 7	DAC 1	Q I Bias	xx71	zip logic
	DAC 2	LED Bias	xx72	zip logic
	DAC 3	Zap Voltage	xx73	zip logic
unused section 8 to D				
CSR	CSR0	Sense Bias CSR	xxE0	zip logic
section E	CSR1	Squid CSR	xxE1	zip logic
	CSR2	Squid Driver CSR	xxE2	zip logic
	CSR3	LED CSR	xxE3	zip logic
	CSR4	Q CSR	xxE4	zip logic
	CSR5	CSR5	xxE5	zip logic
Test		Test Pulse	xxFF	zip logic
section F		FET Heater	xxFE	zip logic
The Module is decoded from bits 8 to12 of the address bus	The SECTIONS are decoded from bits 4 to 7 of the address bus	The SUBSECTIONS are decoded from bits 0 to 3 of the address bus		Outputs are from logic #1: zip_logic3.vhd

PART 2: CSR SUBSECTION OUTPUTS vs DATA BUSS BITS

Data Bit	SENSE BIAS CSR	Squid CSR	Squid Driver CSR	LED CSR	Q CSR	CSR5	Module ID	Data Bit
BD0	***QET_DAC_EXT_A***	***EXT_INT_SQ_A***	**CHA_GAIN0**	WIDTH_0	***Q_O_GAIN0***	TRIG_ENA	Serial Number bit 0	BD0
BD1	***QET_DAC_EXT_B***	***EXT_INT_SQ_B***	**CHA_GAIN1**	WIDTH_1	***Q_O_GAIN1***		Serial Number bit 1	BD1
BD2	***QET_DAC_EXT_C***	***EXT_INT_SQ_C***	**CHA_GAIN2**	WIDTH_2	***Q_O_GAIN2***		Serial Number bit 2	BD2
BD3	***QET_DAC_EXT_D***	***EXT_INT_SQ_D***	**CHA_POLARITY**	WIDTH_3	***Q_O_POLARITY***		Serial Number bit 3	BD3
BD4	***QET_ENA_HEAT_A***	***SQ_POL_A_-***	**CHB_GAIN0**	WIDTH_4	***Q_I_GAIN0***	CH_A_DAO_ENA	Serial Number bit 4	BD4
BD5	***QET_ENA_HEAT_B***	***SQ_POL_B_-***	**CHB_GAIN1**	WIDTH_5	***Q_I_GAIN1***	CH_B_DAO_ENA	Serial Number bit 5	BD5
BD6	***QET_ENA_HEAT_C***	***SQ_POL_C_-***	**CHB_GAIN2**	WIDTH_6	***Q_I_GAIN2***	CH_C_DAO_ENA	Serial Number bit 6	BD6
BD7	***QET_ENA_HEAT_D***	***SQ_POL_D_-***	**CHB_POLARITY**	WIDTH_7	***Q_I_POLARITY***	CH_D_DAO_ENA	Serial Number bit 7	BD7
BD8		TEST_ENA_A	**CHC_GAIN0**	RATE_0	Q_O_ENA		Board Version bit 0	BD8
BD9		TEST_ENA_B	**CHC_GAIN1**	RATE_1	Q_I_ENA		Board Version bit 1	BD9
BD10		TEST_ENA_C	**CHC_GAIN2**	RATE_2	Q_O_DAO_ENA		Board Version bit 2	BD10
BD11		TEST_ENA_D	**CHC_POLARITY**	RATE_3	Q_I_DAO_ENA		Board Version bit 3	BD11
BD12	***ZAP_ENA_A***	PRE_INT_MON_A	**CHD_GAIN0**	RATE_4	LED_1_ENA		Board Type bit 0	BD12
BD13	***ZAP_ENA_B***	PRE_INT_MON_B	**CHD_GAIN1**	RATE_5	LED_2_ENA		Board Type bit 1	BD13
BD14	***ZAP_ENA_C***	PRE_INT_MON_C	**CHD_GAIN2**	RATE_6	LED_CTRL_0		Board Type bit 2	BD14
BD15	***ZAP_ENA_D***	PRE_INT_MON_D	**CHD_POLARITY**	RATE_7	LED_CTRL_1		Board Type bit 3	BD15
	Register outputs that are PLAIN text are outputs of the latching register: logic #2: csr_logic3.vhd		**Register outputs that are BOLD text are outputs that are pulses from logic #3: ziprelay2.vhd**		***Register outputs that are bold and italized text are outputs that are pulses from logic #4: chargeamps.vhd***		Module Info ID bits are read only. These are shorts to +VCC or GND to set the condition	

PART 3: GAIN AND POLARITY DECODING MATRIZ

POLARITY	2	1	0	GAIN
0	0	0	0	1
0	0	0	1	1.43
0	0	1	0	2
0	0	1	1	5
0	1	0	0	10
0	1	0	1	14.3
0	1	1	0	20
0	1	1	1	50
1	0	0	0	-1
1	0	0	1	-1.43
1	0	1	0	-2
1	0	1	1	-5
1	1	0	0	-10
1	1	0	1	-14.3
1	1	1	0	-20
1	1	1	1	-50

Data bits to the DACs set the output voltage level

DAC output voltage calculation:
Vout=Vrefl +((Vrefh-Vrefl) * N)/4096
N= is digital code in decimal

NOTE:
ALL SIGNAL NAMES ARE HIGH TRUE

LED_CTRL_1	LED_CTRL_0	
0	0	OFF
0	1	SINGLE
1	0	MULTI
1	1	ON

PART 5: Module Address decode vs. slot number

Address	Slot Number

PART 4: CHIPS AND DECODED OUTPUTS TO ZIP BOARD CIRCUITS

These are the names of the chips, the project name that the code is found in

xxx0 0000 xxxx xxxx	00xx	0
xxx0 0001 xxxx xxxx	01xx	1
xxx0 0010 xxxx xxxx	02xx	2
xxx0 0011 xxxx xxxx	03xx	3
xxx0 0100 xxxx xxxx	04xx	4
xxx0 0101 xxxx xxxx	05xx	5
xxx0 0110 xxxx xxxx	06xx	6
xxx0 0111 xxxx xxxx	07xx	7
xxx0 1000 xxxx xxxx	08xx	8
xxx0 1001 xxxx xxxx	09xx	9
xxx0 1010 xxxx xxxx	0Axx	10
xxx0 1011 xxxx xxxx	0Bxx	11
xxx0 1100 xxxx xxxx	0Cxx	12
xxx0 1101 xxxx xxxx	0Dxx	13
xxx0 1110 xxxx xxxx	0Exx	14
xxx0 1111 xxxx xxxx	0Fxx	15
xxx1 0000 xxxx xxxx	10xx	16
xxx1 0001 xxxx xxxx	11xx	17
xxx1 0010 xxxx xxxx	12xx	18
xxx1 0011 xxxx xxxx	13xx	19
xxx1 0100 xxxx xxxx	14xx	20
xxx1 0101 xxxx xxxx	15xx	21

and the outputs by name that they decode for the ZIP board

project name:chargeamps	project name: zipchips	project name:ziprelay2	project name: addrlogic
CHARGEAMP_V2	**CSR_LOGIC3_V2**	ZIPRELAY2	**ZIP_LOGIC3**
qo_gain_1	q_o_ena	chA_gain_1	module_id
qo_gain_10	q_i_ena	chA_gain_10	qet_daccs
qo_gain_1_143	led_1_ena	chA_gain_1_143	sq_bias_daccs
qo_gain_2_5	led_2_ena	chA_gain_2_5	sq_lockpt_daccs
qo_gain_1_2	ext_int_sq_A	chA_gain_1_2	sq_gain_daccs
qo_gain_143_5	ext_int_sq_B	chA_gain_143_5	sq_drv_daccs
qo_pol_pos	ext_int_sq_C	chA_pol_pos	q_drv_daccs
qo_pol_neg	ext_int_sq_D	chA_pol_neg	qbias_daccs
qi_gain_1	test_ena_A	chB_gain_1	sense_bias_csr
qi_gain_10	test_ena_B	chB_gain_10	squid_csr
qi_gain_1_143	test_ena_C	chB_gain_1_143	squid_drv_csr
qi_gain_2_5	test_ena_D	chB_gain_2_5	led_csr
qi_gain_1_2	pre_int_mon_A	chB_gain_1_2	q_csr
qi_gain_143_5	pre_int_mon_B	chB_gain_143_5	csr5
qi_pol_pos	pre_int_mon_C	chB_pol_pos	dacs_r_w
qi_pol_neg	pre_int_mon_D	chB_pol_neg	chipselect_cntrl_logic
zap_ena_A	trig_ena	chC_gain_1	test_pulse
zap_ena_B	led_pulse_out	chC_gain_10	buffer_ena
zap_ena_C	clock2ena	chC_gain_1_143	buffer_wrt_rd
zap_ena_D	chipselect	chC_gain_2_5	module_select
ena_heat_A	ch_A_dao_ena	chC_gain_1_2	subdac(0)
ena_heat_B	ch_B_dao_ena	chC_gain_143_5	subdac(1)
ena_heat_C	ch_C_dao_ena	chC_pol_pos	clock_ena
ena_heat_D	ch_D_dao_ena	chC_pol_neg	power_up
sq_pol_A_pos	qo_dao_ena	chD_gain_1	fet_heat_on
sq_pol_A_neg	qi_dao_ena	chD_gain_10	system_reset
sq_pol_B_pos	logic_rdy	chD_gain_1_143	ps1_on_f
sq_pol_B_neg		chD_gain_2_5	ps2_on_a
sq_pol_C_pos	READ ONLY INFO	chD_gain_1_2	ps3_on_v
sq_pol_C_neg	moduleconfig(0-15)	chD_gain_143_5	
sq_pol_D_pos		chD_pol_pos	
sq_pol_D_neg		chD_pol_neg	
qetdac_ext_A		module_addr	
qetdac_ext_B		clockena	
qetdac_ext_C		chipselect	
qetdac_ext_D			
clock3ena			
chipselect			
	CONTROL INPUTS FROM ZIP_LOGIC		
sense_bias_csr	sense_bias_csr	squid_driver_csr	
squid_csr	squid_csr	module_select	
q_csr	q_csr		
	csr5		
	led_csr		
	moduleid		
testpulse	test_pulse		
	CONTROL INPUTS FROM CSR_LOGIC3		
trig_ena			
	CONTROL INPUTS FROM OTHER SOURCES		
read	read	read	read
write	write	write	write
logic_rdy	logic_rdy	logic_rdy	slot(4 downto 0)
power_up	power_up	power_up	addr(15 downto 0)
trigplus_minus	trigplus_minus		clock
clock3_1KHZ	clock_100KHZ	clock_1KHZ	pwr_monitor
bd(0-15)	bd(0-15)	bd(0-15)	pwr_supervisor

ZIP MODULE ADDRESSING

UNUSED			Subrack SLOT					SECTION				SUBSECTION			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

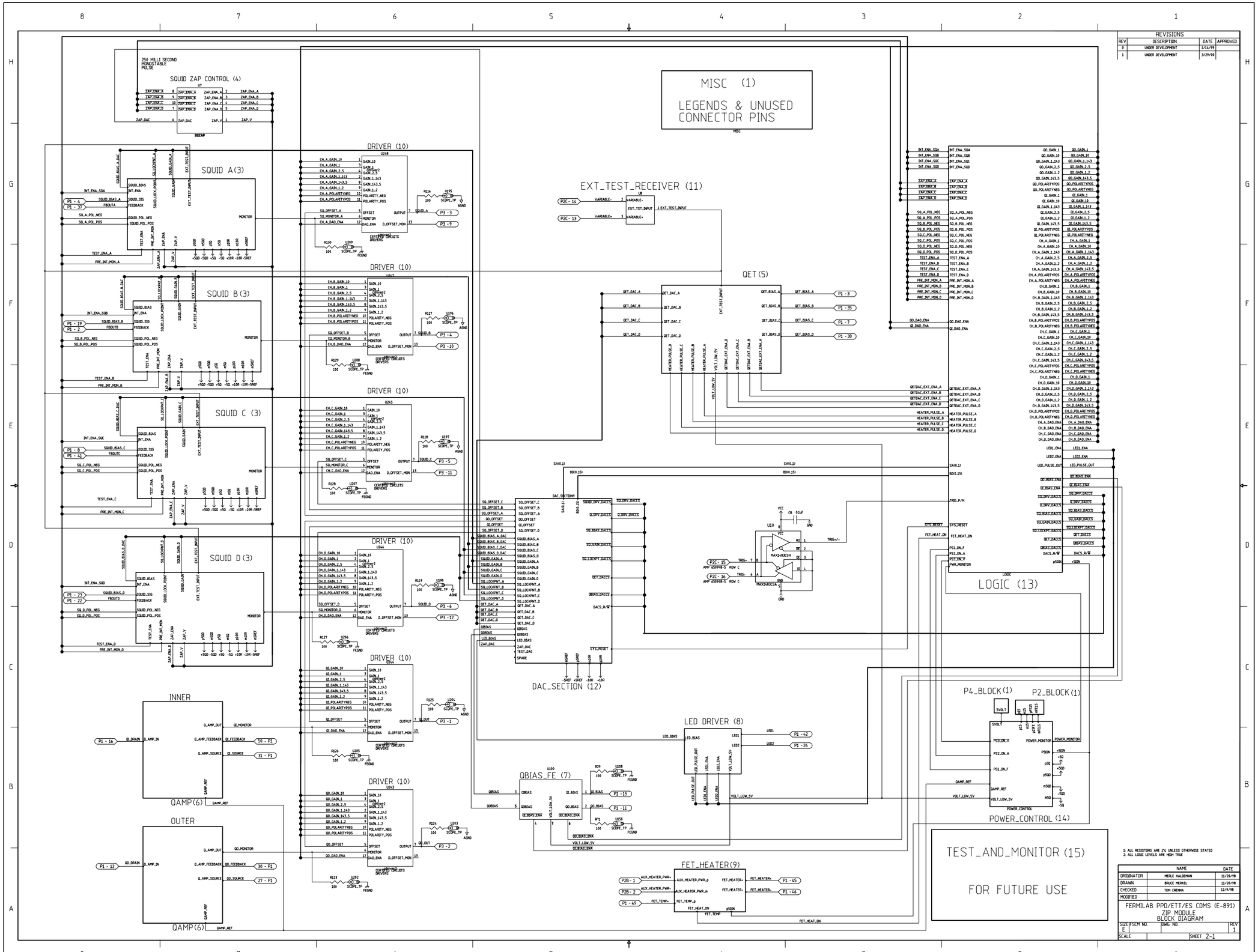
Available for possible future addition

	SECTIONS	SUBSECTIONS 0	1	2	3	4	5	6	7	E	F
F	COMMAND	RESET									Test Pulse
E	CSR	SPARE									FET Heater
D	SPARE	SPARE	DAC 3 SENSOR BIAS D	DAC 3 SQUID BIAS D	DAC 3 SQUID LOCK D	DAC 3 SQUID GAIN D	DAC 3 SQUID D DRIVER OFFSET				
C	SPARE	SPARE	DAC 2 SENSOR BIAS C	DAC 2 SQUID BIAS C	DAC 2 SQUID LOCK C	DAC 2 SQUID GAIN C	DAC 2 SQUID C DRIVER OFFSET				
B	SPARE	SPARE	DAC 1 SENSOR BIAS B	DAC 1 SQUID BIAS B	DAC 1 SQUID LOCK B	DAC 1 SQUID GAIN B	DAC 1 SQUID B DRIVER OFFSET				
A	SPARE	SPARE	DAC 0 SENSOR BIAS A	DAC 0 SQUID BIAS A	DAC 0 SQUID LOCK A	DAC 0 SQUID GAIN A	DAC 0 SQUID A DRIVER OFFSET				
9	SPARE	SPARE									
8	SPARE	SPARE									
7	Q BIAS DAC	SPARE									
6	Q DRIVER DAC	+15A									
5	SQUID DRIVER DAC	-15A								CSR5	
4	SQUID GAIN DAC	+15FE								CSR4	
3	SQUID LOCK DAC	-15FE							DAC 3 ZAP VOLTAGE	CSR3	
2	SQUID BIAS DAC	+5						DAC 2 TEST VOLTAGE	DAC 2 LED BIAS	CSR2	
1	SENSOR BIAS DAC	TEMP						DAC 1 Qi DRIVER OFFSET	DAC 1 Qi BIAS	CSR1	
0	MODULE INFO.	I D						DAC 0 Qo DRIVER OFFSET	DAC 0 Qo BIAS	CSR0	

Notes:

1. For addressing purposes, modules are divided into 16 sections, each having a 4 bit address. Each section is divided into 16 subsections. For example, in order to address the FET Heater of a ZIP Module plugged into Subrack-SLOT 7, you would use address 0011111111110; or hexadecimal address 07FE
2. Command Column (F) items only require a write command to the address to execute.

Merle Haldeman
Revised 7/21/2003



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDER DEVELOPMENT	1/14/99	
1	UNDER DEVELOPMENT	3/29/00	

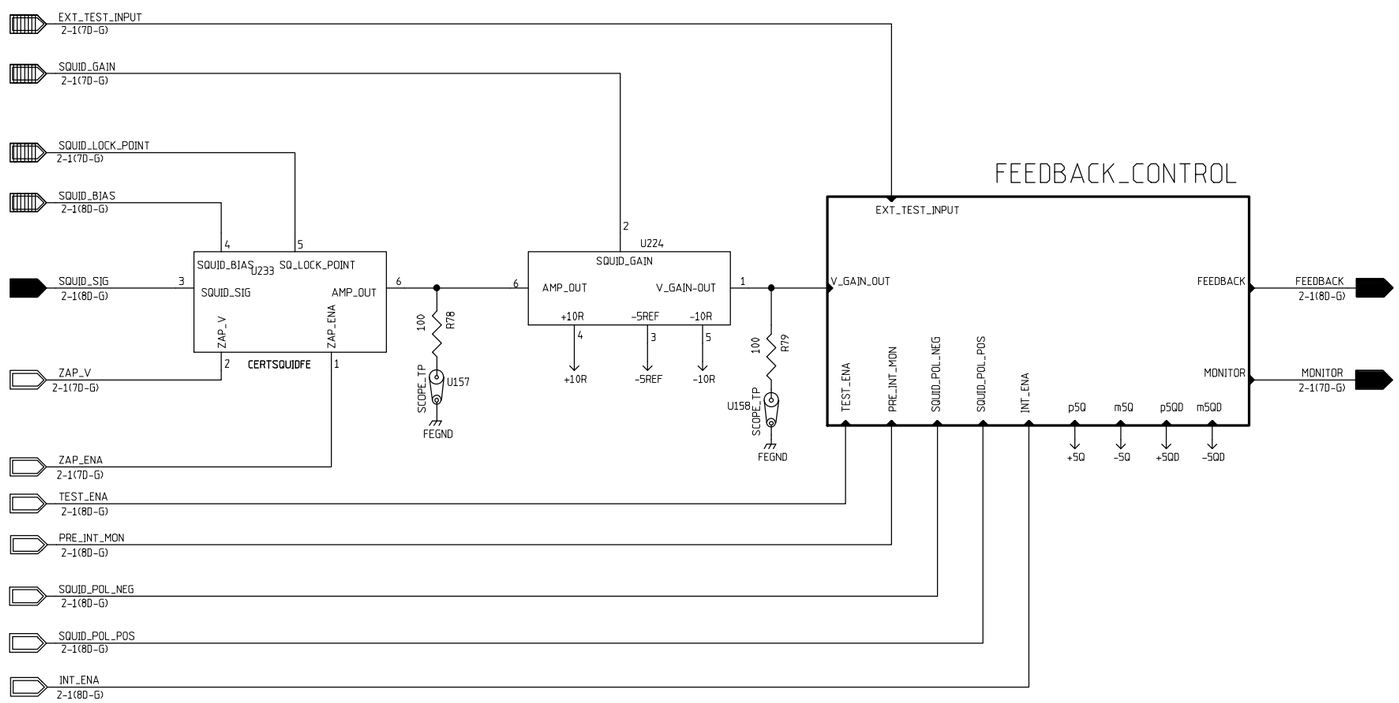
1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE MEM TRUE

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/20/98
DRAWN	BRUCE MERKEL	11/20/98
CHECKED	TOM CRENNA	12/9/98
MODIFIED		

FERMILAB PPD/ETT/ES COMS (E-891)
ZIP MODULE
BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
E			1
SCALE		SHEET 2-1	

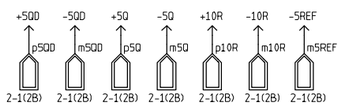
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SQUID FRONT END

SQUID VARIABLE GAIN AMPLIFIER

SQUID FEEDBACK CONTROL



1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

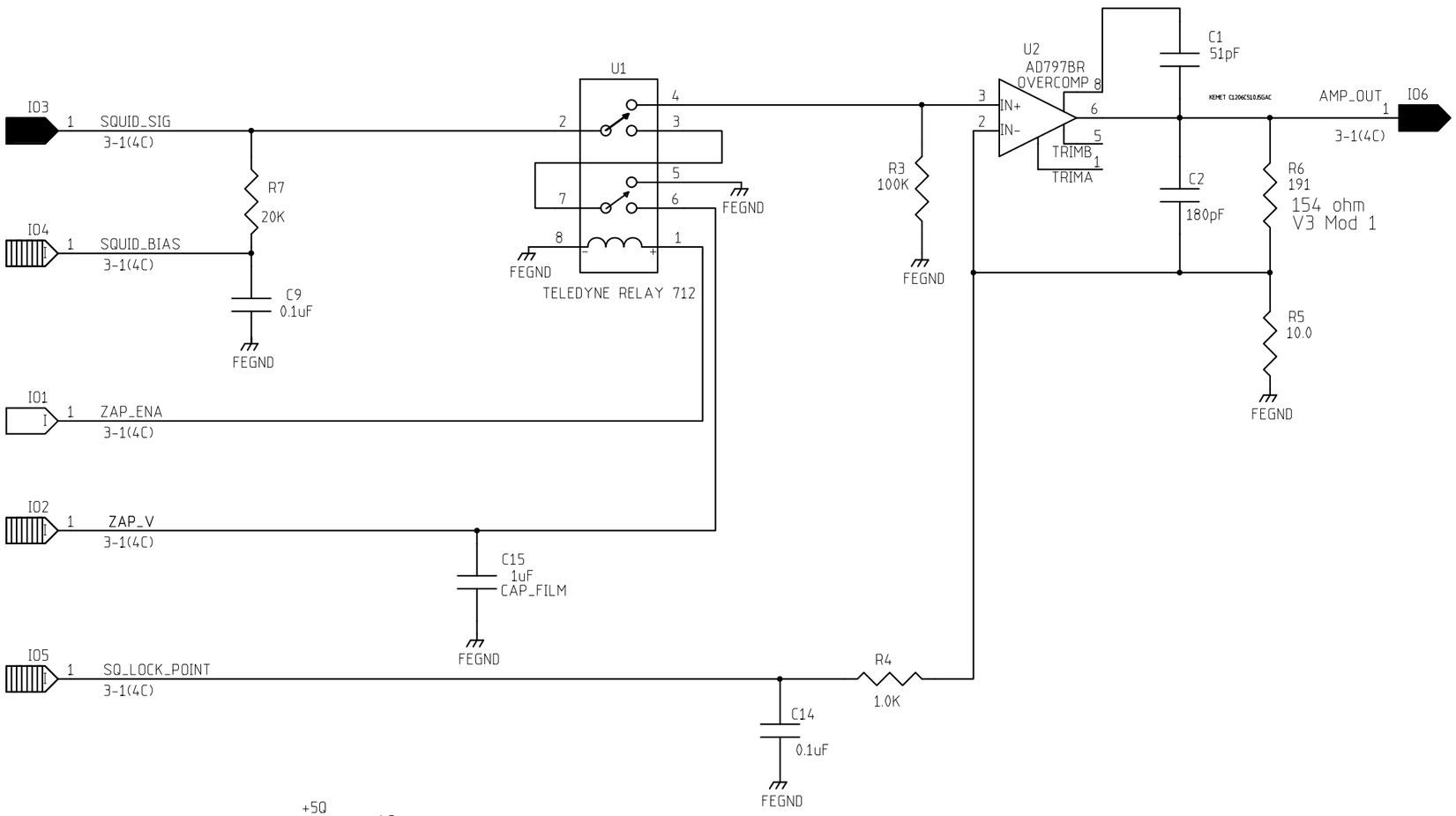
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

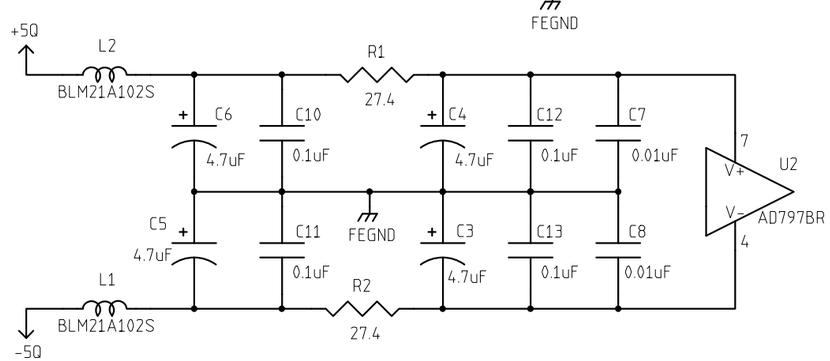
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 3-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

RELAY SHOWN IN
DEENERGIZED STATE



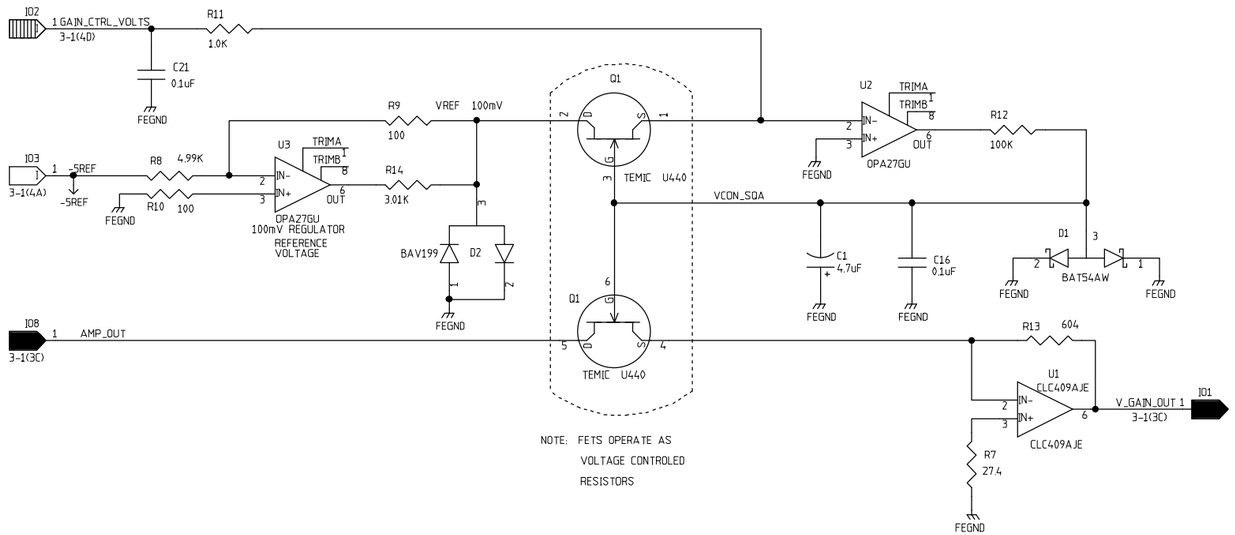


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/11/98
DRAWN	BRUCE MERKEL	11/11/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FRONT END

SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 3-2	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



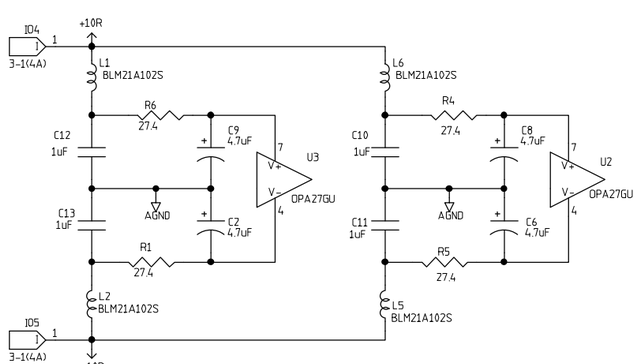
NOTE: FETS OPERATE AS
VOLTAGE CONTROLED
RESISTORS

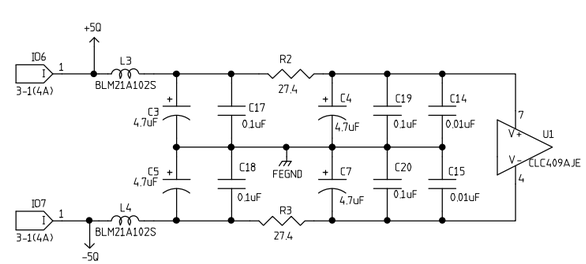
VARIABLE GAIN AMPLIFIER

$$GAIN = R13 \times \frac{GVC}{100}$$

GCV = GAIN_CONTROL_VOLTAGE IN VOLTS

R13 IN OHMS

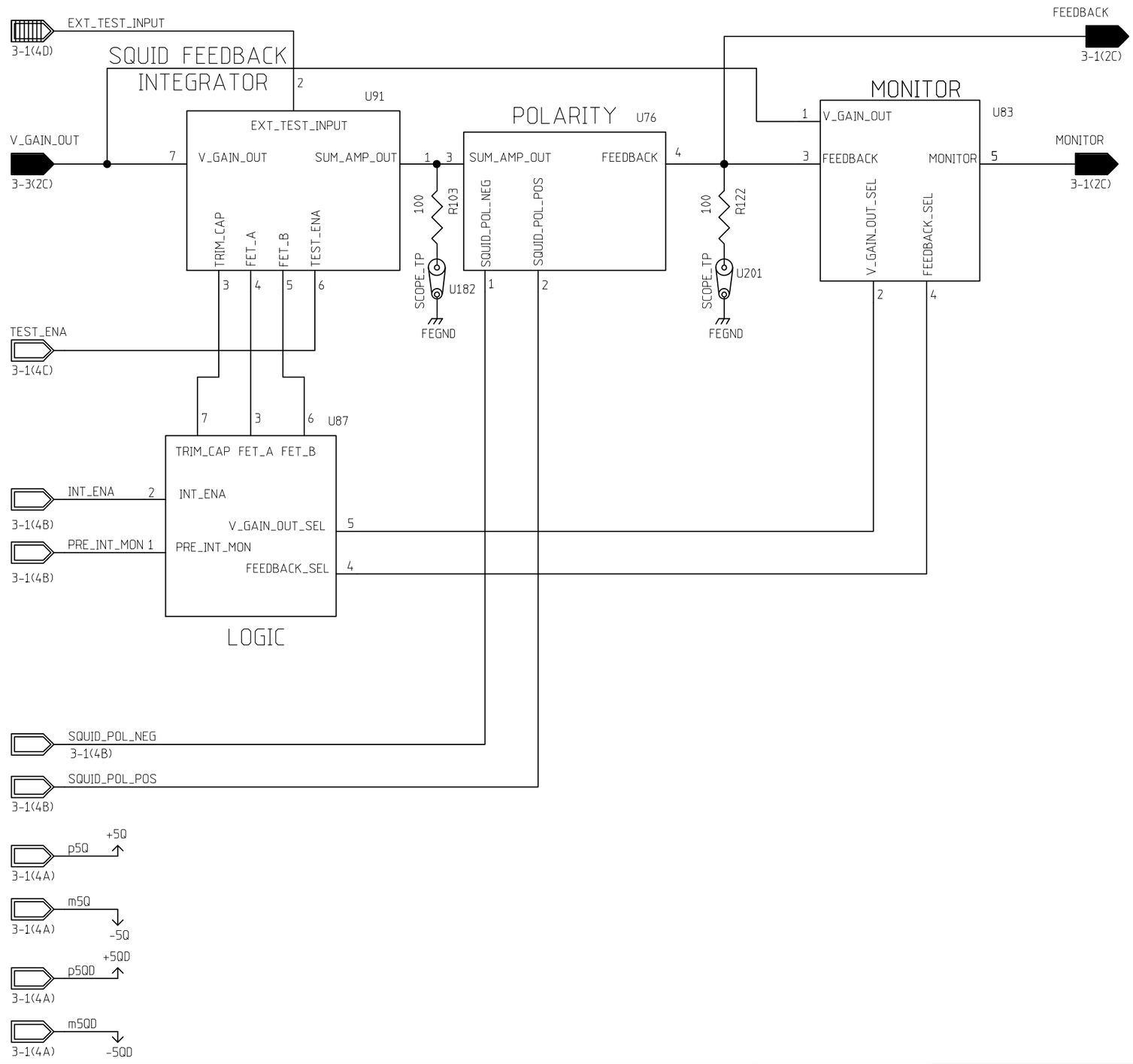




	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID VARIABLE GAIN AMP

SIZE	FSCM NO.	DWG. NO.	REV
C			
SCALE		SHEET 3-3	



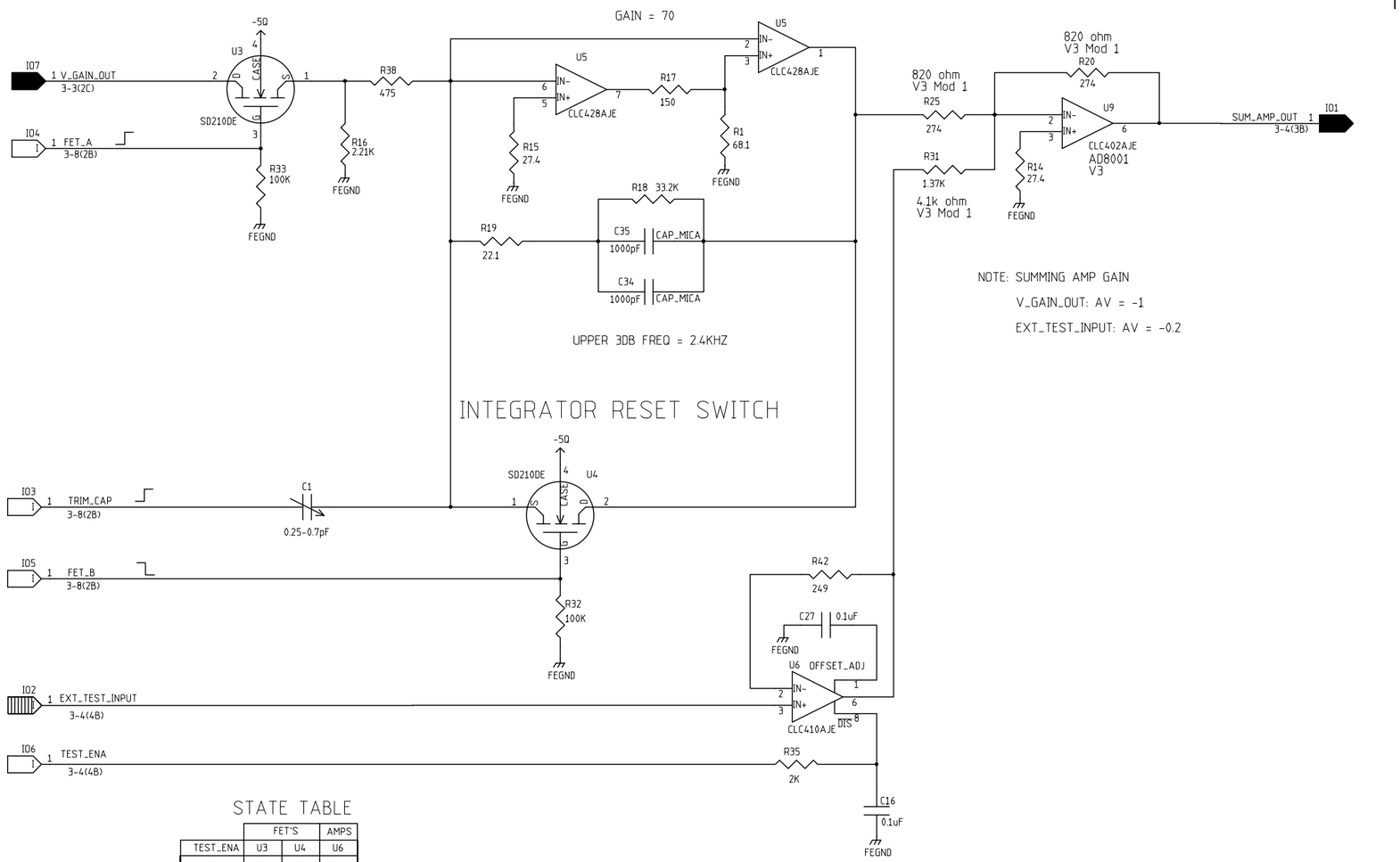
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 3-4	

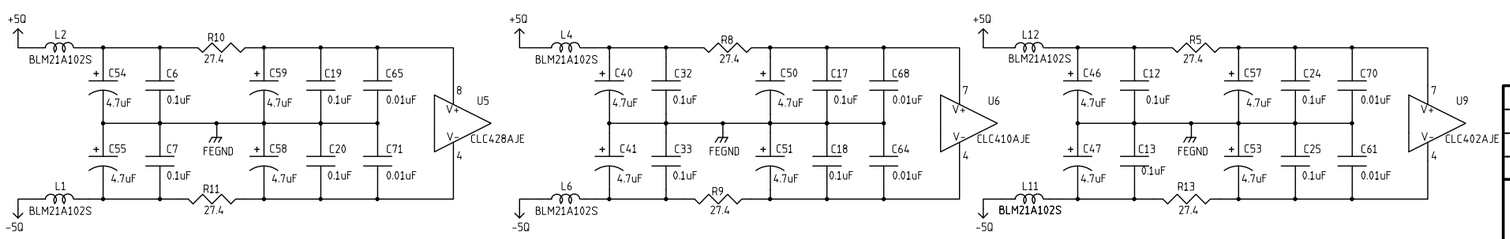
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	UPDATED FOR VERSION 1	9/17/99	



STATE TABLE

	FET'S		AMPS
TEST_ENA	U3	U4	U6
LOW	O	C	E
HI	C	O	D

O = OPEN C = CLOSED
E = ENABLE D = DISABLE

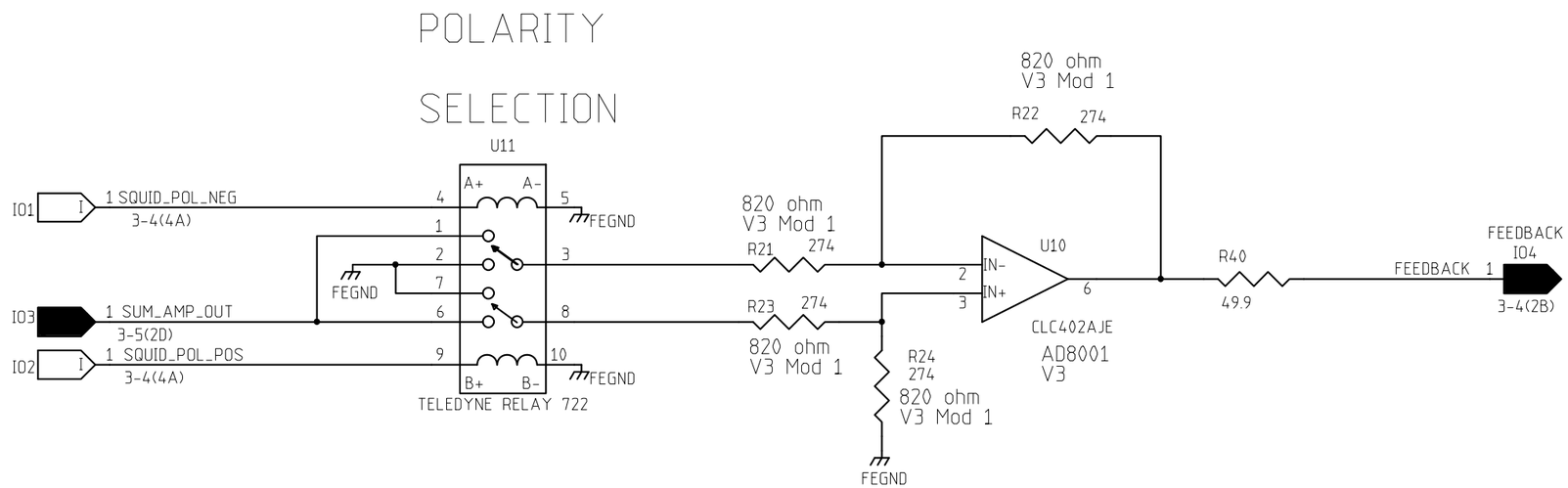


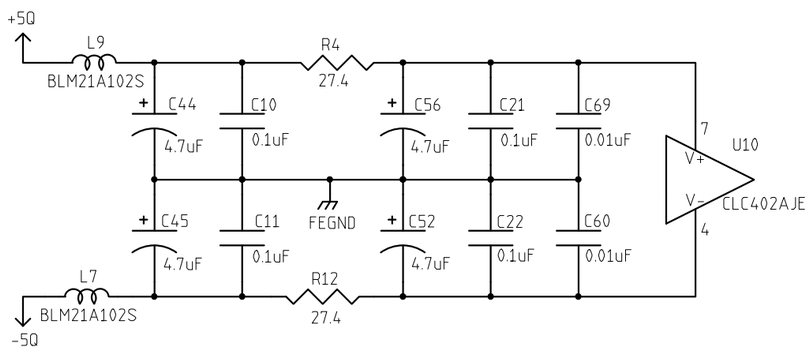
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK INTEGRATOR

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 3-5	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

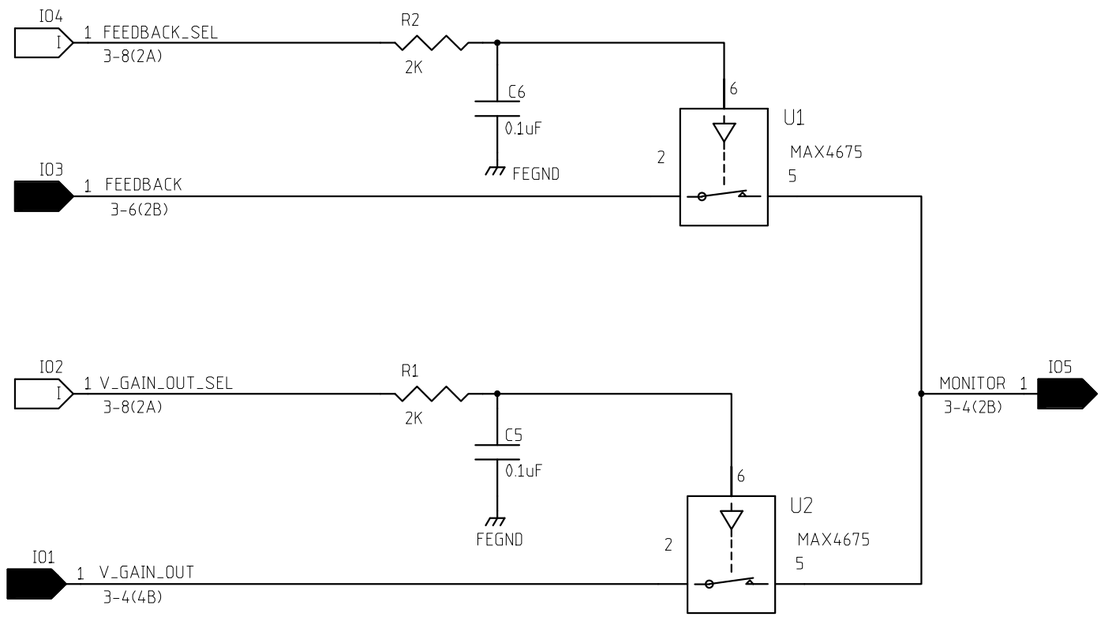
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK POLARITY

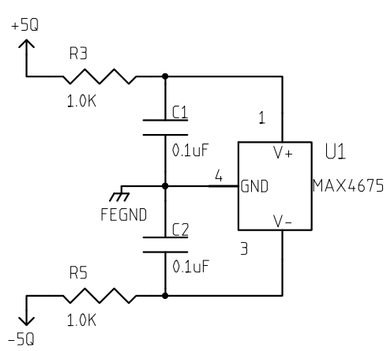
SIZE	FSCM NO.	DWG. NO.	REV
B			

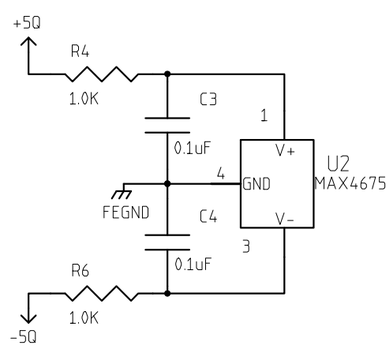
SCALE | SHEET 3-6

MONITOR SELECTION SWITCHES

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
2	REPLACED OP AMPS WITH ANALOG SWITCH	12/08/2K	







MAX4675	
IN	SWITCH
0	OFF
1	ON

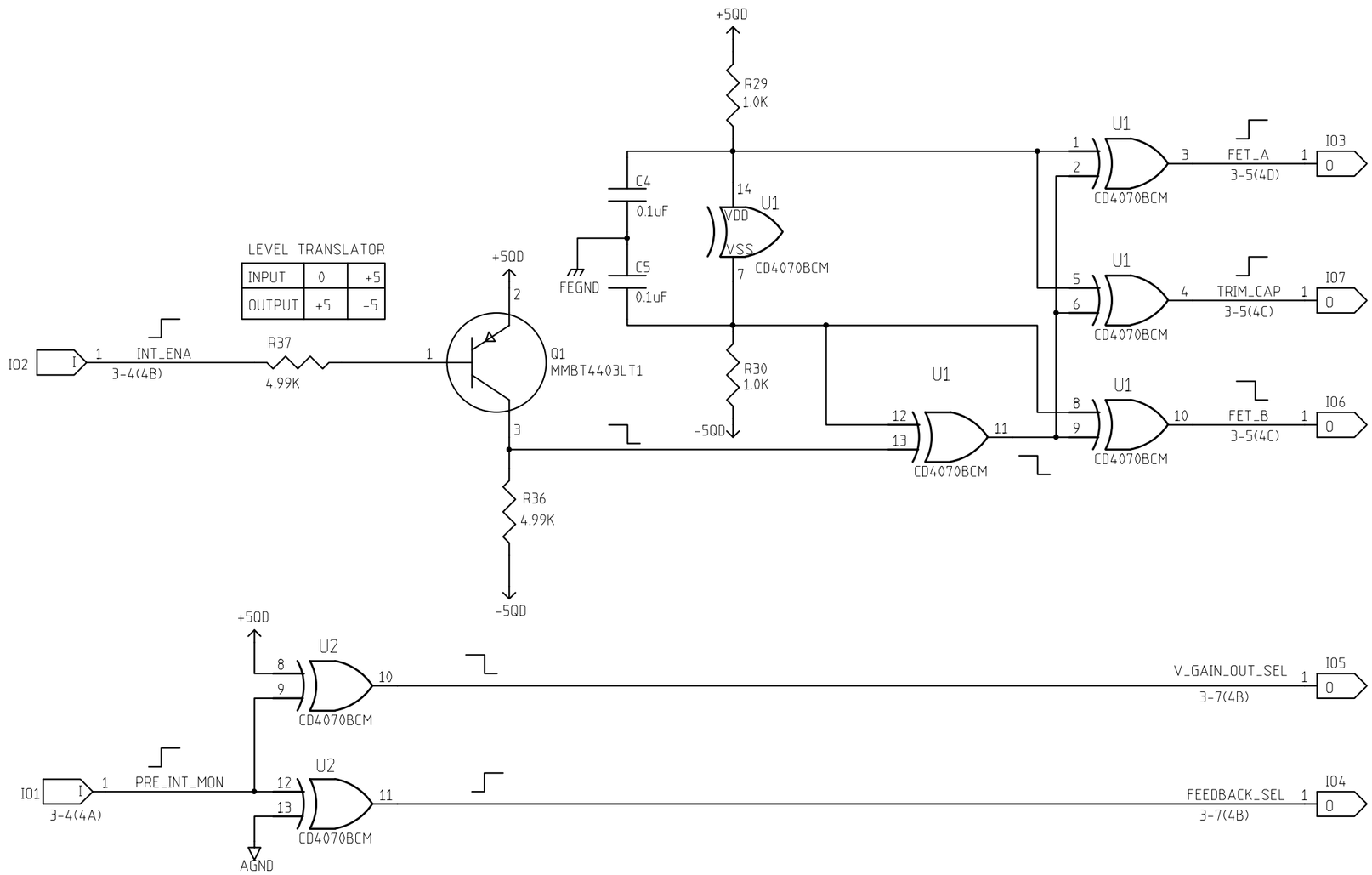
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

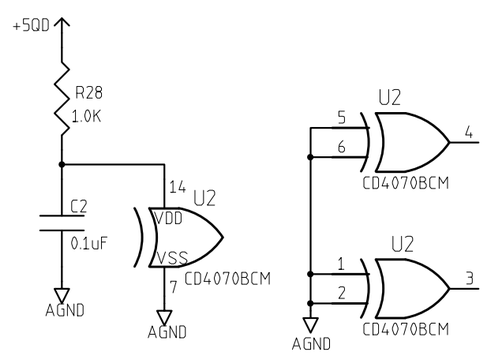
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK MONITOR

SIZE	FSCM NO.	DWG. NO.	REV
B			2

SCALE | SHEET 3-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





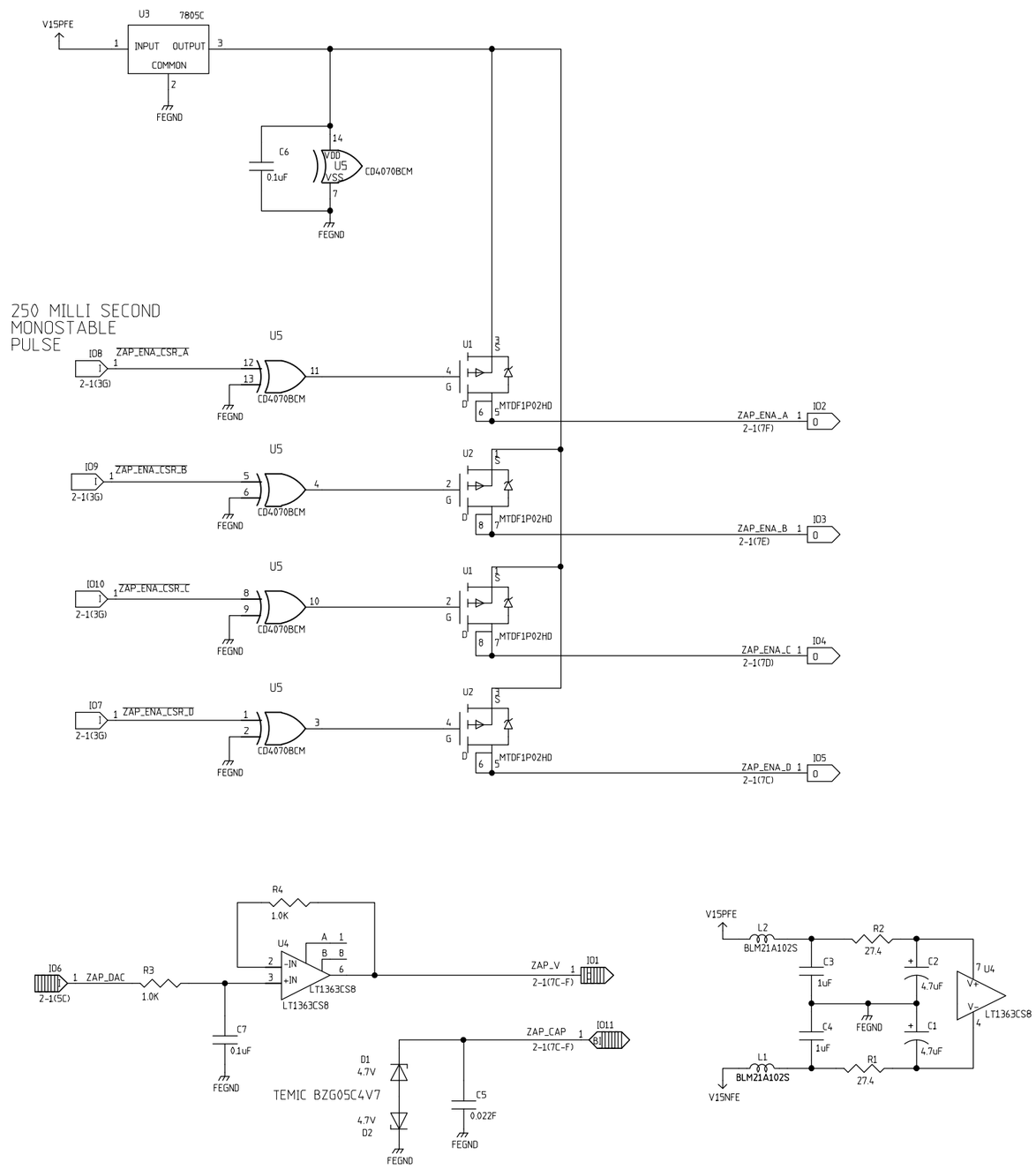
NOTE: U1 POWER SHOWN ABOVE

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK LOGIC

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 3-8	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



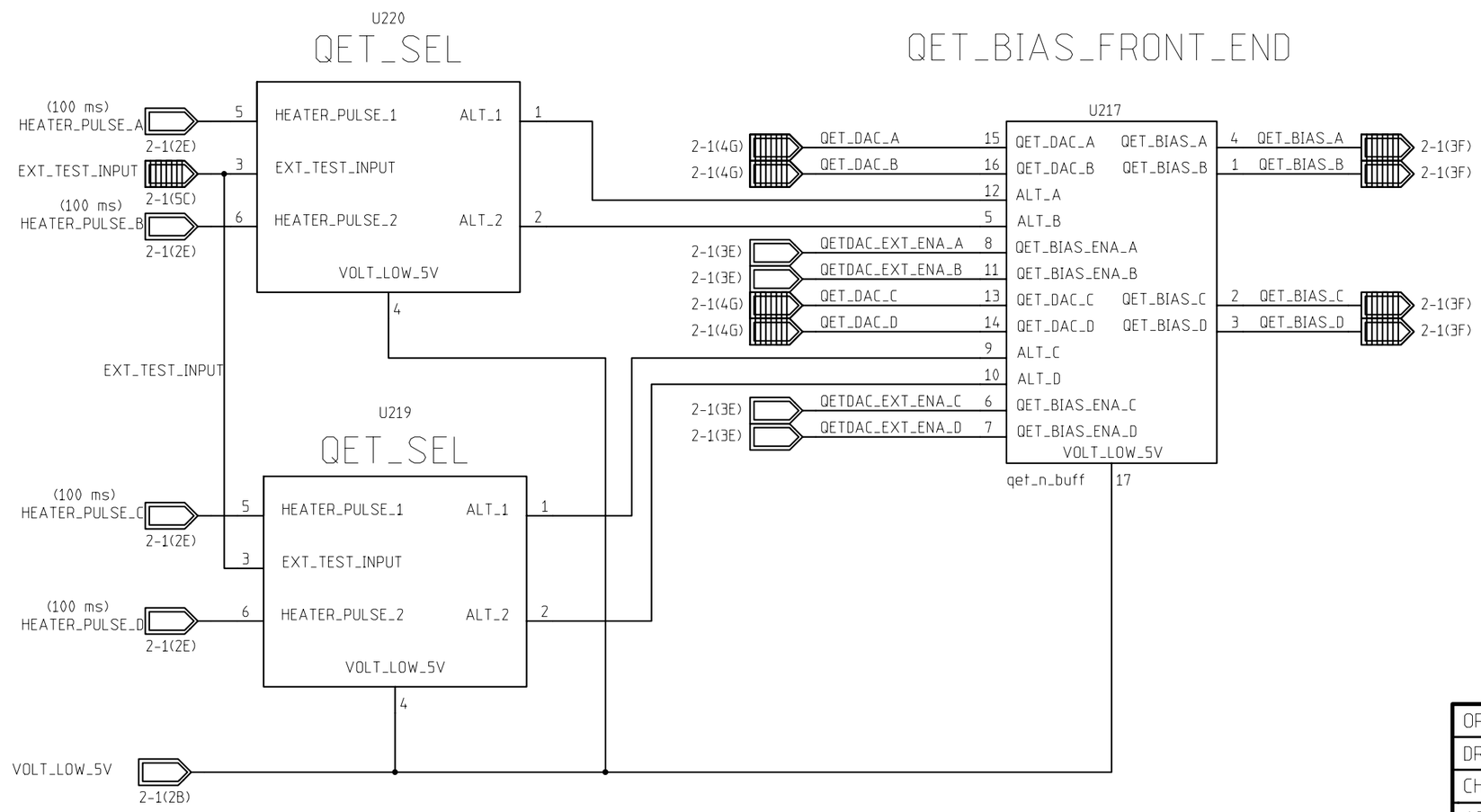
REVISED 1/11/99 BRUCE MERKEL

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID ZAP CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
C			
SCALE		SHEET 4-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDER DEVELOPMENT	1-20-99	

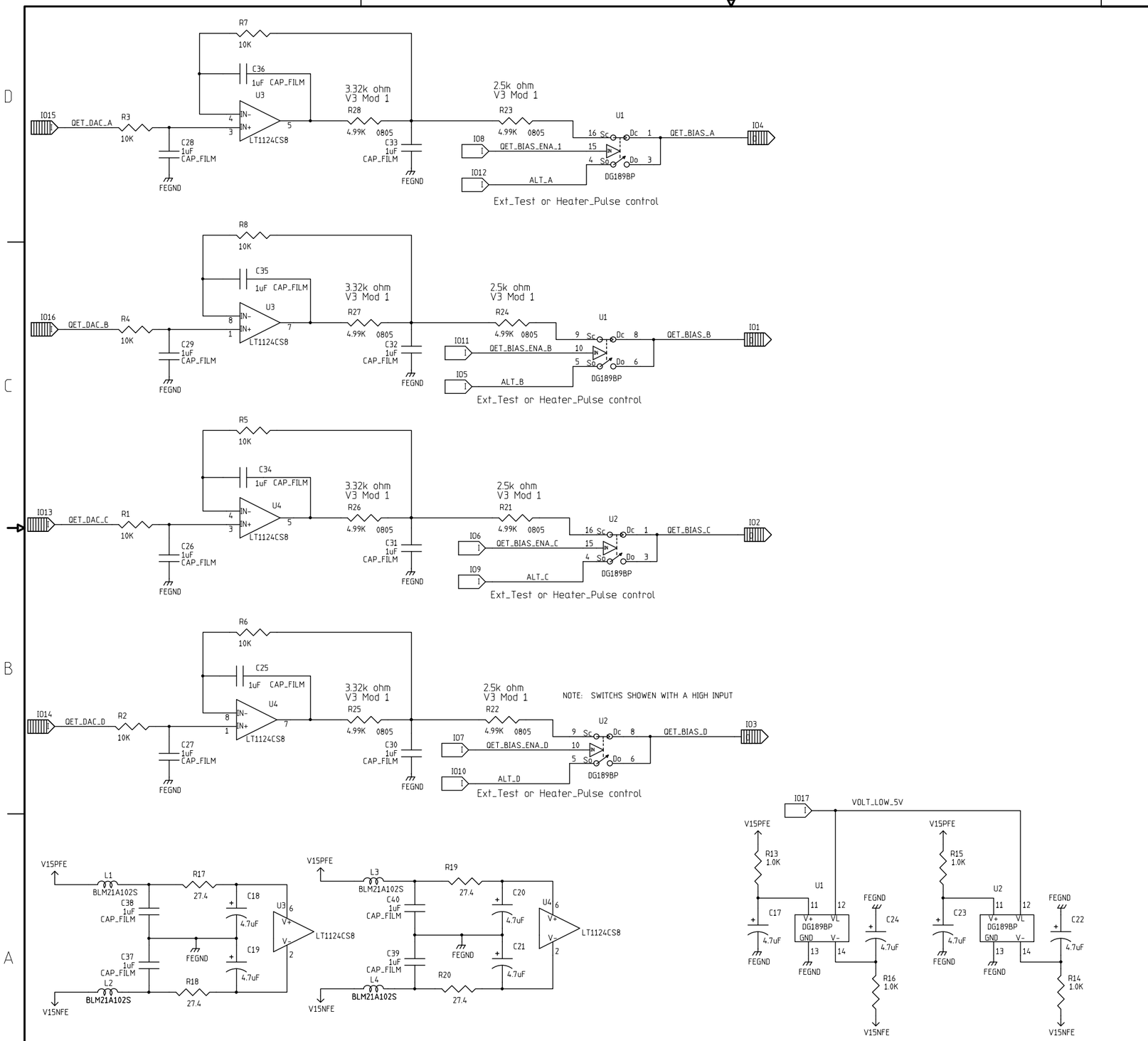


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QET BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 5-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	REPLACED 1uF CAPS WITH BACK TO BACK 4.7uF TANT. CAPS	2 29 00	BDM



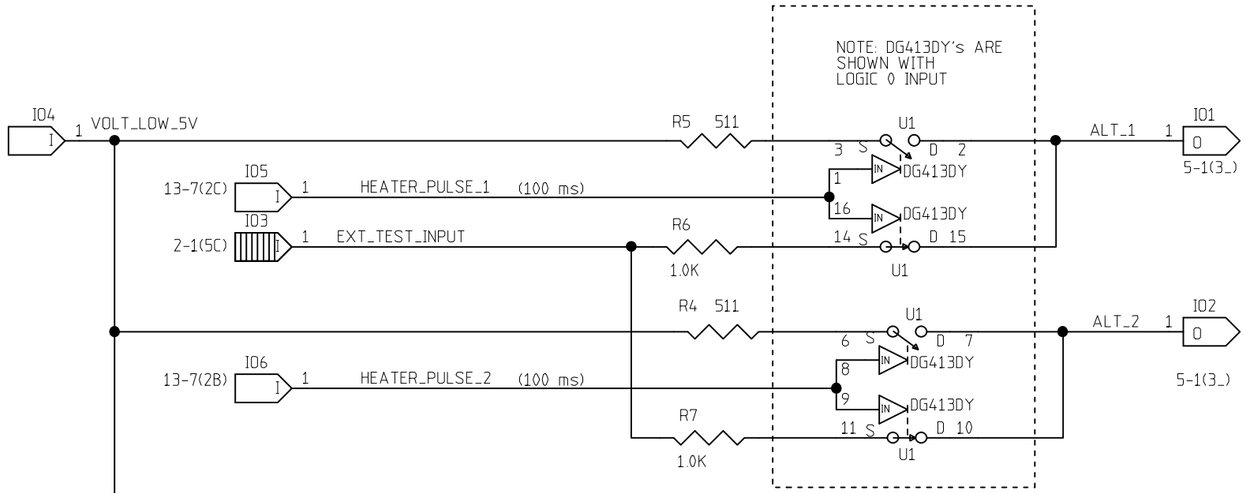
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	06/17/99
DRAWN	BRUCE MERKEL	07/16/99
CHECKED		
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QET BIAS FRONT END

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 5-2	

DWG. NO.
SH.
REV

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



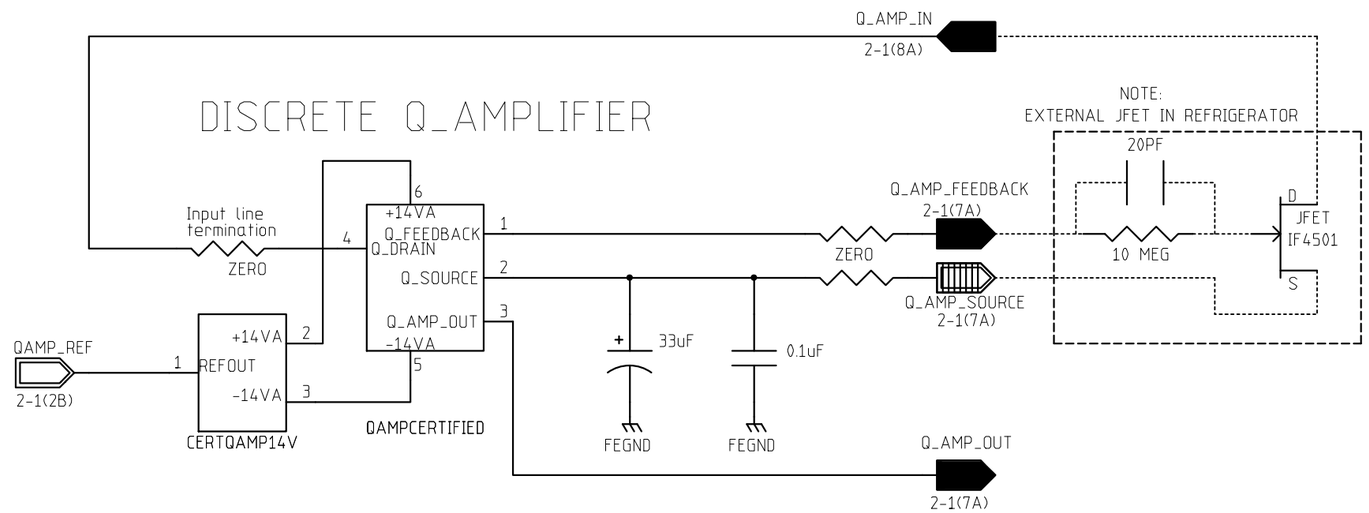
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	07/16/99
CHECKED		
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QET_SEL

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 5-4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

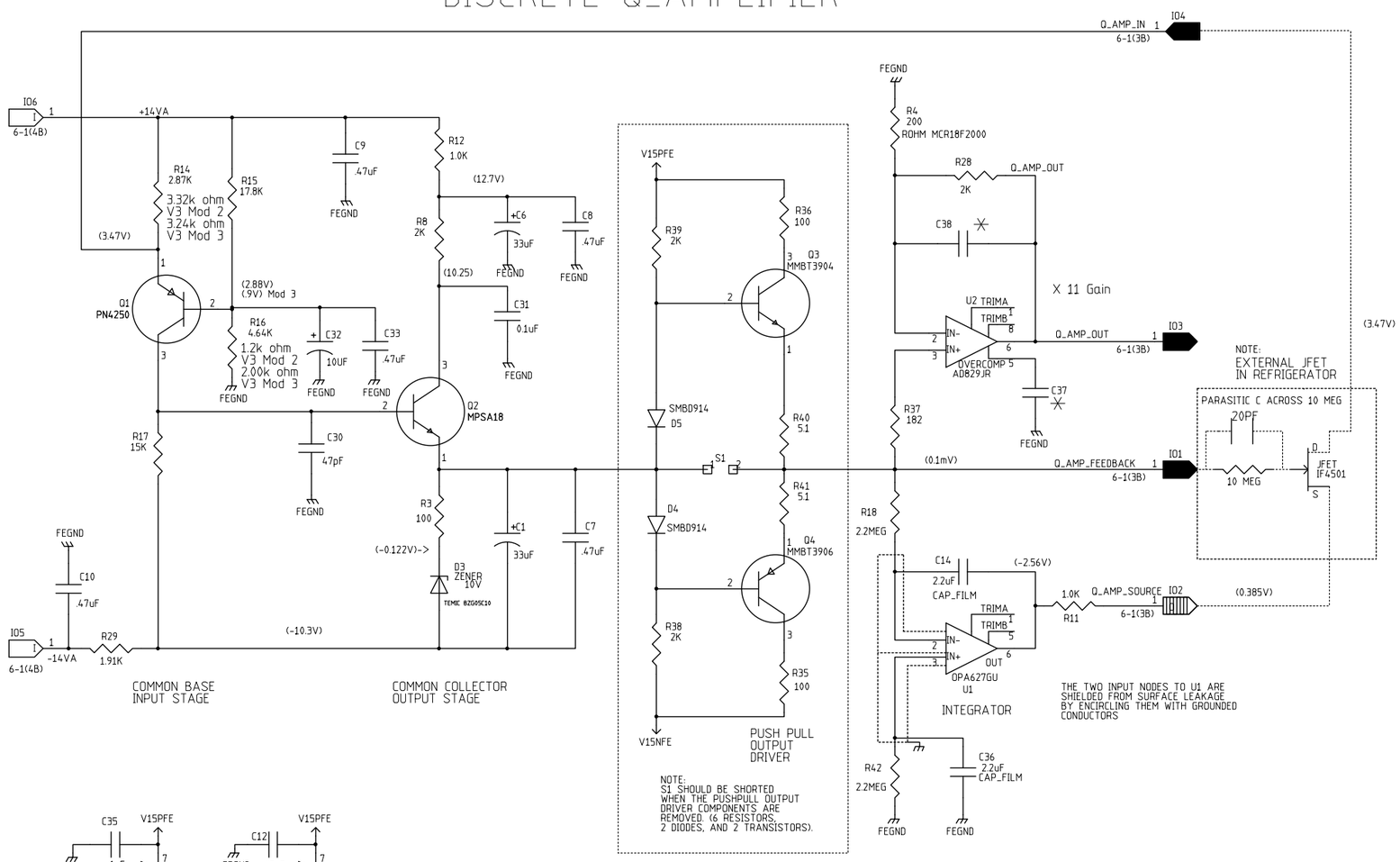
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QAMP BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 6-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	GENERAL MODIFICATIONS	9/27/99	B.MERKEL
2	REPLACED U2 MOD U1 REPLACE C30	11/13/00	B MERKEL

DISCRETE Q_AMPLIFIER



(VOLTAGE) DC REFERENCE VOLTAGES
WITH LOOP CLOSED

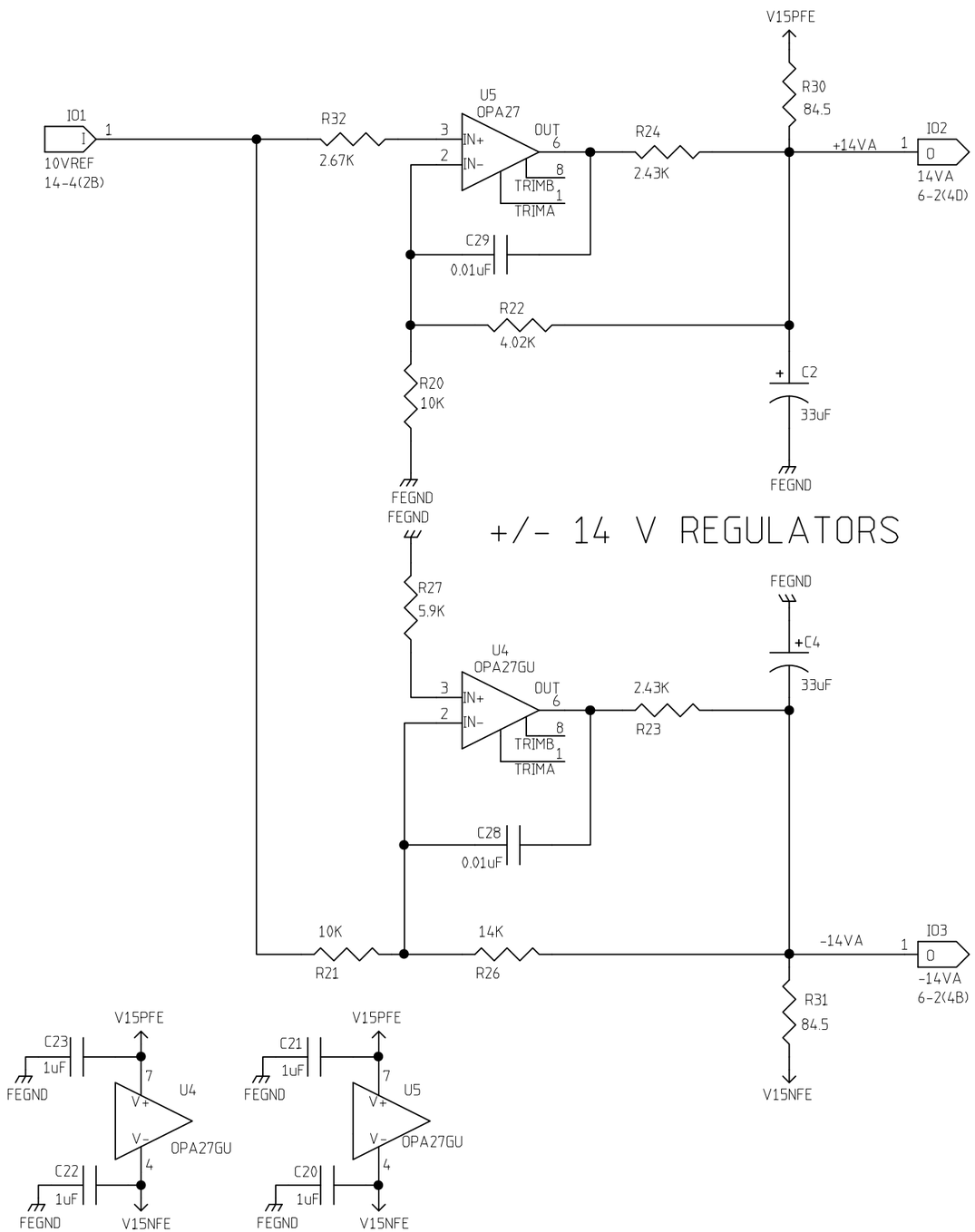
✳ VALUE TO BE DETERMINED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/EET/ES CDMS (E-891)
ZIP MODULE
DISCRETE Q AMPLIFIER

SIZE	FSCM NO.	DWG. NO.	REV
C			2
SCALE		SHEET 6-2	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



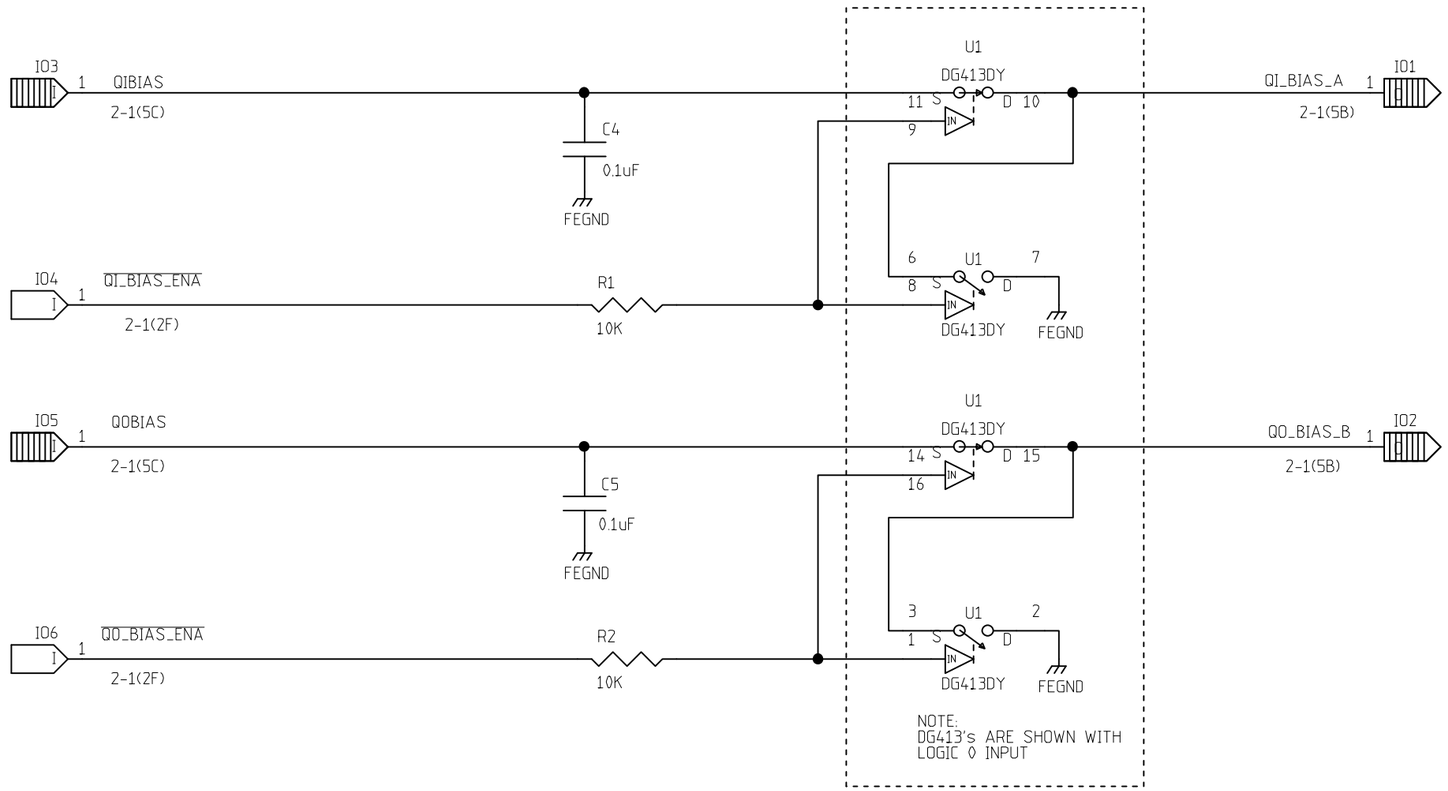
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

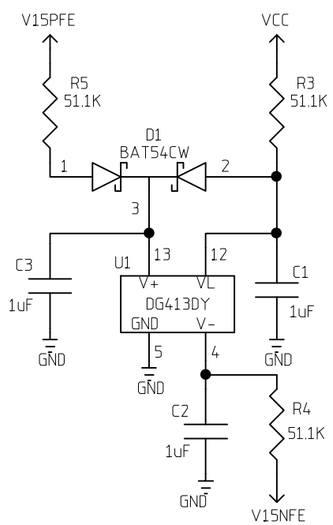
FERMILAB PPD/ ETT/ ES CDMS (E-891)

ZIP MODULE

Q AMP 14V

SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 6-3	





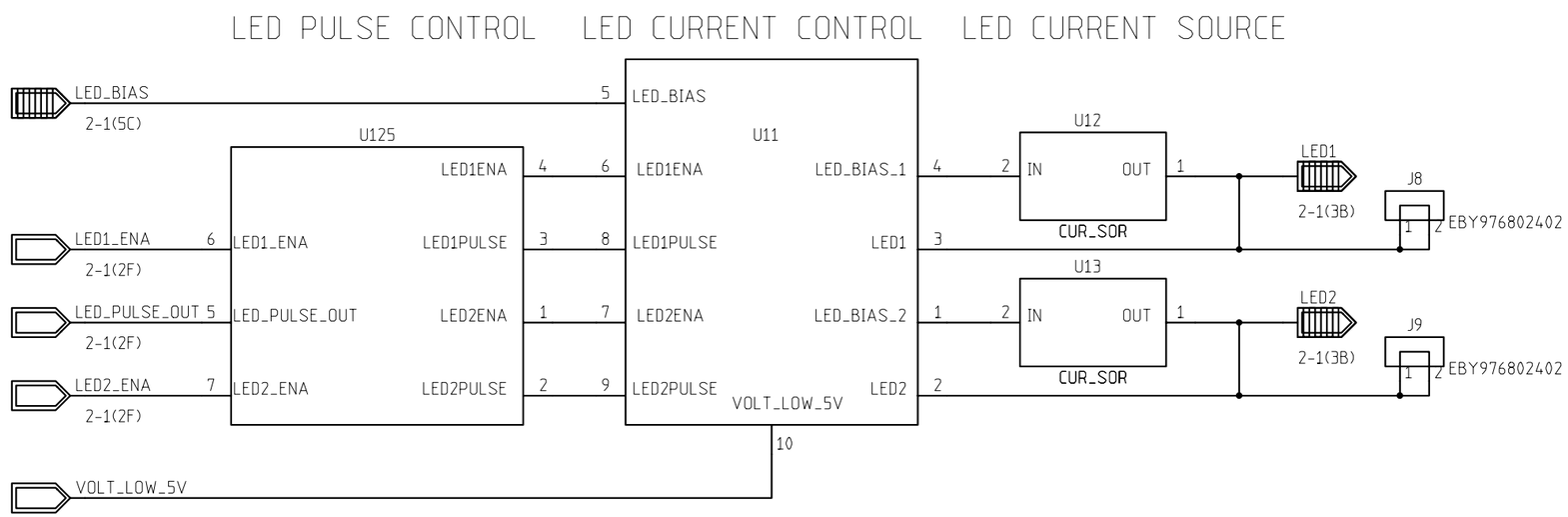
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	12/08/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QBIAS FRONT END

SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 7-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	MOVED DIGITAL OUT OF ANALOG AREA	3/24/99	B MERKEL



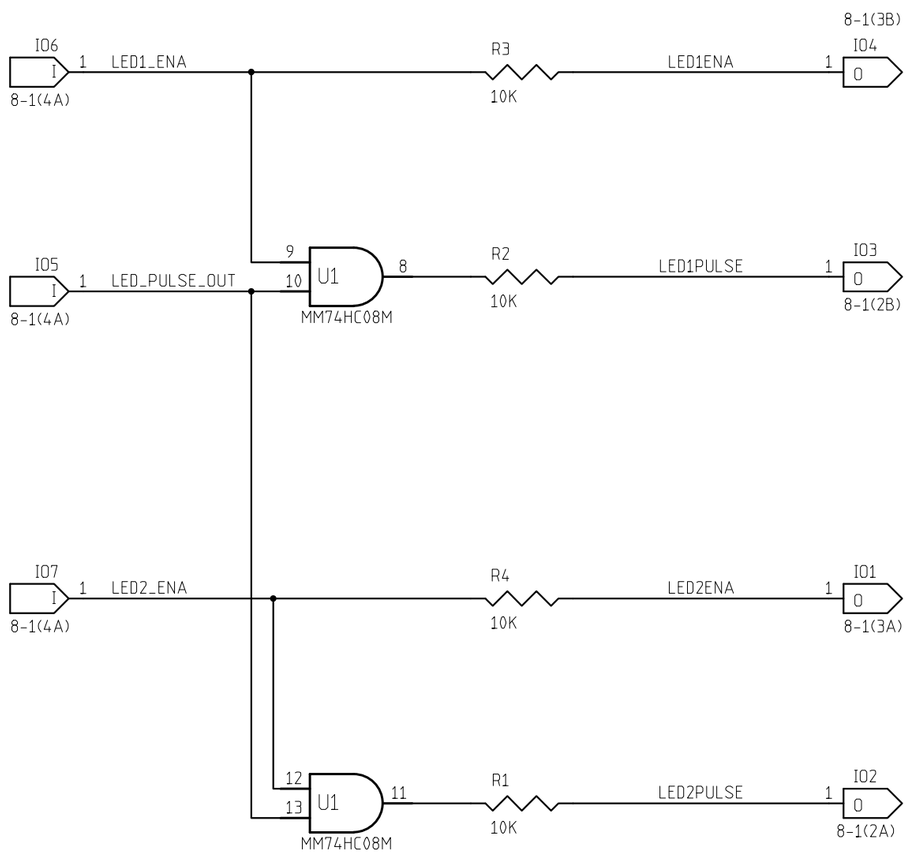
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	3/24/99
CHECKED		
APPROVED		

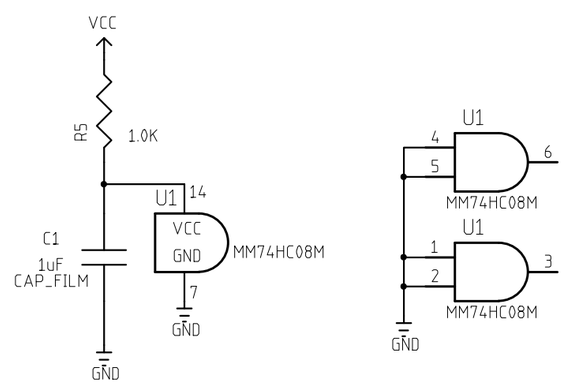
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
LED BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE		SHEET 8-1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





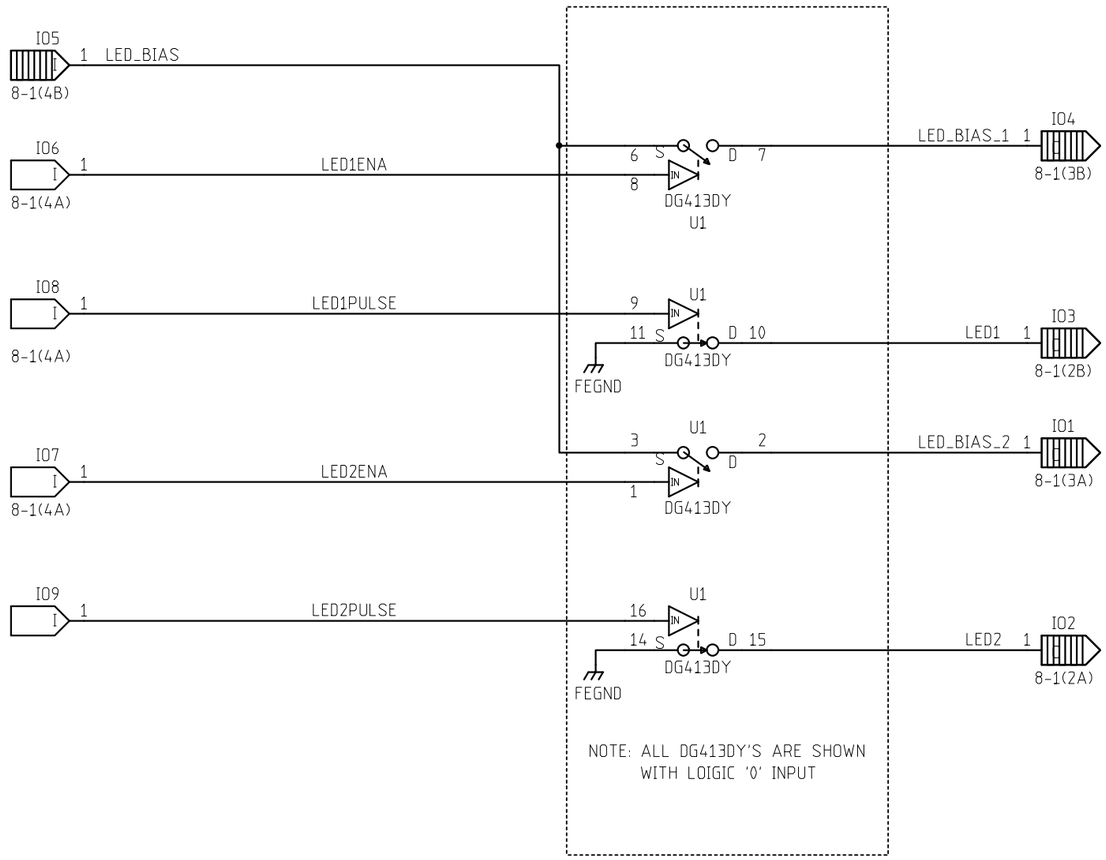
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	3/24/99
DRAWN	BRUCE MERKEL	3/24/99
CHECKED		
APPROVED		

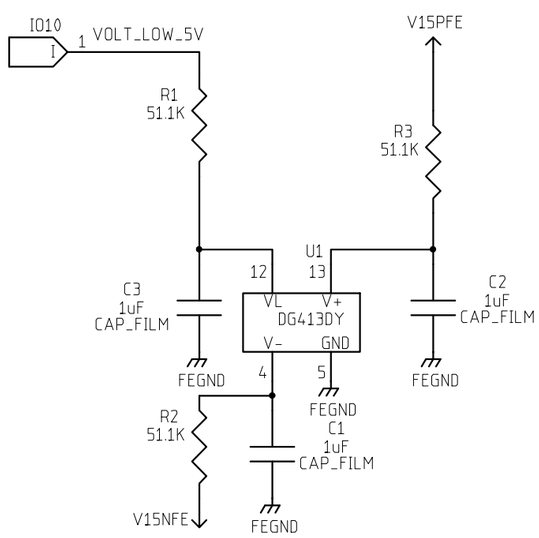
FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
LED PULSE CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 8-3

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	ADDED A 5V OUTSIDE SOURCE AND REMOVED THE DIGITAL LOGIC TO THE DIGITAL SECTION	3/24/99	B MERKEL

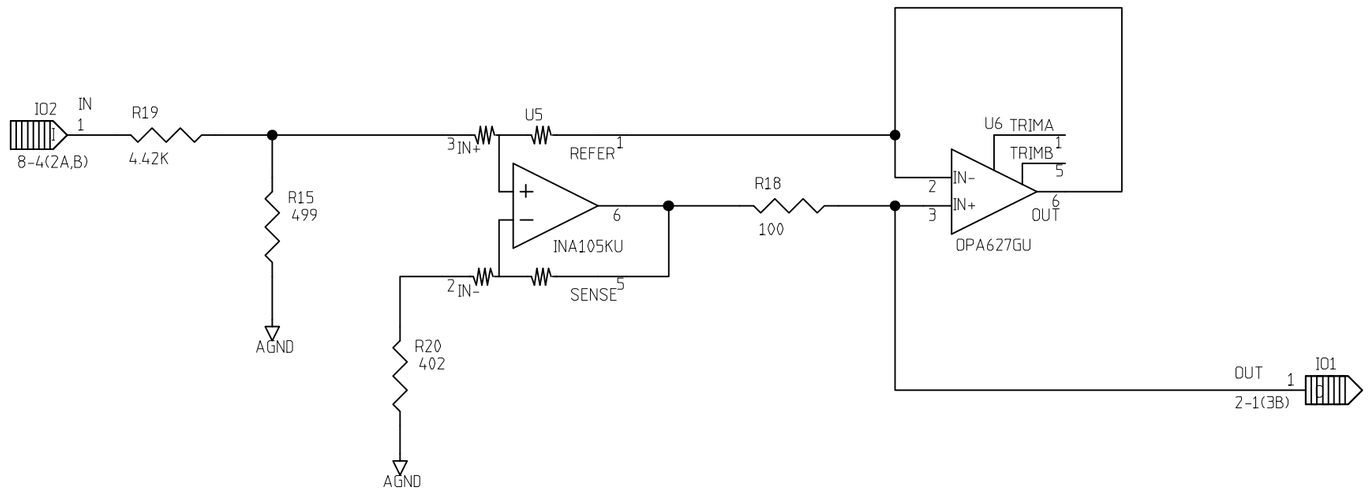


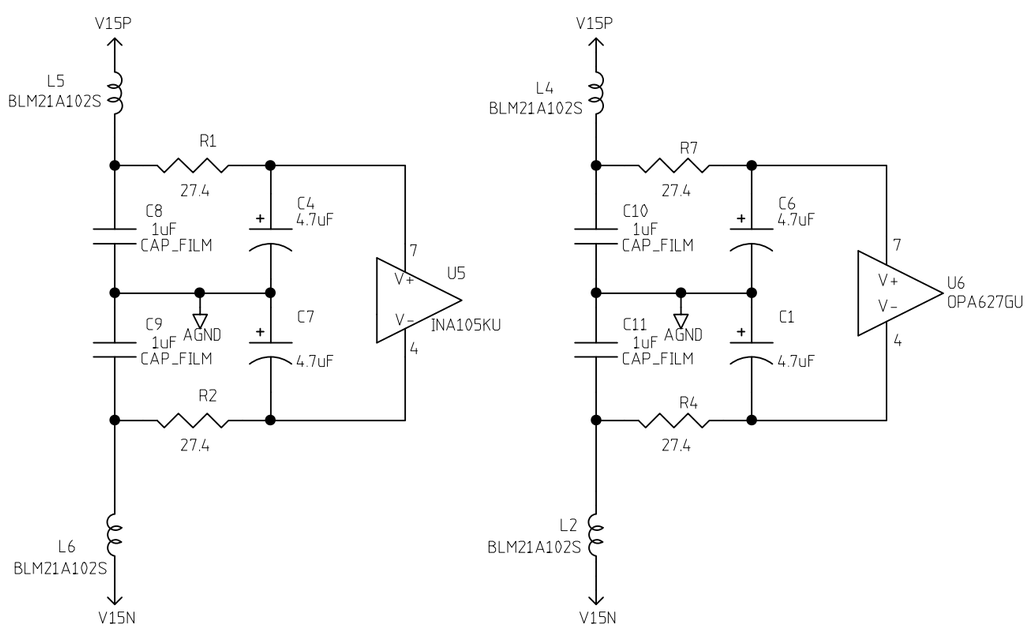


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	12/17/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
LED CURRENT CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 8-4	





REVISIONS

REV	DESCRIPTION	DATE	APPROVED
1	CHANGED RESISTOR R18 TO 499 OHM	9/25/00	BDM
2	CHANGED RESISTOR R18 TO 100 OHM ADDED RESISTOR R19	4/4/01	BDM
3	CHANGED RESISTORS R15 AND R19 AND ADDED RESISTOR R20	6/19/01	BDM

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	12/09/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

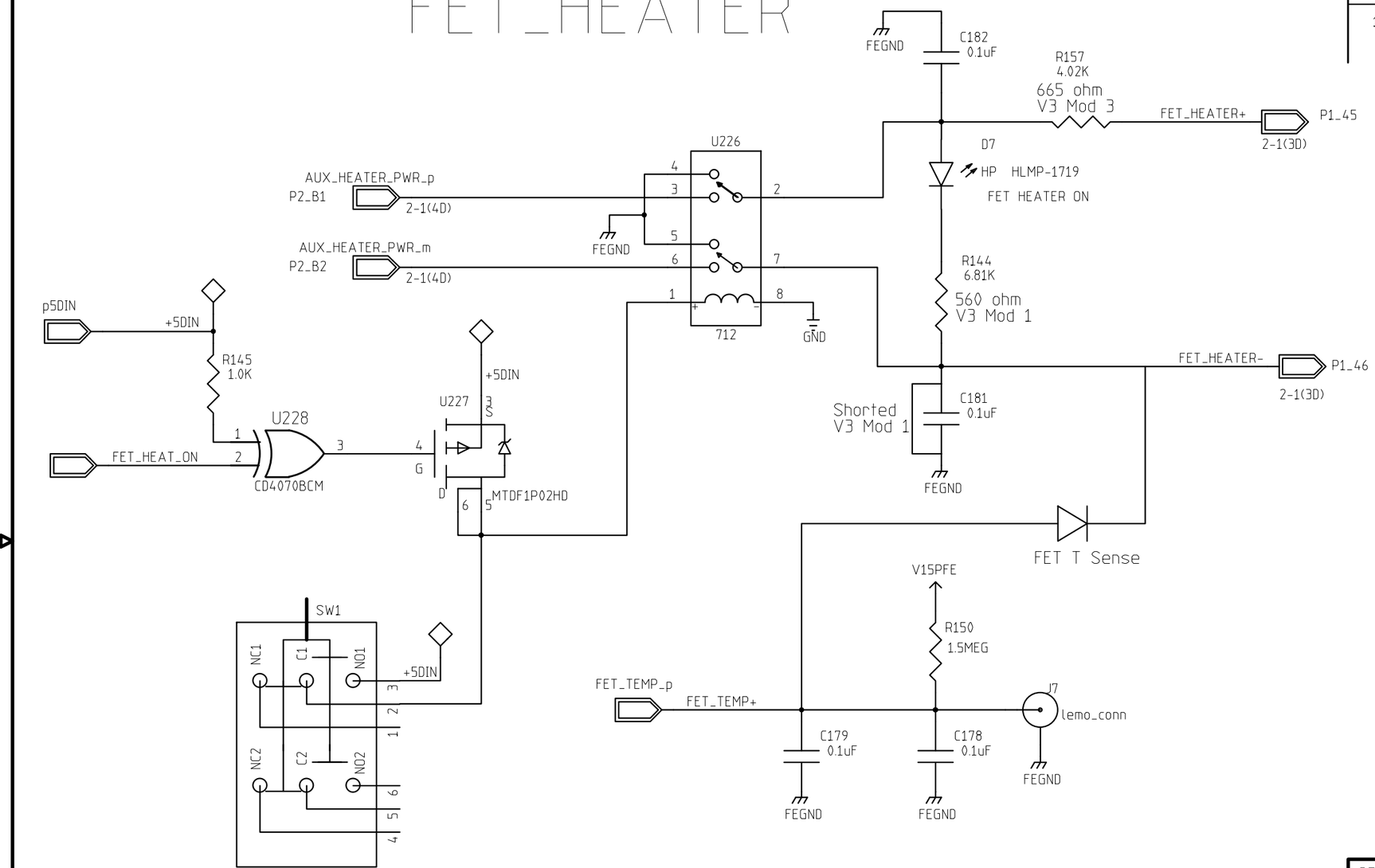
FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
LED CURRENT SOURCE

SIZE	FSCM NO.	DWG. NO.	REV
B			3

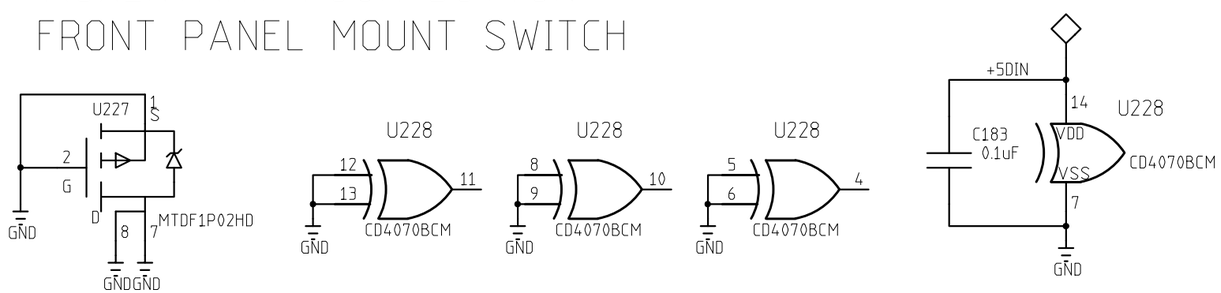
SCALE | SHEET 8-5

FET_HEATER

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	SCHEMATIC UPDATED FOR VERSION 1	10/18/99	BDM



MONENTARY PUSH BUTTON
FRONT PANEL MOUNT SWITCH



1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	9/23/99
DRAWN	BRUCE MERKEL	9/23/99
CHECKED		
APPROVED		

FERMILAB PPD/EET/ES CDMS (E-891)
ZIP MODULE
FET_HEATER

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 9-1	

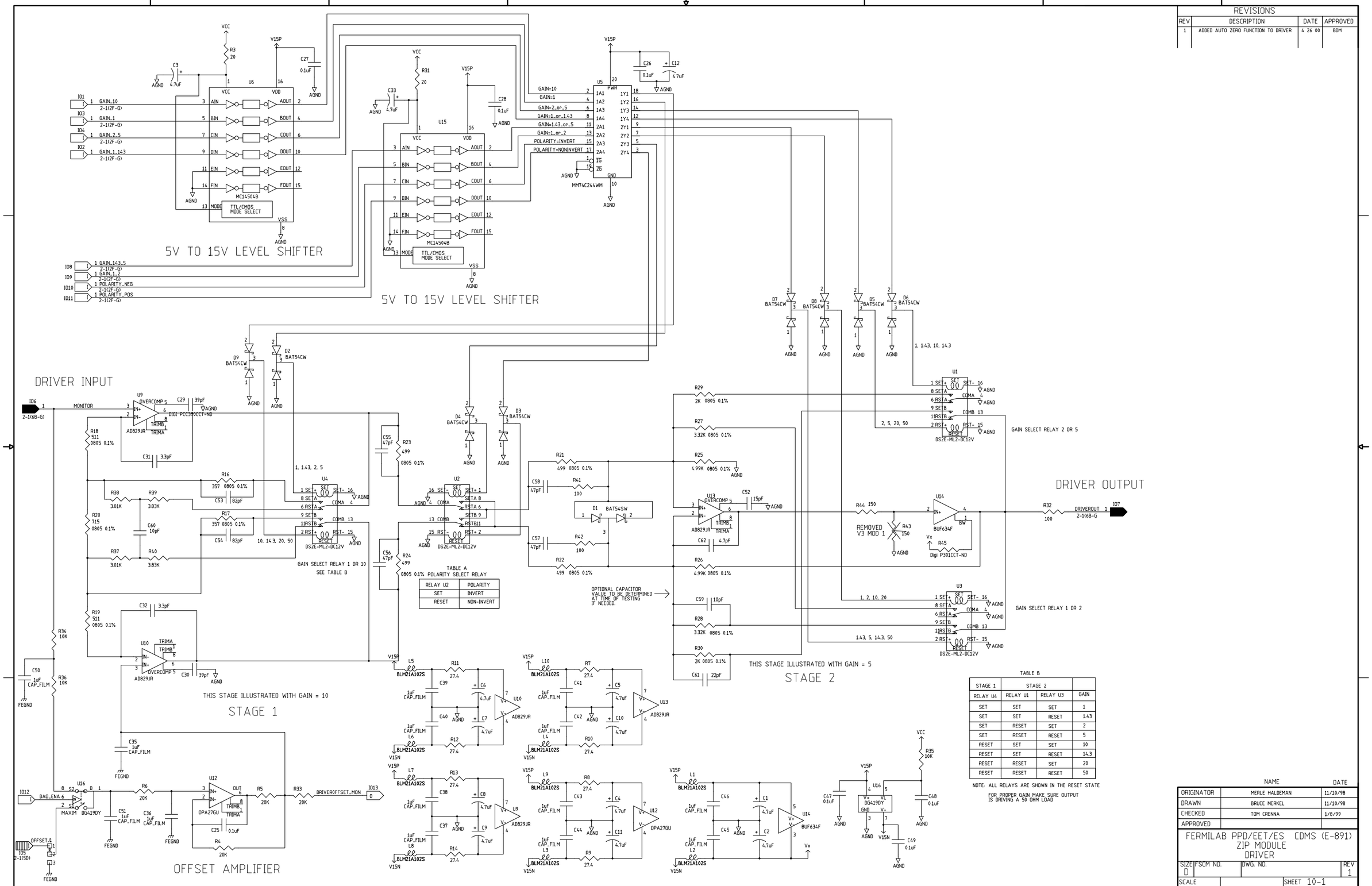


TABLE A POLARITY SELECT RELAY

RELAY U2	POLARITY
SET	INVERT
RESET	NON-INVERT

TABLE B

STAGE 1	STAGE 2		
RELAY U4	RELAY U1	RELAY U3	GAIN
SET	SET	SET	1
SET	SET	RESET	1.43
SET	RESET	SET	2
SET	RESET	RESET	5
RESET	SET	SET	10
RESET	SET	RESET	14.3
RESET	RESET	SET	20
RESET	RESET	RESET	50

NOTE: ALL RELAYS ARE SHOWN IN THE RESET STATE

FOR PROPER GAIN MAKE SURE OUTPUT IS DRIVING A 50 OHM LOAD

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
1	ADDED AUTO ZERO FUNCTION TO DRIVER	4 26 00	BDM

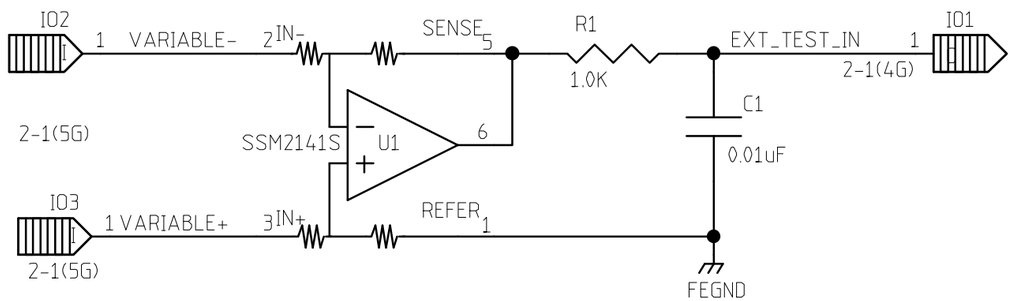
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/10/98
DRAWN	BRUCE MERKEL	11/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

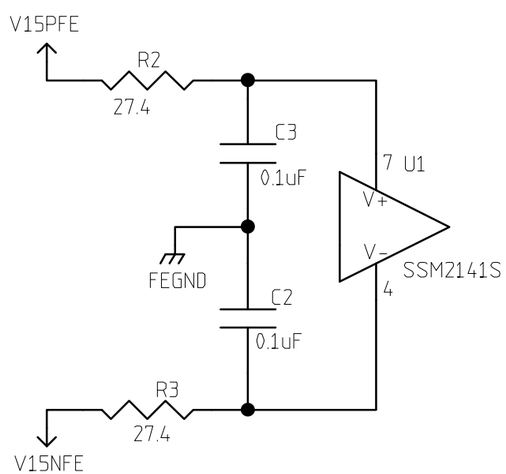
FERMILAB PPD/EET/ES CDMS (E-891)
ZIP MODULE
DRIVER

SIZE D | FSCM NO. | DWG. NO. | REV 1

SCALE | SHEET 10-1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





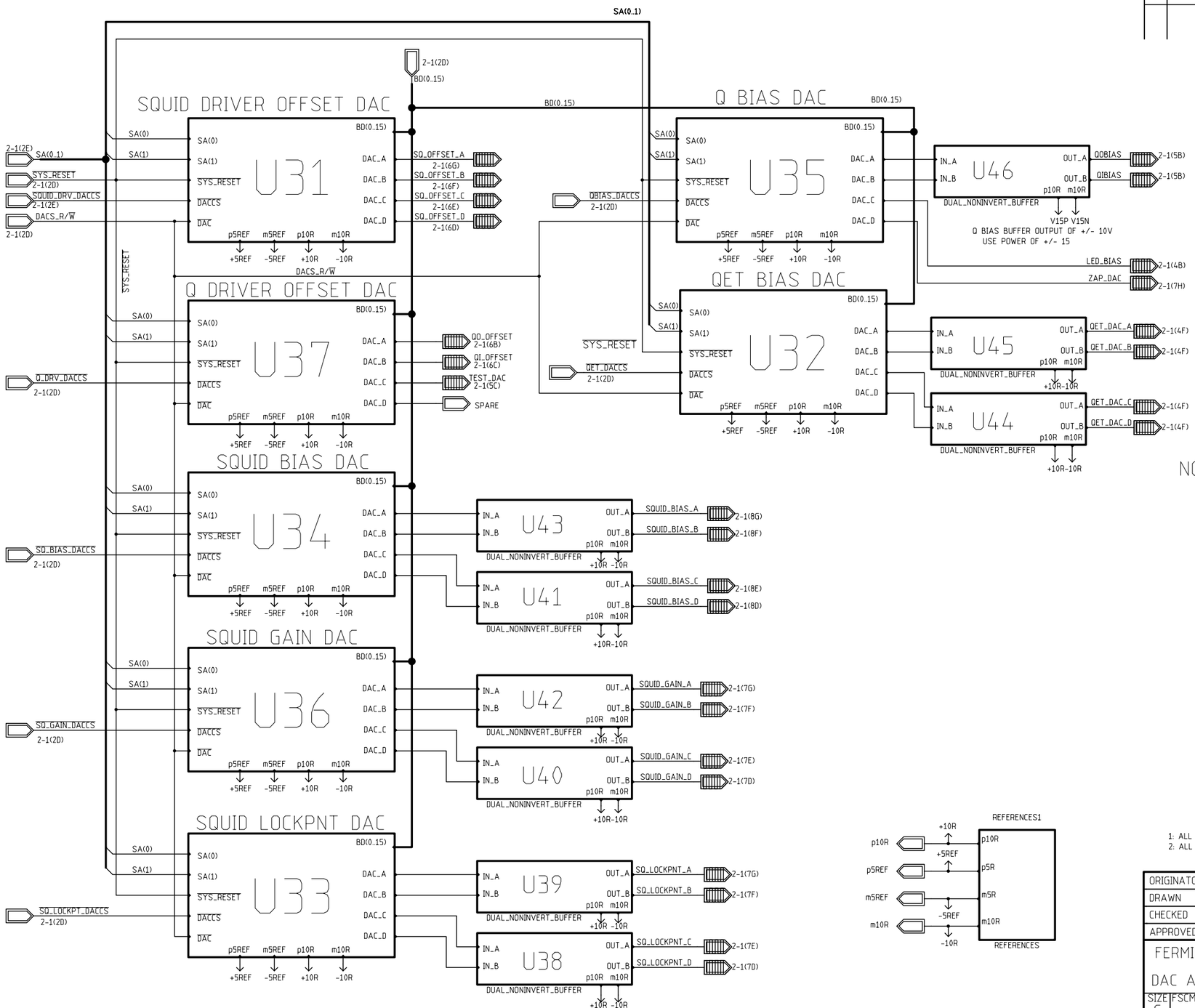
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
EXTERNAL TEST RECEIVER

SIZE	FSCM NO.	DWG. NO.	REV
A			

SCALE | SHEET 11-1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



NOTE: ALL BUFFERS ARE NON-INVERTING

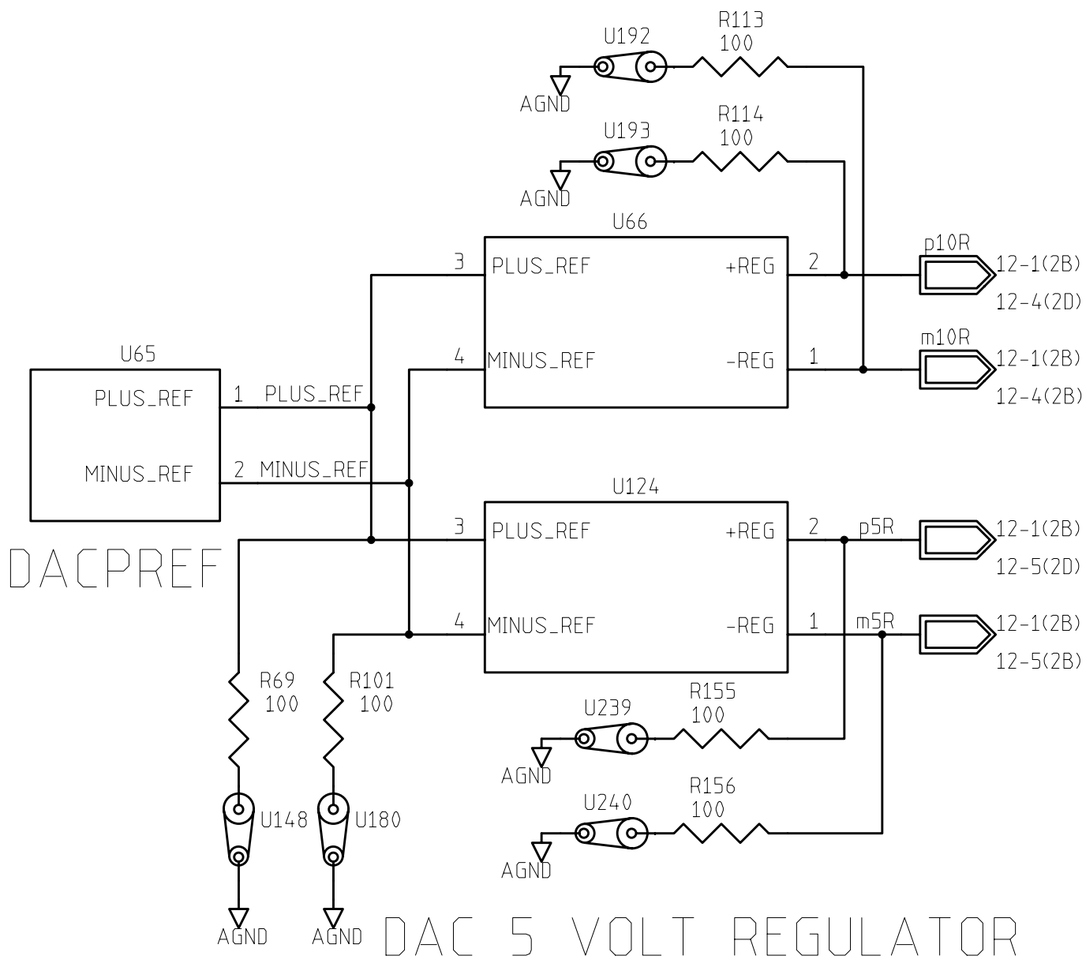
1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
DAC AND BUFFERS BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 12-1	

DAC 10 VOLT REGULATOR



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDER DEVELOPMENT	1-19-99	

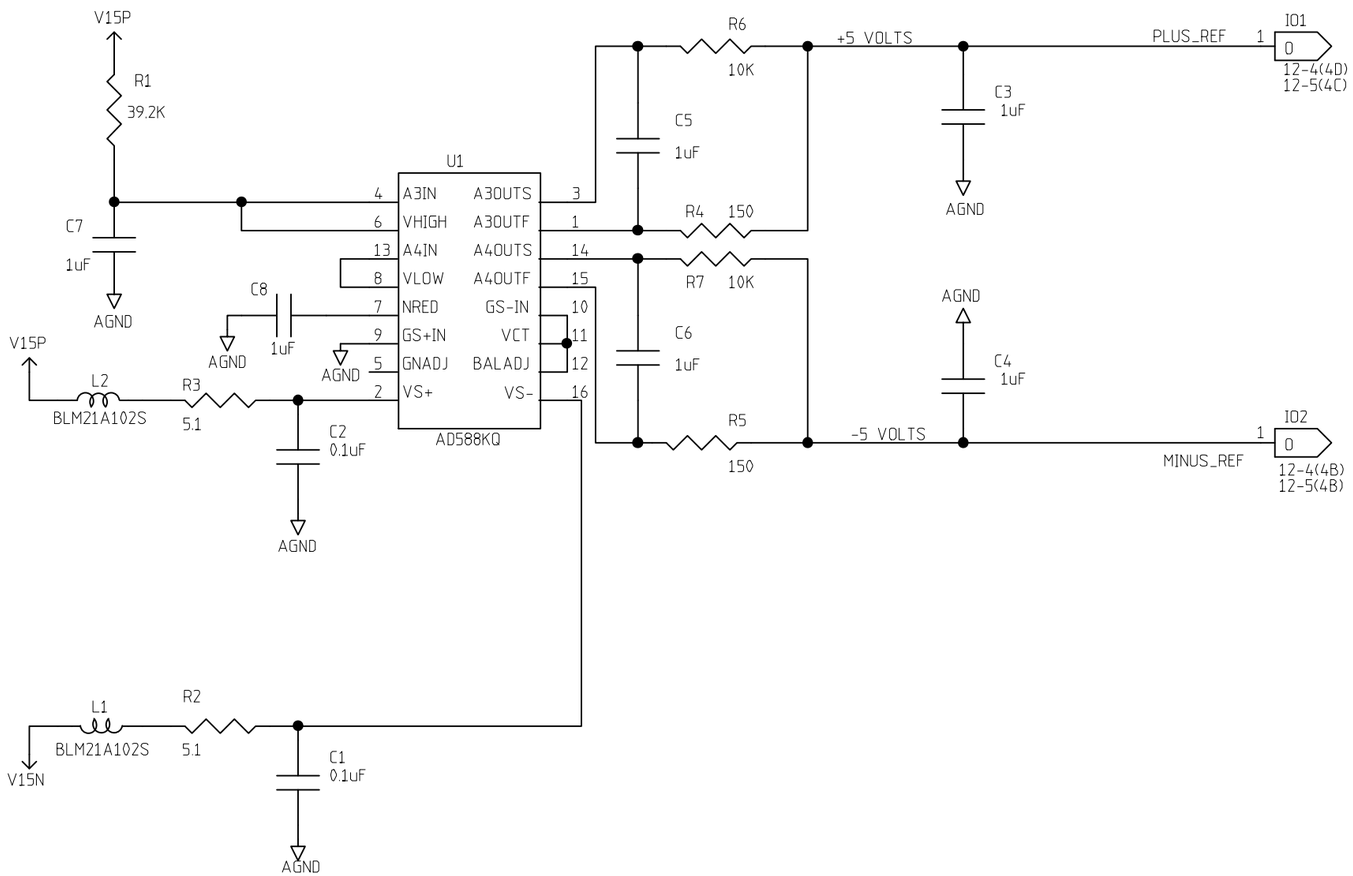
1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC REFERENCES

SIZE	FSCM NO.	DWG. NO.	REV
A			
SCALE		SHEET 12-2	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



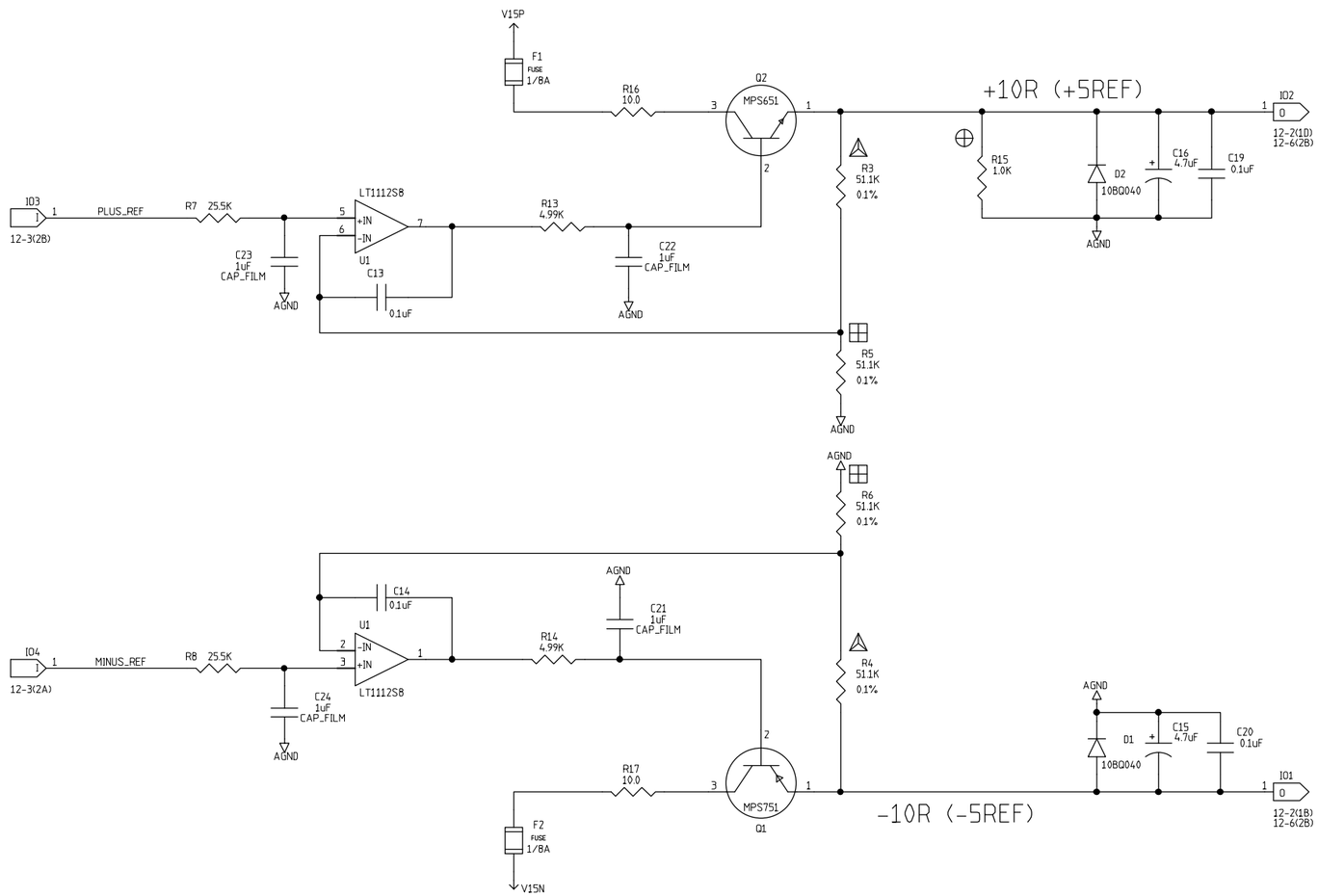
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	12/01/98
DRAWN	BRUCE MERKEL	12/01/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

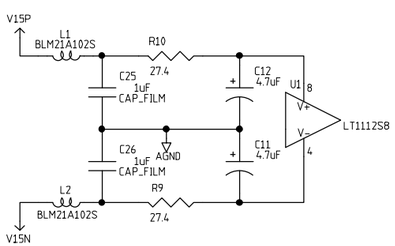
FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC PRECISION REFERENCE

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 12-3

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	USE FOR BOTH 10 & 5 VOLT REFERENCE	3/23/99	B MERKEL
1	replaced regulators with transistors	4/11/00	B MERKEL





RESISTANCE CHART FOR STUFFING THE DAC REGULATORS

SYMBOL	+5 VOLT	- 5 VOLT	+10 VOLT	-10 VOLT
⊕	1K OHM	N.U.	N.U.	N.U.
△	25.5K OHM	25.5K OHM	51.1K OHM	51.1K OHM
⊞	N.U.	N.U.	51.1K OHM	51.1K OHM

N.U. = NOT USED

NOTES:

1: ALL RESISTORS ARE 1% UNLESS OTHERWISE SPECIFIED

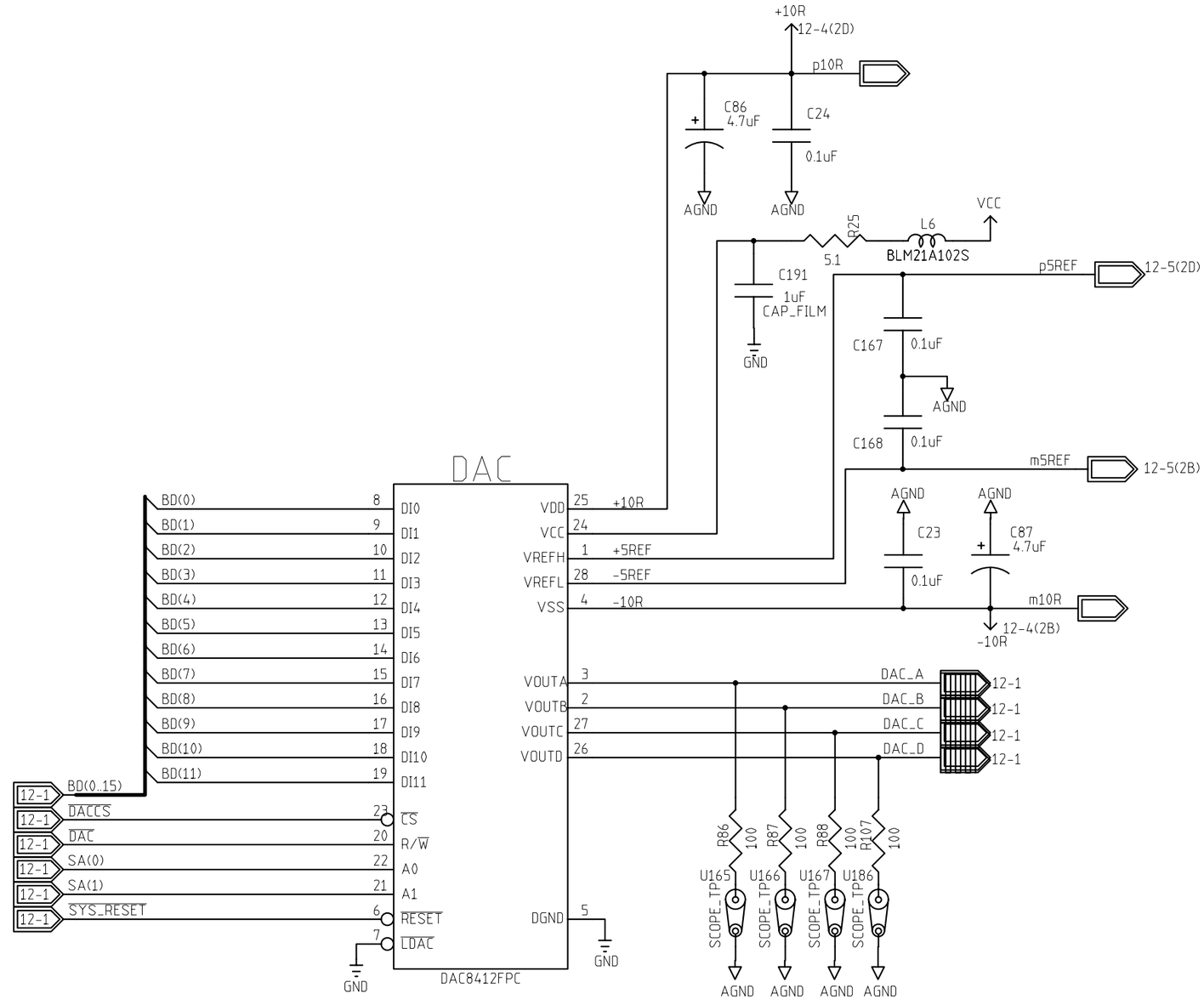
2: ALL LOGIC STATEMENTS ARE HIGH TRUE

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	12/01/98
DRAWN	BRUCE MERKEL	04/11/00
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC +/- VOLTAGE REFERENCES

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 12-4	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
	UNDER DEVELOPMENT	1-19-99	



1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

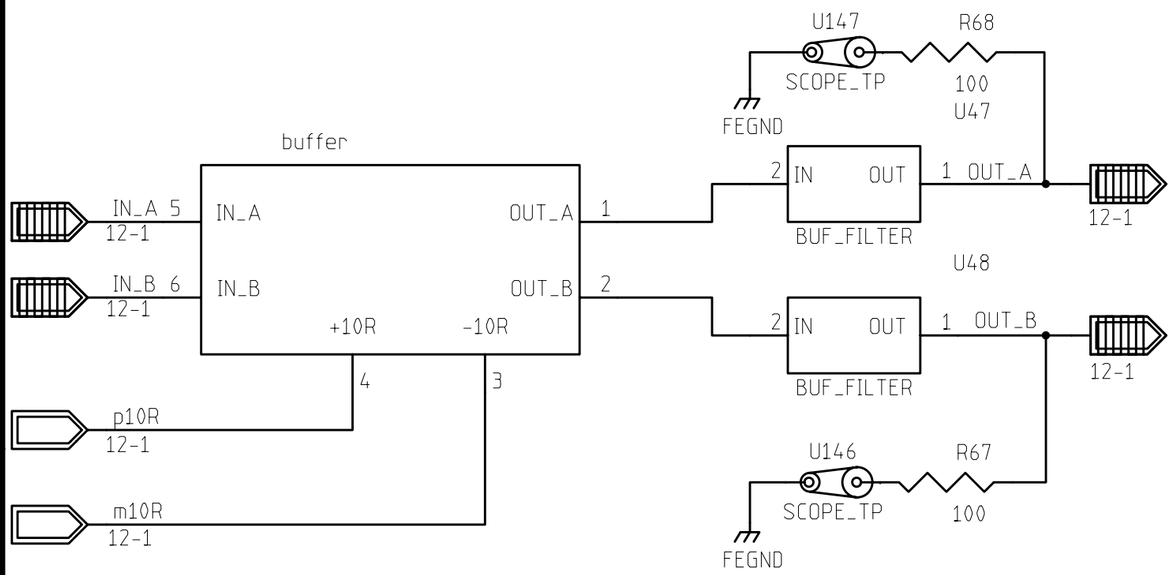
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC'S_1_TO_7

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 12-6	

U35

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

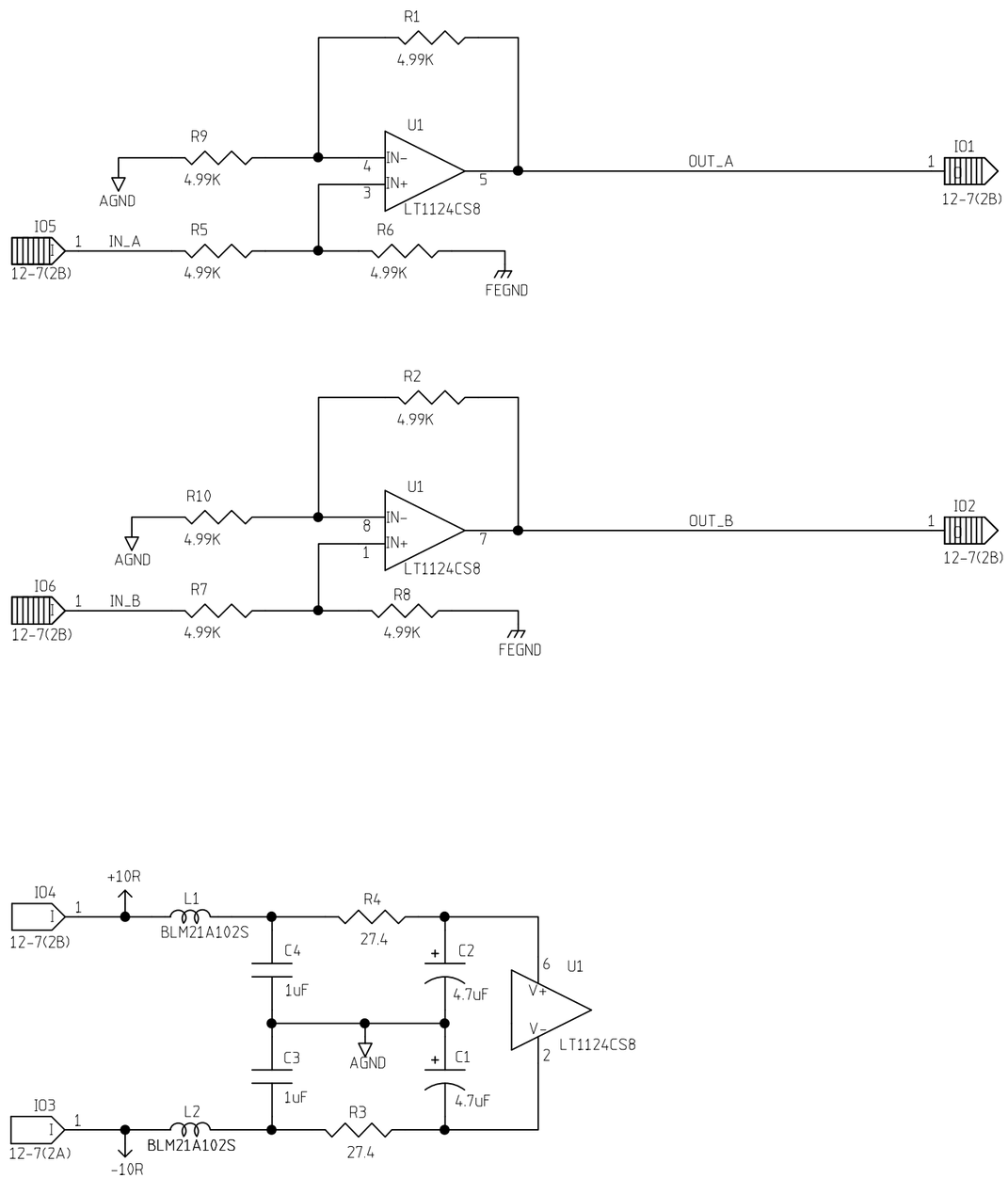
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1
SCALE		SHEET 12-7	

U46

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



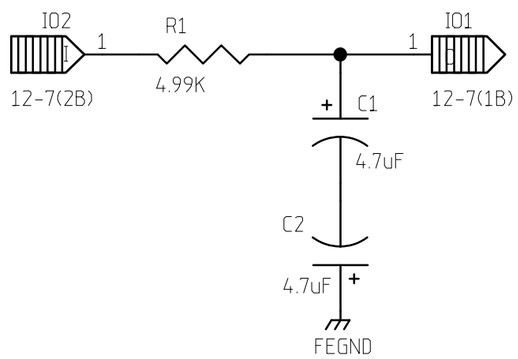
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
DUAL NON-INVERTING BUFFERS

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 12-8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

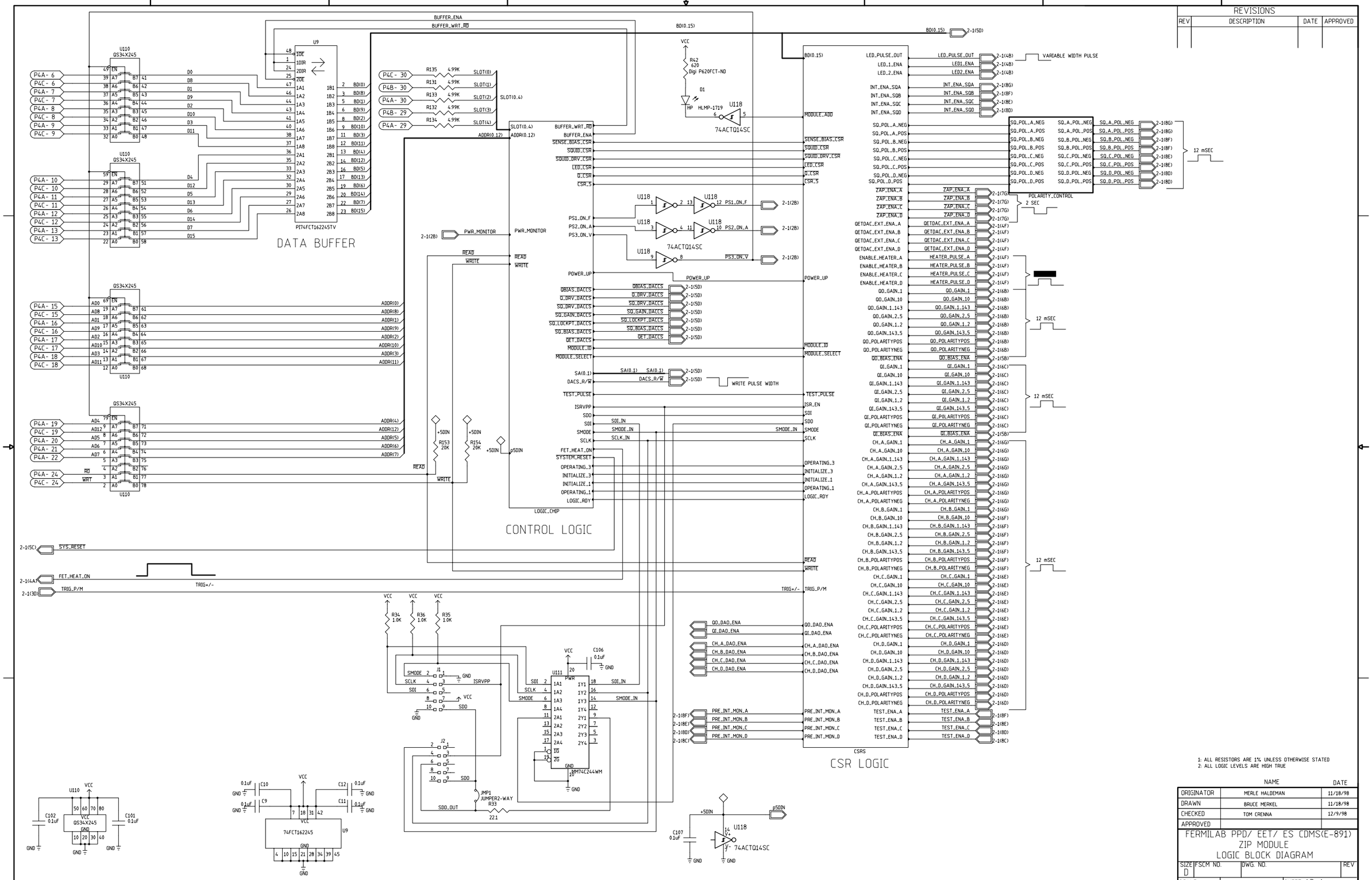


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	12/09/98
DRAWN	BRUCE MERKEL	12/09/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
BUFFER FILTER

SIZE	FSCM NO.	DWG. NO.	REV
A			

SCALE		SHEET 12-9



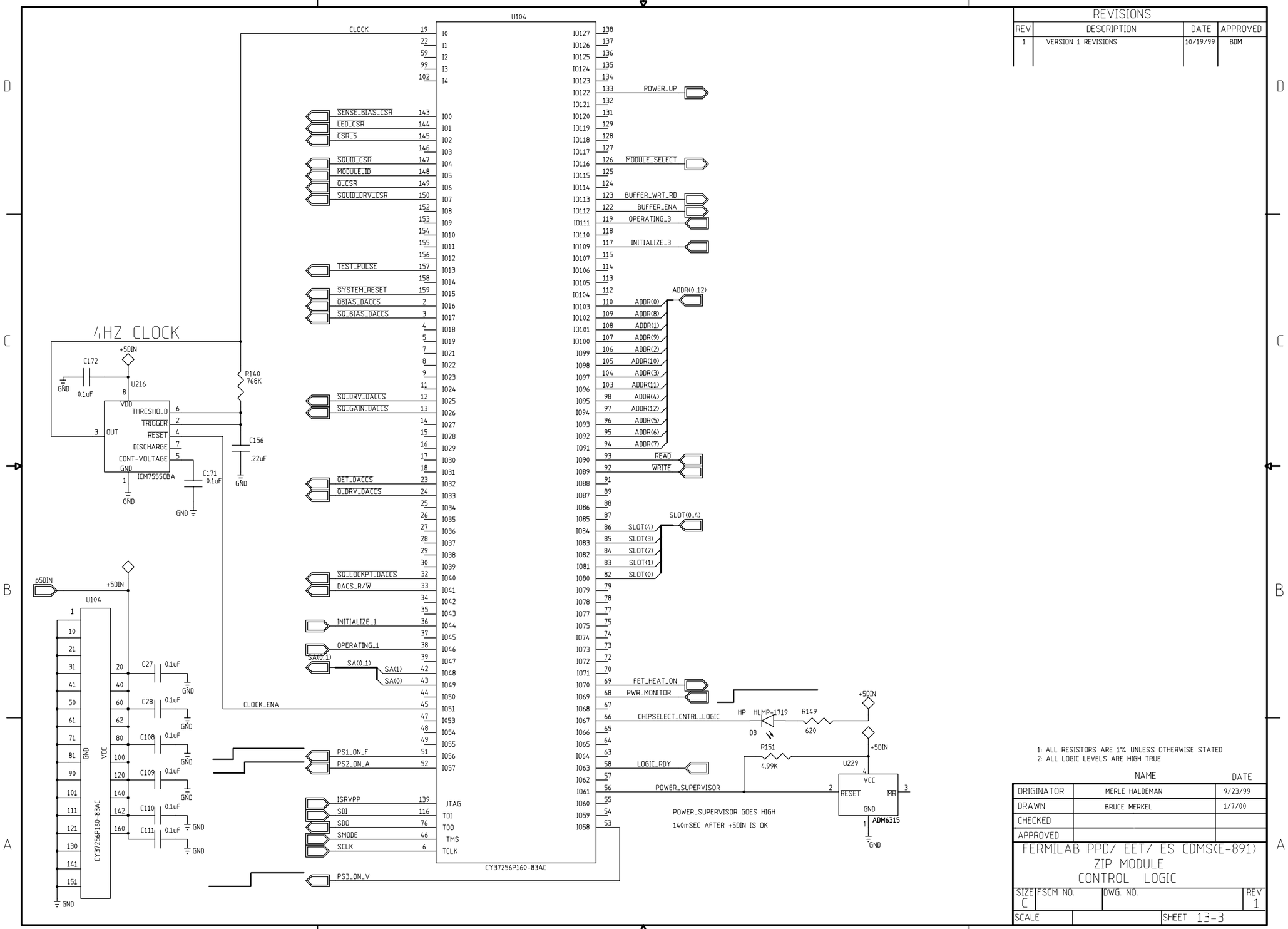
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	12/9/98
APPROVED		

FERMILAB PPD/ EET/ ES CDMS(E-891)
ZIP MODULE
LOGIC BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
D			
SCALE		SHEET 13-1	



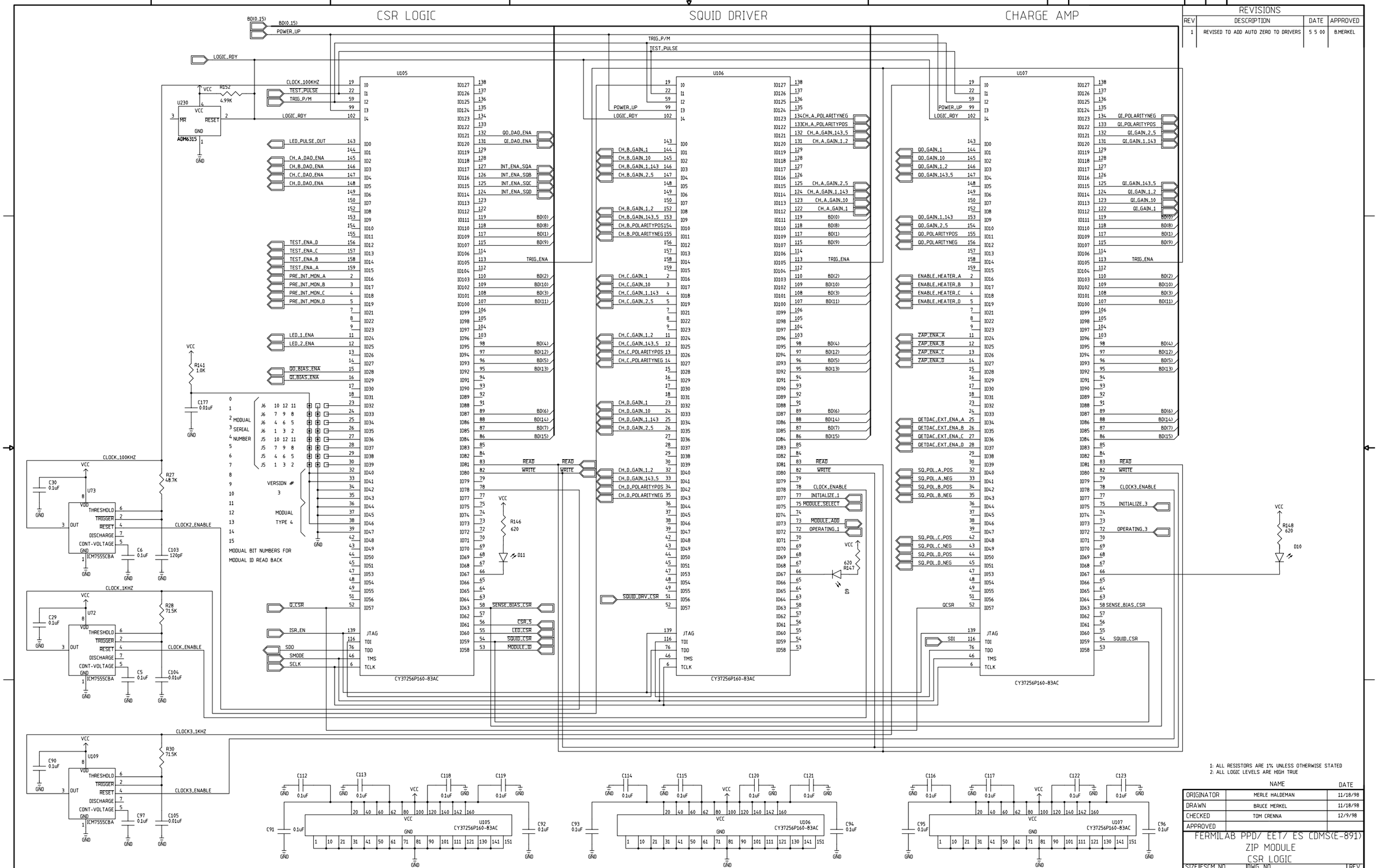
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	VERSION 1 REVISIONS	10/19/99	BDM

1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	9/23/99
DRAWN	BRUCE MERKEL	1/7/00
CHECKED		
APPROVED		

FERMILAB PPD/ EET/ ES CDMS(E-891)
ZIP MODULE
CONTROL LOGIC

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 13-3	



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	REVISED TO ADD AUTO ZERO TO DRIVERS	5 5 00	B.MERKEL

1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

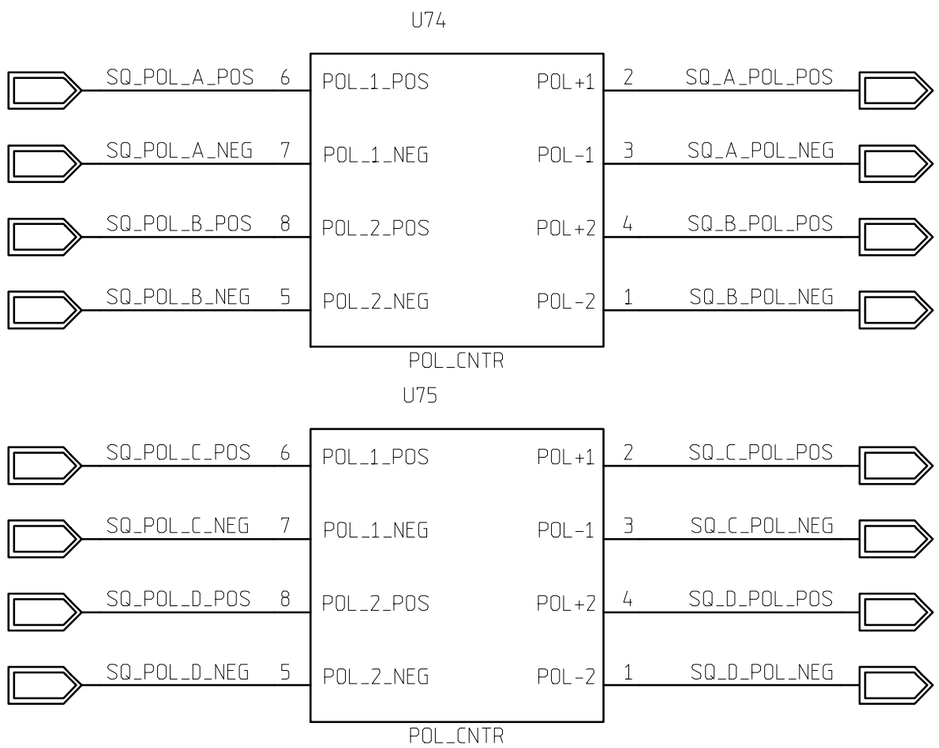
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	12/9/98
APPROVED		

FERMILAB PPD/ EET/ ES CDMS(E-891)
ZIP MODULE
CSR LOGIC

SIZE D | FSCM NO. | DWG. NO. | REV 1
SCALE | SHEET 13-4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDER DEVELOPMENT	1-20-99	

11mSEC ONE SHOT



	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
POLARITY CONTROL

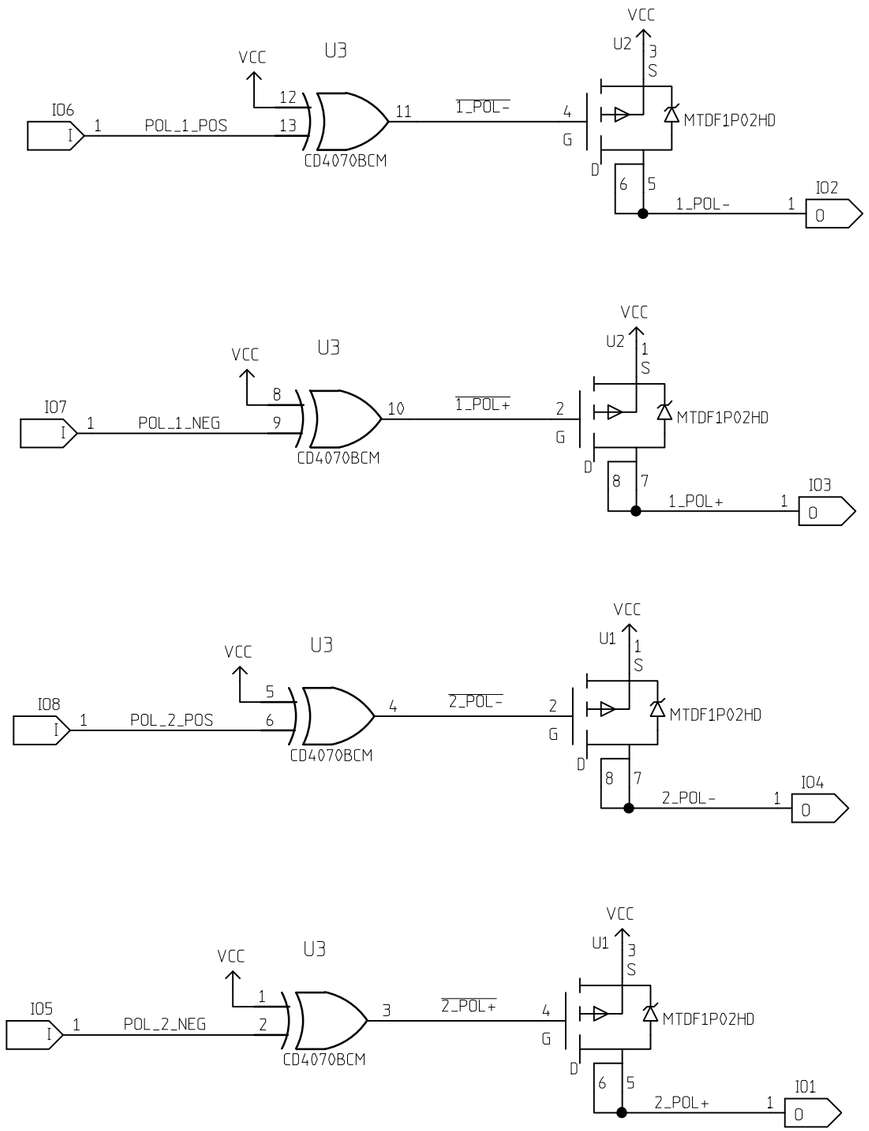
SIZE	FSCM NO.	DWG. NO.	REV
A			1

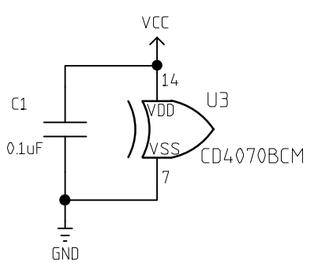
SCALE | SHEET 13-5

DWG. NO.	SH.	REV

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDER DEVELOPMENT	1-20-99	

11mSEC PULSE

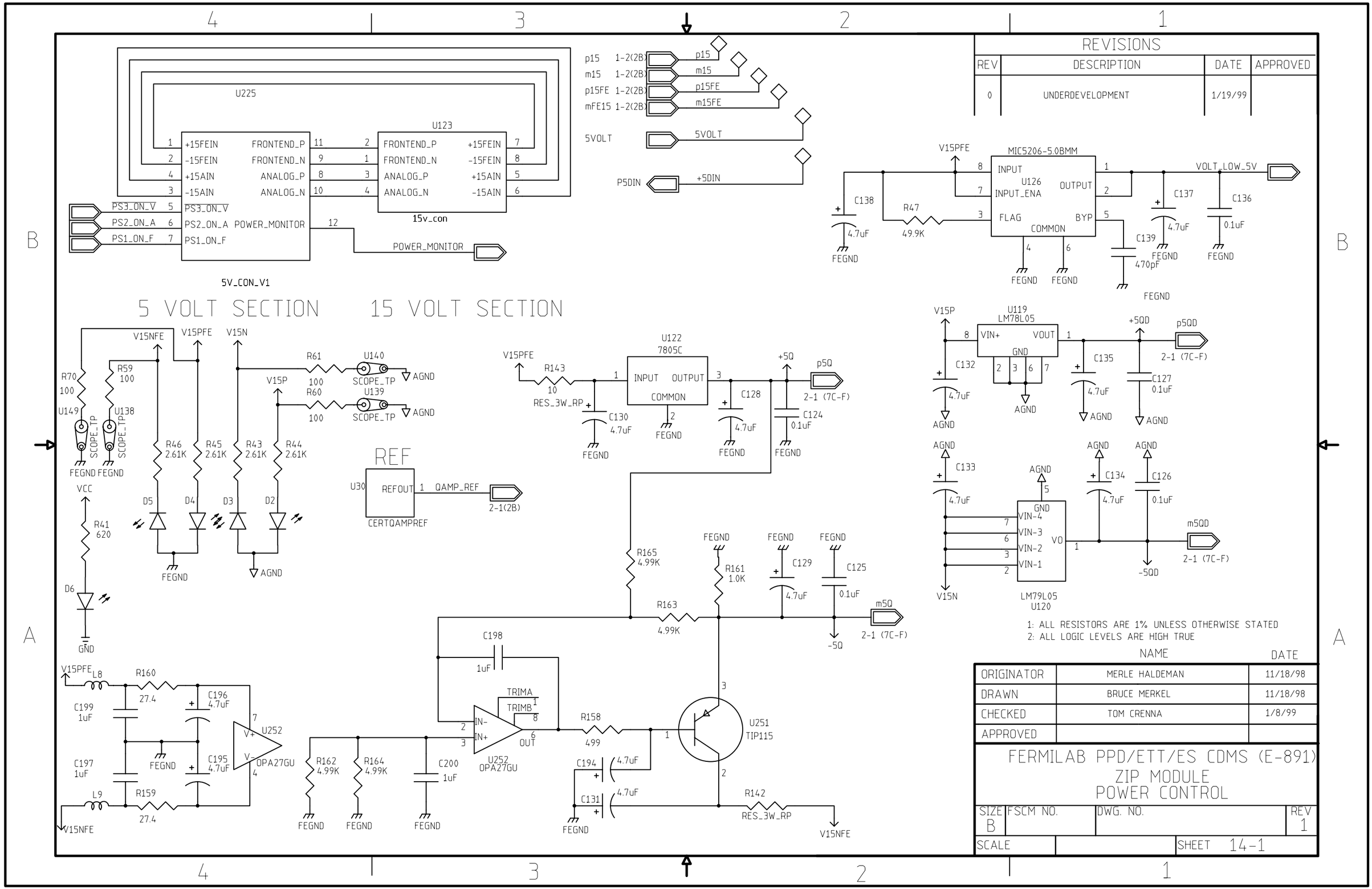




	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
POLARITY CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 13-5	



1: ALL RESISTORS ARE 1% UNLESS OTHERWISE STATED
2: ALL LOGIC LEVELS ARE HIGH TRUE

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDERDEVELOPMENT	1/19/99	

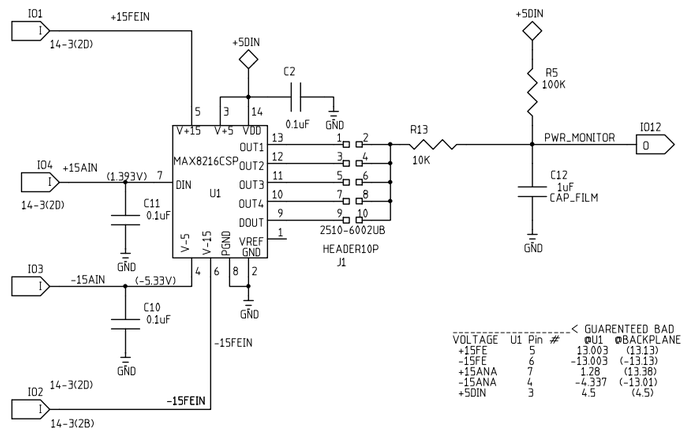
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
POWER CONTROL

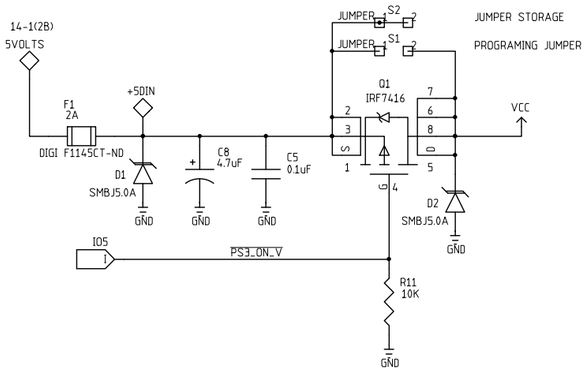
SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 14-1	

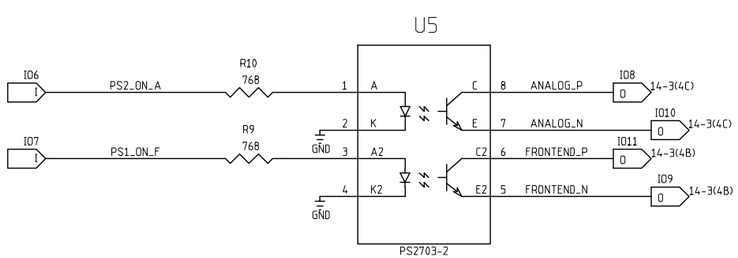
POWER ON SEQUENCER

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



VOLTAGE	U1 Pin #	< GUARENTEED BAD ⊕U1	⊕BACKPLANE	> GUARENTEED GOOD ⊕U1	⊕BACKPLANE	EXPECTED ⊕U1	MEASURED ⊕BACKPLANE
+15FE	5	13.003	(13.13)	13.467	(13.6)	14.82	(15)
-15FE	6	-13.003	(-13.13)	-13.467	(-13.6)	-14.82	(-15)
+15ANA	7	1.28	(13.38)	1.262	(13.87)	1.37	(15)
-15ANA	4	-4.337	(-13.01)	-4.493	(-13.47)	-5.002	(-15)
+5DIN	3	4.5	(4.5)	4.657	(4.657)	5.0	(5.0)





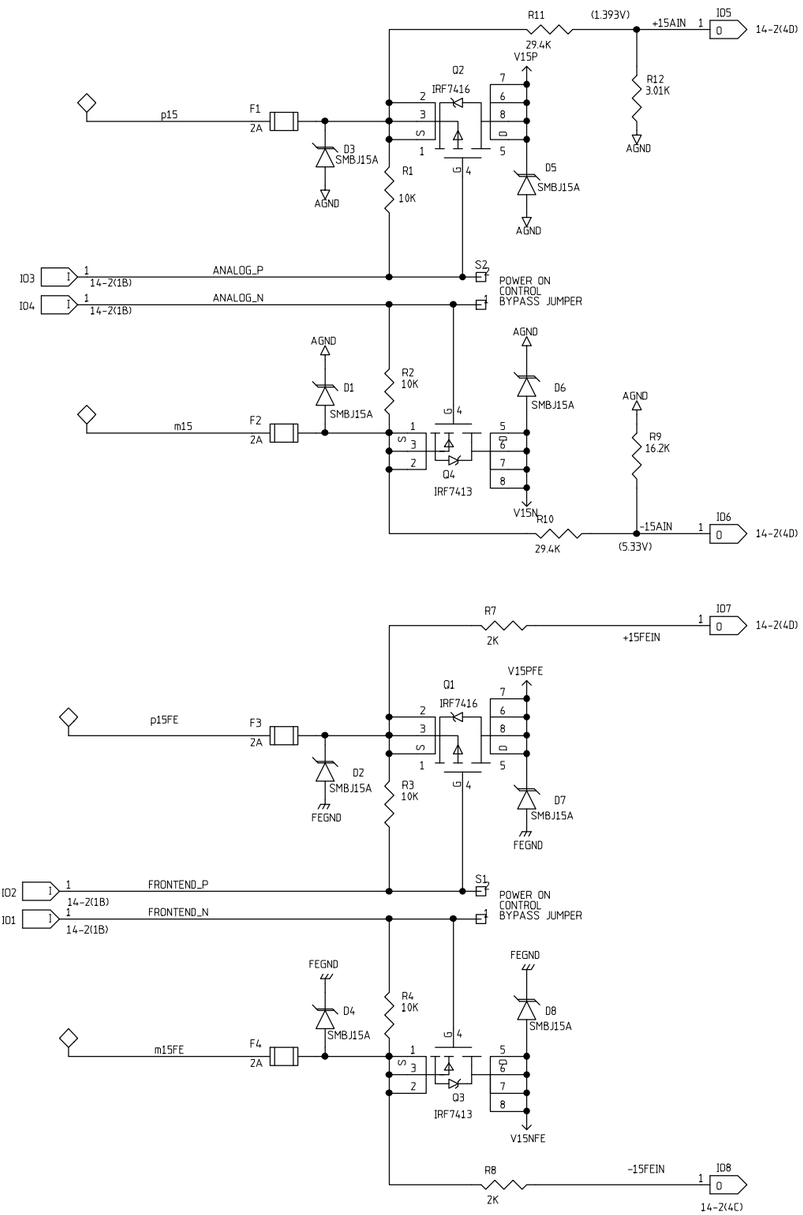
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
5 VOLT SECTION

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 14-2	

POWER ON SEQUENCER CONTINUED

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
15 VOLT SECTION

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 14-3	

This file is named Backplane Pinout.xls
and can be found at
Network Neighborhood\Ppdserver1\ETT.PPD\PROJECTS\Ett_ES\CDMS\crates\9U

50 Pin D Connector
Detector I/O
Slots 1 thru 9, and
12 thru 20
[Crate Front View]

J1

Pin #		Pin #		Pin #	
50	Qi Feedback			17	FEGND
		33	FEGND		
49	FET Temp+			16	Qi Drain
		32	FEGND		
48	FEGND			15	Qi Bias
		31	Qi Source		
47	FEGND			14	FEGND
		30	Qo Feedback		
46	FET Heater-			13	FEGND
		29	FEGND		
45	FET Heater +			12	Qo Drain
		28	FEGND		
44	FEGND			11	Qo Bias
		27	Qo Source		
43	FEGND			10	FEGND
		26	LED 2		
42	LED 1			9	FEGND
		25	FEGND		
41	FBout C			8	SQUID Bias C
		24	FEGND		
40	FEGND			7	QET Bias C
		23	SQUID Bias D		
39	FEGND			6	FEGND
		22	Fbout D		
38	QET Bias D			5	FEGND
		21	FEGND		
37	FBout A			4	SQUID Bias A
		20	FEGND		
36	FEGND			3	QET Bias A
		19	SQUID Bias B		
35	QET Bias B			2	FBout B
		18	FEGND		
34	FEGND			1	FEGND

The backplane connector is
part # AMP 205211-2

The mating connector on the
module is part # AMP 745355-4

This ZIP connector will be mounted to a brass plate
that is machined to match the backplane connector

48 Pin DIN Connector
Crate Power
Slots 1 thru 21
[Crate Front View]

J2

Pin #	Row A	Row B	Row C
1	FEGND	Aux Heater Power+	FEGND
2	FEGND	Aux Heater Power-	FEGND
3	FE +15	FE +15	FE +15
4	FEGND	FEGND	FEGND
5	FE -15	FE -15	FE -15
6	FEGND	FEGND	FEGND
7	FEGND	FEGND	FEGND
8	AGND	AGND	AGND
9	A15+	A15+	A15+
10	AGND	AGND	AGND
11	A15-	A15-	A15-
12	AGND	AGND	AGND
13	10Hz+	AGND	VARIABLE+
14	10Hz-	AGND	VARIABLE-
15	1kHz+	**Spare**	Trig+
16	1kHz-	**Spare**	Trig-

The backplane connector is
part # AMP 535034-4

The mating connector on the
module is part # AMP 650948-5

This connector information is the same for
both the ZIP and RTF modules

25 Pin D Connector
Detector Output
Slots 1 thru 9, and
12 thru 20
[Crate Front View]

J3

Pin #			Pin #
		Spare 3	13
25	AGND		
		SQD offset Mon	12
24	AGND		
		SQC offset Mon	11
23	AGND		
		SQB offset Mon	10
22	AGND		
		SQA offset Mon	9
21	AGND		
		Spare 2	8
20	AGND		
		Spare 1	7
19	AGND		
		SQUID D	6
18	AGND		
		SQUID C	5
17	AGND		
		SQUID B	4
16	AGND		
		SQUID A	3
15	AGND		
		Qo Out	2
14	AGND		
		Qi Out	1

The backplane connector is
part # AMP 207463-1

The mating connector on the
module is part # AMP 745353-4

This ZIP connector is mounted
to a machined cutout in the
backplane.

Slots 1 thru 20
Detector n
(n = 1 through 18)
[Crate Front View]

J4-1

Pin #	Row A	Row B	Row C
1	5 Volts	5 Volts	5 Volts
2	5 Volts	5 Volts	5 Volts
3	5 Volts	5 Volts	5 Volts
4	5 Volts	5 Volts	5 Volts
5	DGND	DGND	DGND
6	D0	DGND	D8
7	D1	DGND	D9
8	D2	DGND	D10
9	D3	DGND	D11
10	D4	DGND	D12
11	D5	DGND	D13
12	D6	DGND	D14
13	D7	DGND	D15
14	DGND	DGND	DGND
15	A 0	DGND	A 8
16	A 1	DGND	A 9
17	A 2	DGND	A 10
18	A 3	DGND	A 11
19	A 4	DGND	A 12
20	A 5	DGND	A 13
21	A 6	DGND	A 14
22	A 7	DGND	A 15
23	DGND	DGND	DGND
24	Read	DGND	Write
25	DGND	DGND	DGND
26	5 Volts	5 Volts	5 Volts
27	5 Volts	5 Volts	5 Volts
28	5 Volts	5 Volts	5 Volts
29	Local Address A4	Local Address A3	5 Volts
30	Local Address A2	Local Address A1	Local Address A0
31	DGND	DGND	DGND
32	Bussed Spare 1	Bussed Spare 2	Sync out

The backplane connector is
part # AMP 535032-4

The mating connector on the
module is part # AMP 650947-5

This connector information is the same for
both the ZIP and RTF modules

Slot 21
GPIB Controller
[Crate Front View]

J4-2

Row A	Row B	Row C	Pin #
spare	5 Volts	Trig1-	1
spare	5 Volts	Trig1+	2
5 Volts	5 Volts	spare	3
5 Volts	5 Volts	spare	4
DGND	DGND	DGND	5
D0	DGND	D8	6
D1	DGND	D9	7
D2	DGND	D10	8
D3	DGND	D11	9
D4	DGND	D12	10
D5	DGND	D13	11
D6	DGND	D14	12
D7	DGND	D15	13
DGND	DGND	DGND	14
A 0	DGND	A 8	15
A 1	DGND	A 9	16
A 2	DGND	A 10	17
A 3	DGND	A 11	18
A 4	DGND	A 12	19
A 5	DGND	A 13	20
A 6	DGND	A 14	21
A 7	DGND	A 15	22
DGND	DGND	DGND	23
Read	DGND	Write	24
DGND	DGND	DGND	25
5 Volts	5 Volts	5 Volts	26
5 Volts	5 Volts	5 Volts	27
5 Volts	5 Volts	5 Volts	28
5 Volts	5 Volts	5 Volts	29
5 Volts	5 Volts	5 Volts	30
DGND	DGND	DGND	31
Bussed Spare 1	Bussed Spare 2	Sync out	32

The backplane connector is
part # AMP 535032-4

The mating connector on the
module is part # AMP 650947-5

This connector information is the same for
both the ZIP and RTF modules

37 Pin D Connector
DC Power Sense
Outputs
[Crate Front View]

J5

Pin #			Pin #
		spare	19
37	spare		
		spare	18
36	spare		
		spare	17
35	spare		
		spare	16
34	spare		
		remote	15
33	remote		
		remote	14
32	remote		
		remote	13
31	HEATER gnd		
		HEATER +	12
30	-15V FE gnd		
		-15V FE	11
29	+15V FE gnd		
		+15V FE	10
28	-15V ANA gnd		
		-15V ANA	9
27	+15V ANA gnd		
		+15V ANA	8
26	Digital gnd		
		Digital +	7
25	HEATER gnd		
		HEATER +	6
24	-15V FE gnd		
		-15V FE	5
23	+15V FE gnd		
		+15V FE	4
22	-15V ANA gnd		
		-15V ANA	3
21	+15V ANA gnd		
		+15V ANA	2
20	Digital gnd		
		Digital +	1

The backplane connector is
part # AMP 207463-1

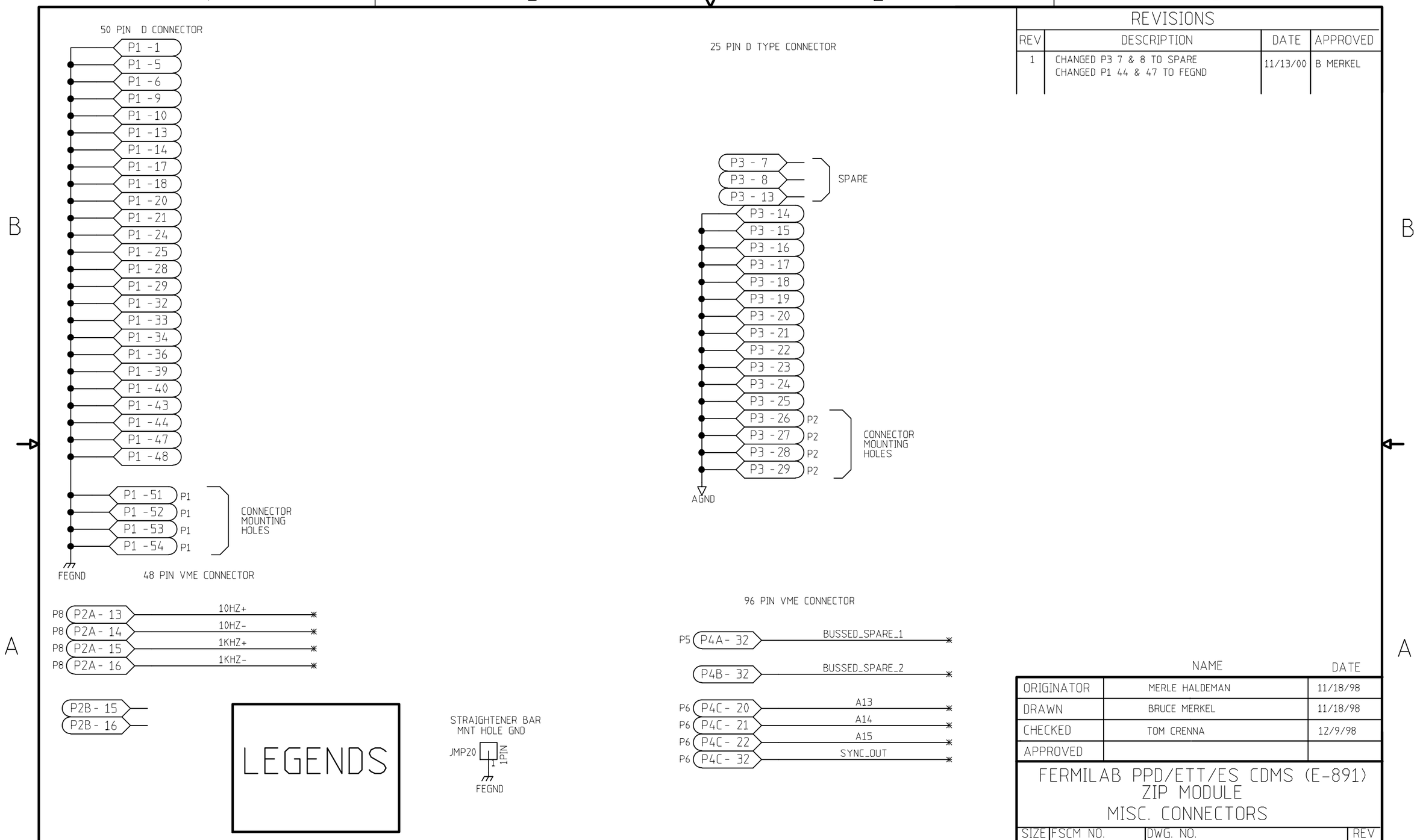
The mating connector on the
module is part # AMP 745353-4

This connector information is the same for
both the ZIP and RTF modules

NOTES;

1	Revision 10/23/97 changed 48 pin contacts C13,C14,C15 and C16
2	Revised view of 50 Pin and 25 Pin connectors to show proper 0rientation on 4/7/99
3	10 Layer Backplane
4	Revision 12/06/00 added the J5 connector information

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	CHANGED P3 7 & 8 TO SPARE CHANGED P1 44 & 47 TO FEGND	11/13/00	B MERKEL

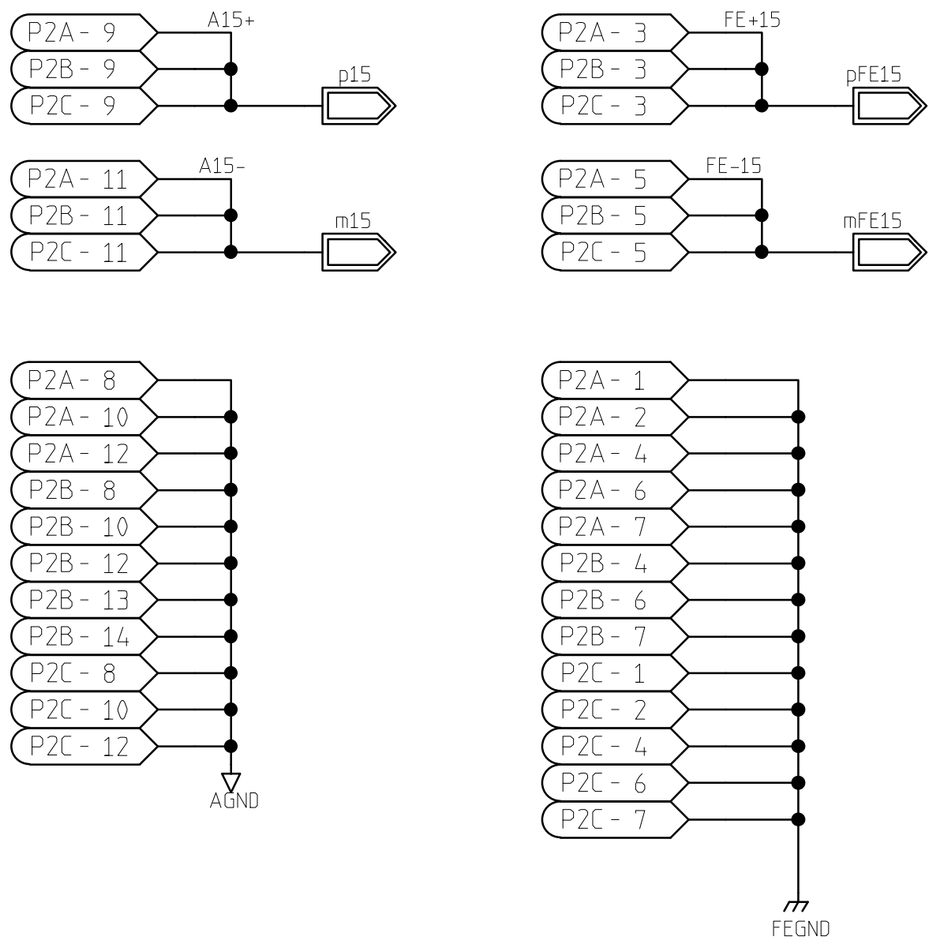


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	12/9/98
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
MISC. CONNECTORS

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 1-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	NAME CHANGE TO MATCH BACKPLANE	7/27/99	BDM



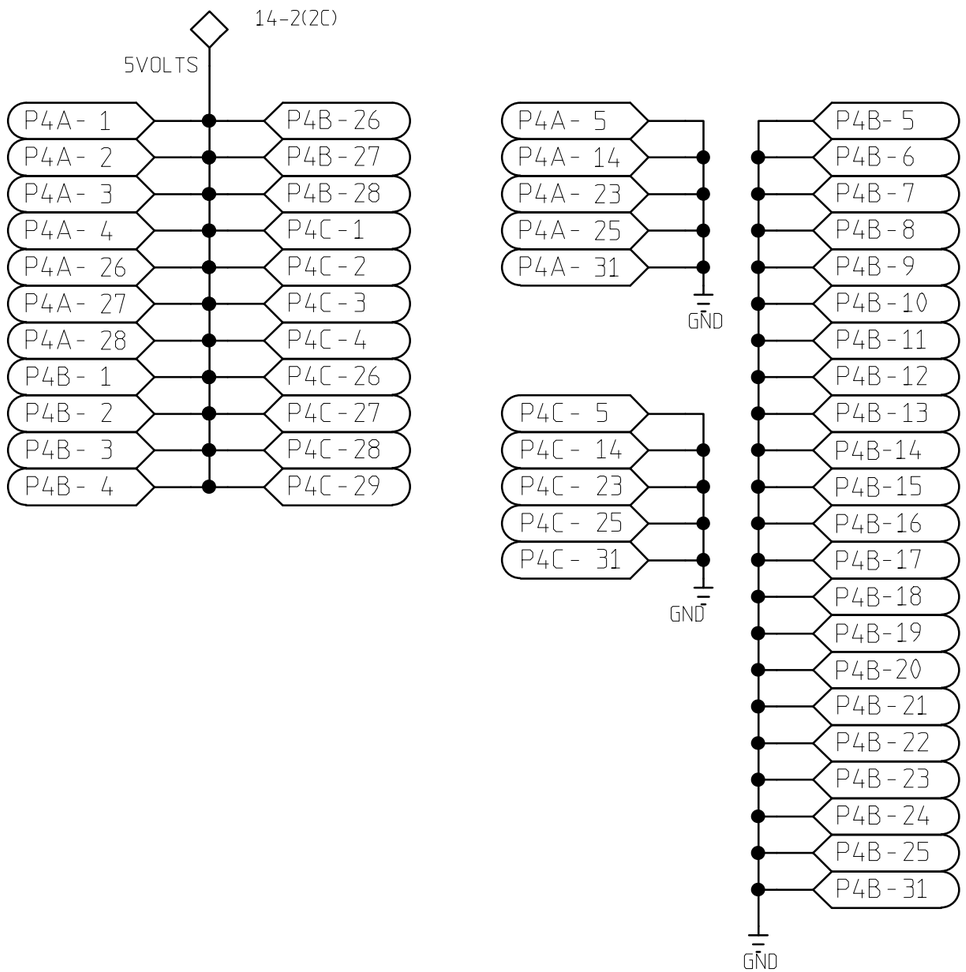
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	10/8/98
DRAWN	BRUCE MERKEL	10/8/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
P2 BACKPLANE POWER CONNECTION

SIZE	FSCM NO.	DWG. NO.	REV
A			

SCALE		SHEET 1-2

P4
(96 PIN CONNECTOR)



REVISIONS

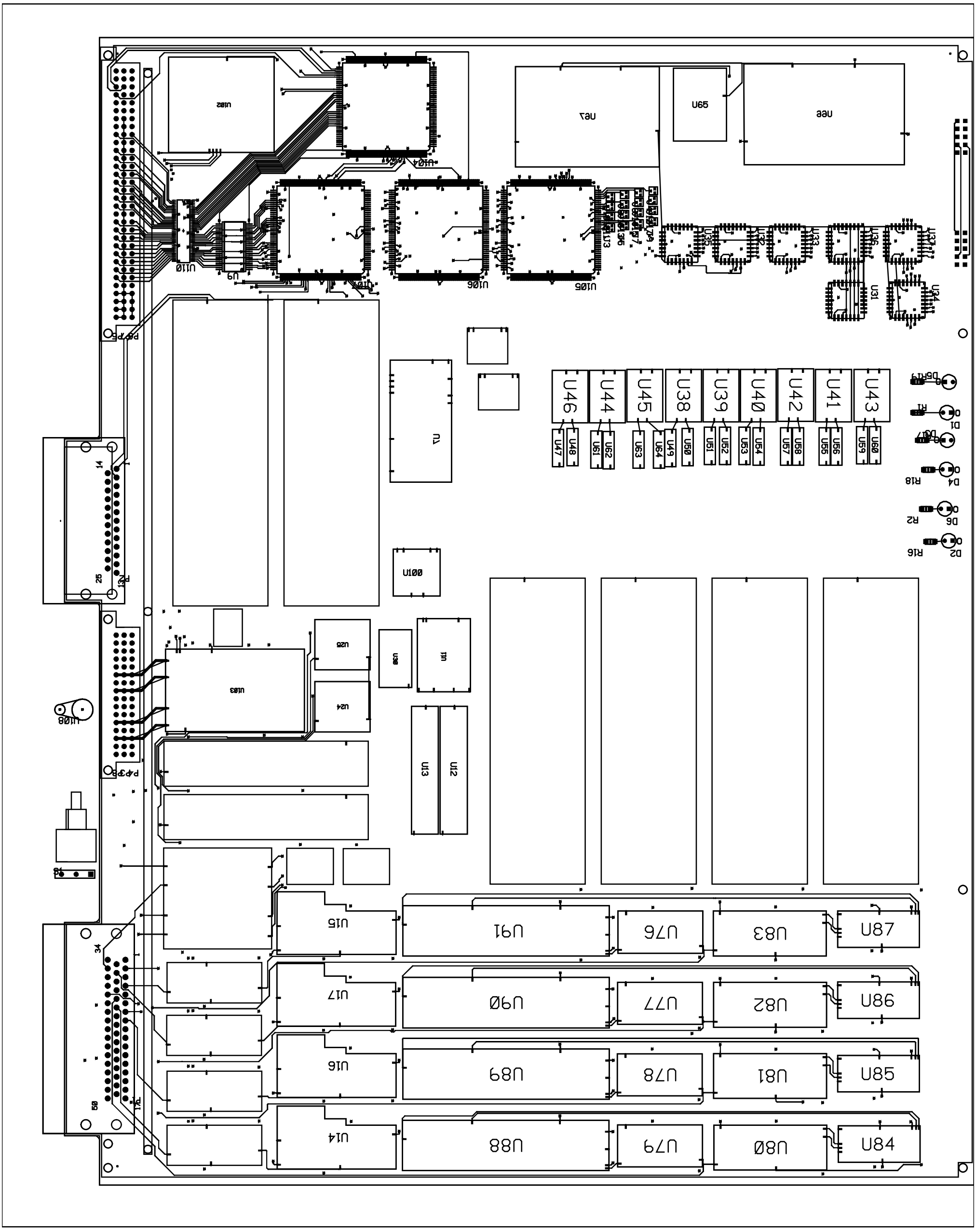
REV	DESCRIPTION	DATE	APPROVED
0	NAME CHANGED TO MATCH BACKPLANE	7/27/99	BDM

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	10/8/98
DRAWN	BRUCE MERKEL	10/8/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
P4 BACKPLANE POWER CONNECTION

SIZE	FSCM NO.	DWG. NO.	REV
A			

SCALE | SHEET 1-3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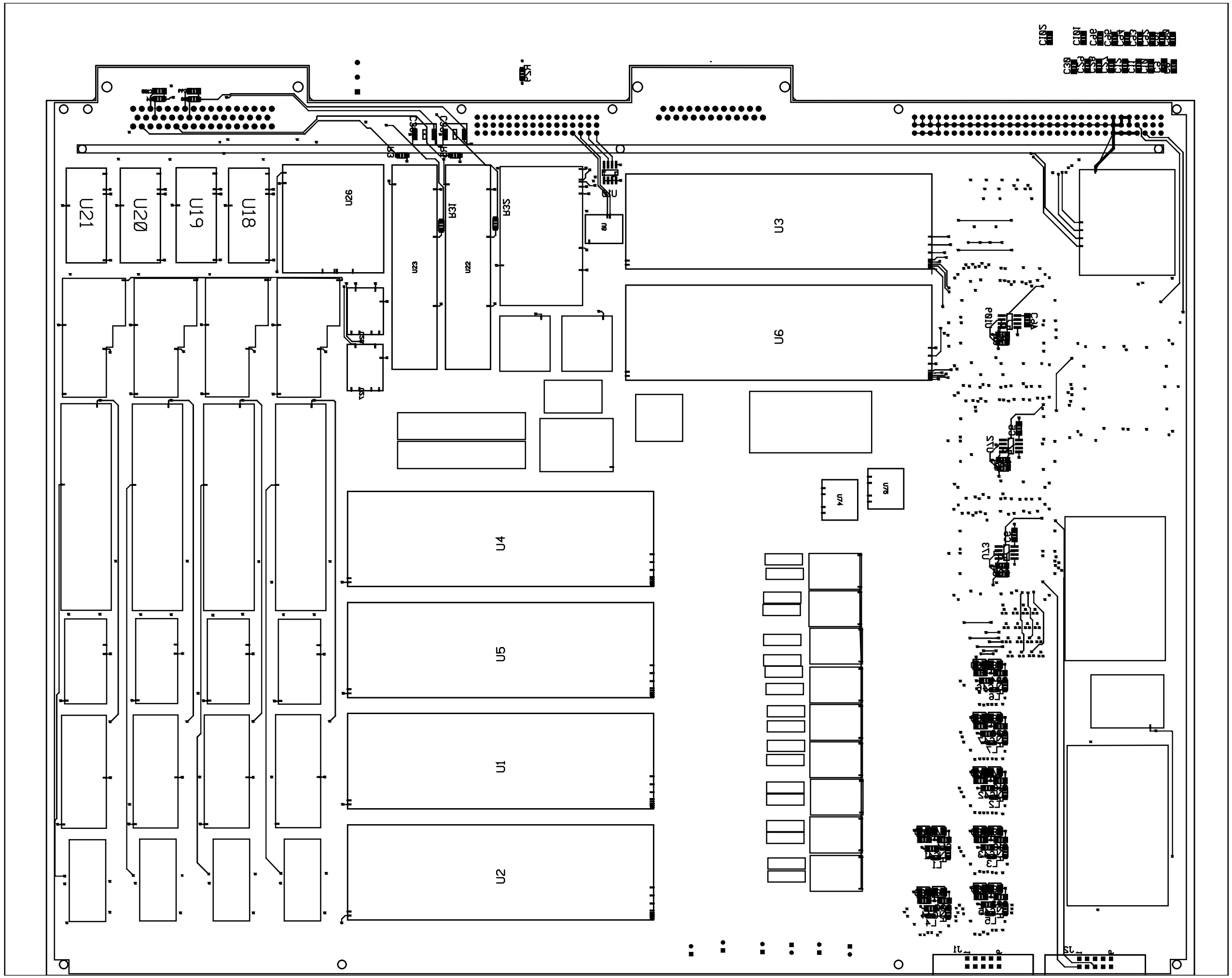
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