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CCD 12 CHANNEL ACQUISITION BOARD
TOP LEVEL SCHEMATIC 12 Channel

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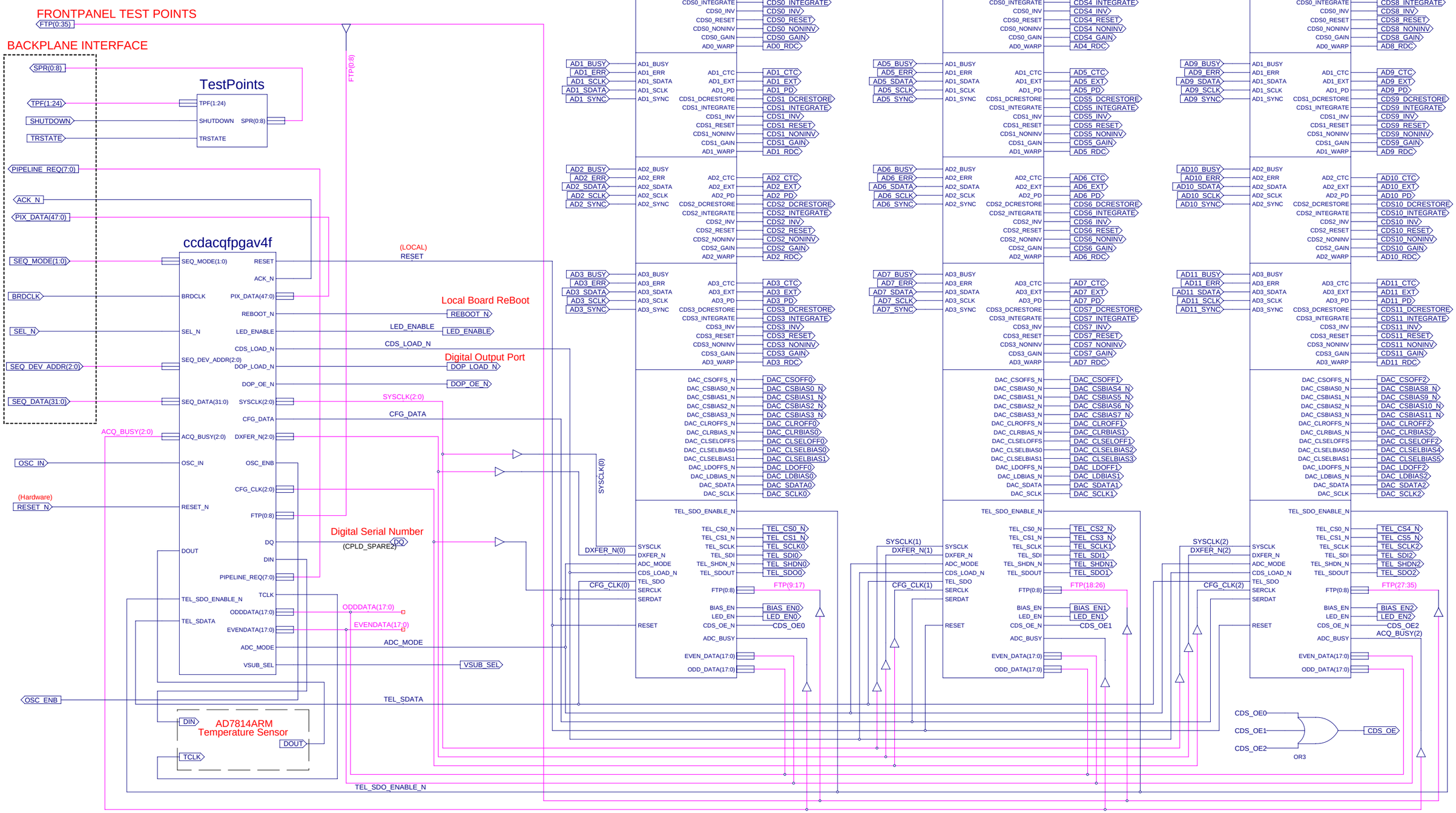
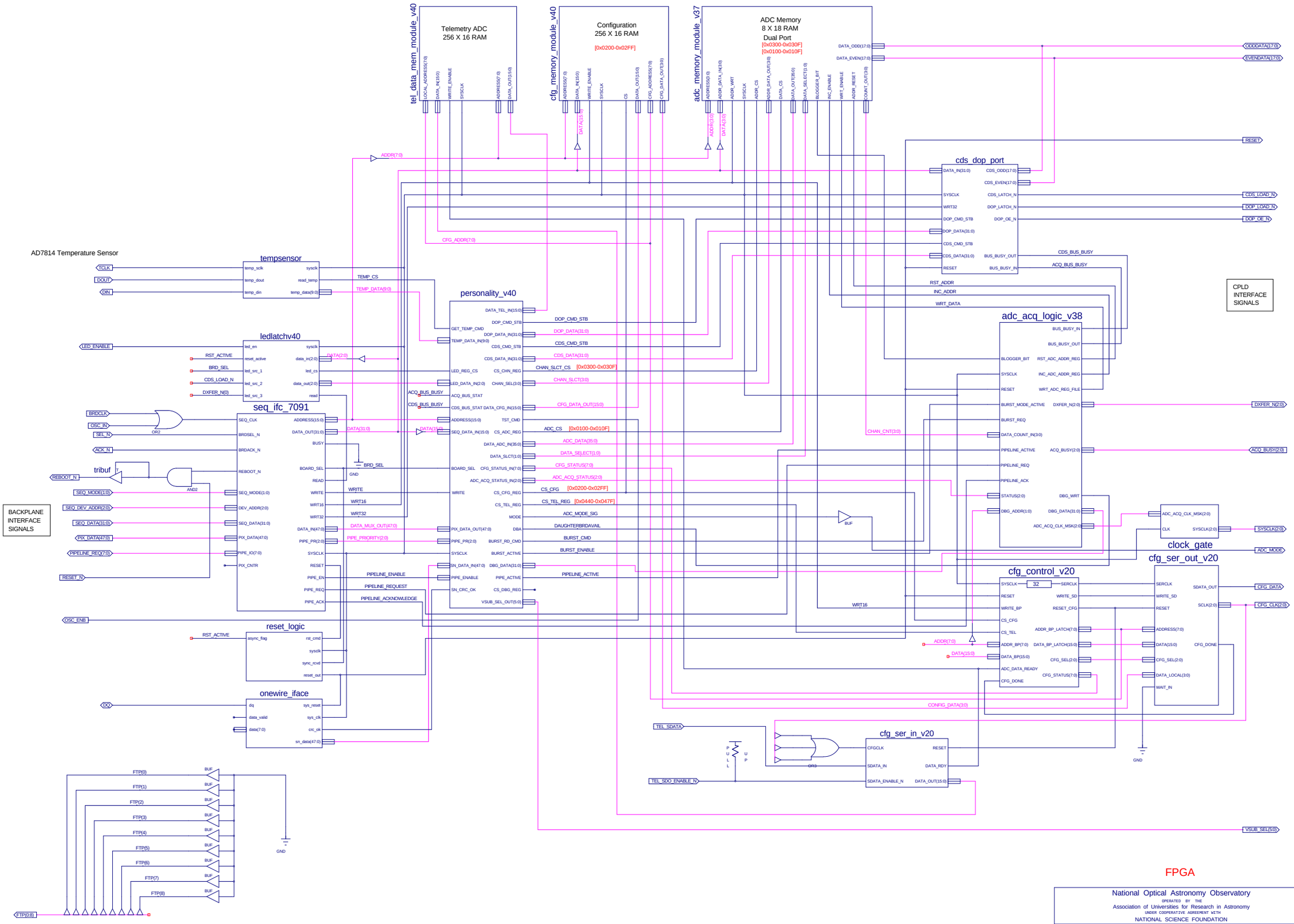
Date: 2006-01-25	Rev 4	Sheet 1 of 1

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Telemetry ADC
256 X 16 RAM
cfg_memory_module_v40
Configuration
256 X 16 RAM
[0x0200-0x02FF]
adc_memory_module_v37
ADC Memory
8 X 18 RAM
Dual Port
[0x0300-0x030F]
[0x0100-0x010F]
cds_dop_port
CPLD
INTERFACE
SIGNALS
AD7814 Temperature Sensor
tempsensor
personality_v40
ledlatchv40
adc_acq_logic_v38
seq_ifc_7091
tribuf
BACKPLANE
INTERFACE
SIGNALS
clock_gate
cfg_ser_out_v20
cfg_control_v20
reset_logic
onewire_iface
cfg_ser_in_v20
FPGA
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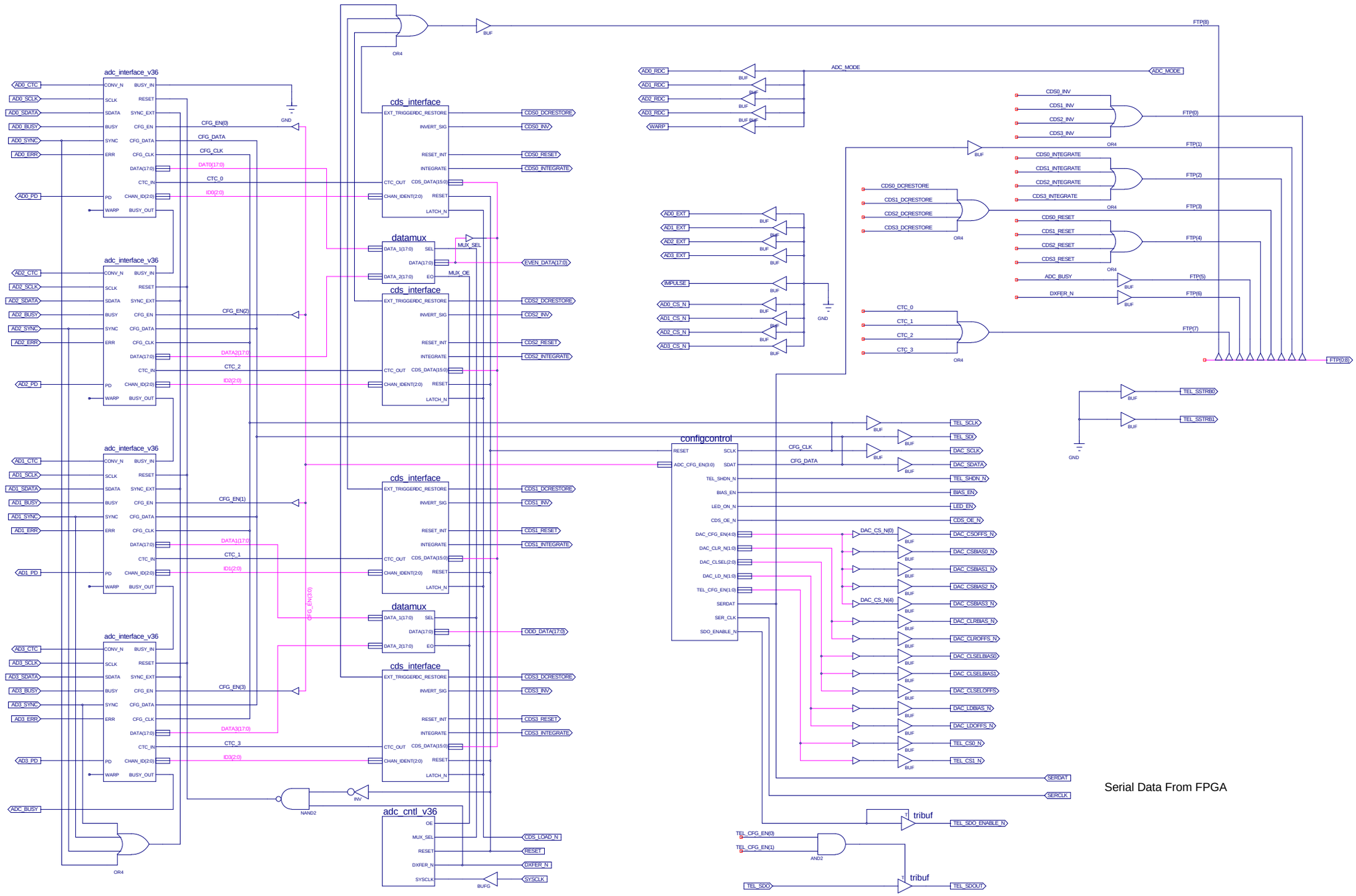
CCD 12 CHANNEL ACQUISITION BOARD FPGA (U62)
TOP LEVEL SCHEMATIC 12 Channel
Dwg No:
Eng: PETER MOORE
Date: 2005-11-04
Rev 3.0
Sheet 1 of 2



Serial Data From FPGA

CPLD

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CCD 12 CHANNEL ACQUISITION BOARD
TOP LEVEL DESIGN

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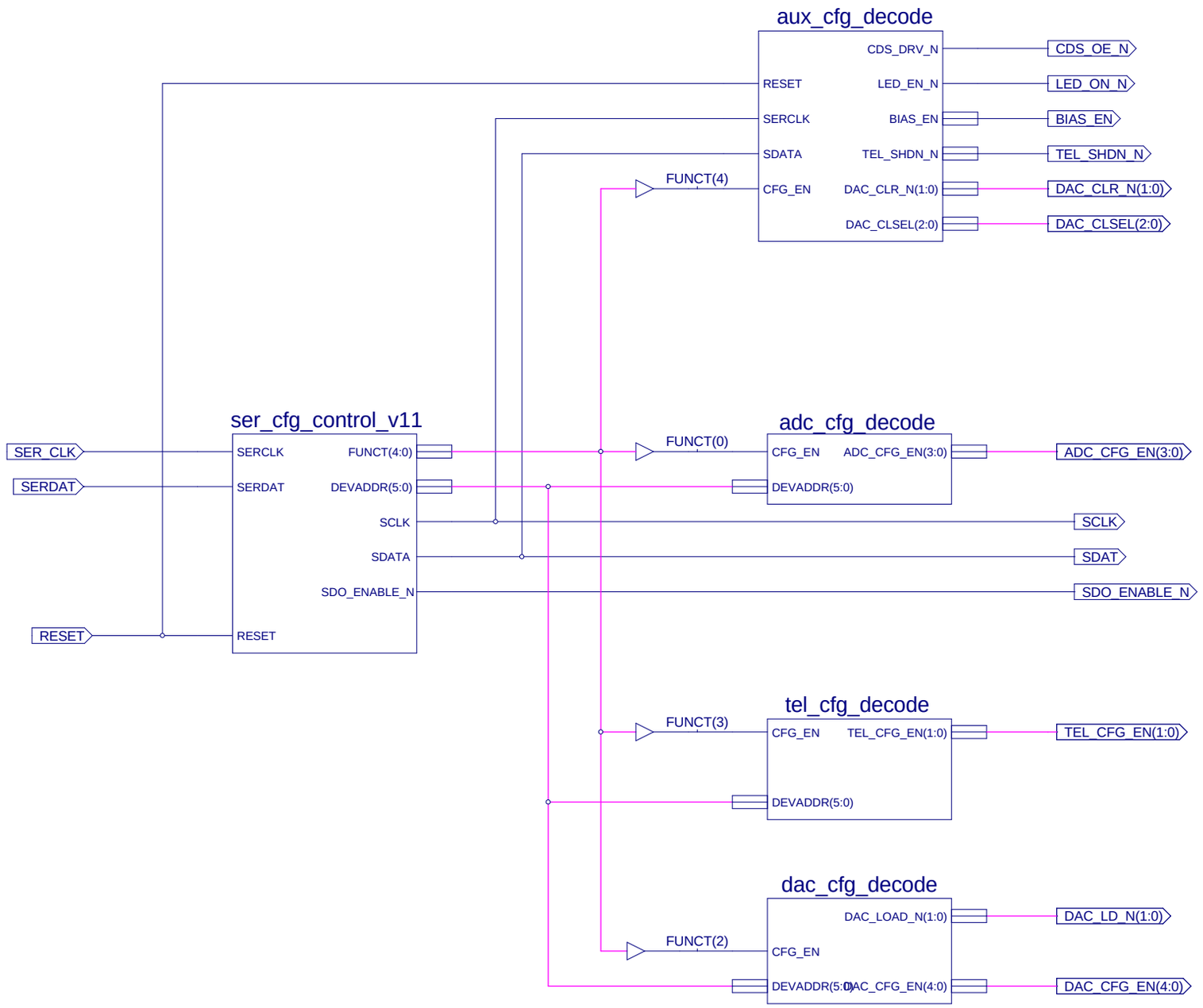

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CCD 12 CHANNEL ACQUISITION BOARD
SERIAL CONFIGURATION LOGIC

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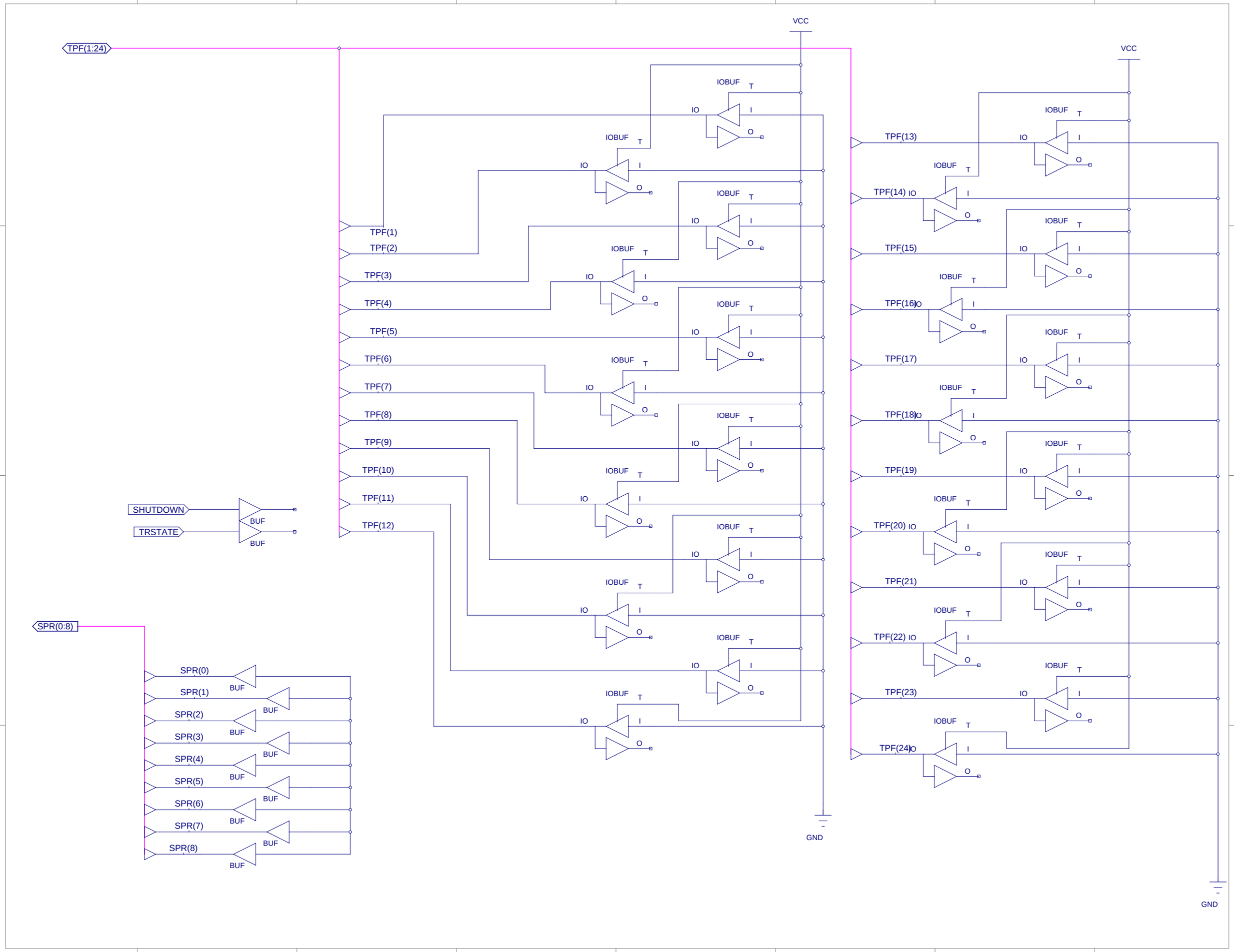
TPF(1:24)
VCC
IOBUF
T
IO
I
O
TPF(1)
TPF(2)
TPF(3)
TPF(4)
TPF(5)
TPF(6)
TPF(7)
TPF(8)
TPF(9)
TPF(10)
TPF(11)
TPF(12)
TPF(13)
TPF(14)
TPF(15)
TPF(16)
TPF(17)
TPF(18)
TPF(19)
TPF(20)
TPF(21)
TPF(22)
TPF(23)
TPF(24)
SHUTDOWN
TRSTATE
BUF
SPR(0:8)
SPR(0)
SPR(1)
SPR(2)
SPR(3)
SPR(4)
SPR(5)
SPR(6)
SPR(7)
SPR(8)
GND