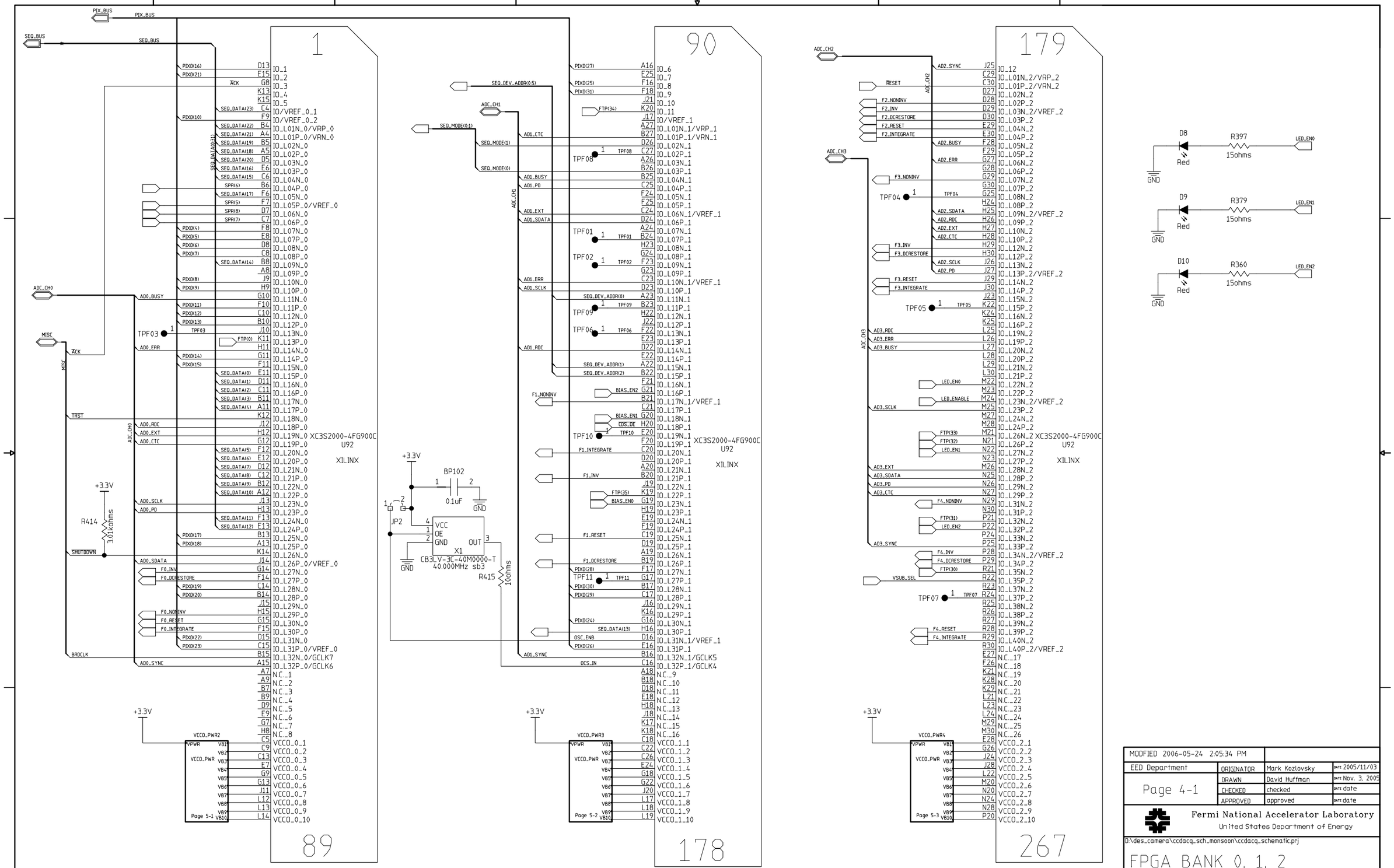


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| EED Department | ORIGINATOR | Mark Kozlovsky | DATE 2005/11/03 |
| Page 4-1 | DRAWN | David Huffman | DATE Nov. 3, 2005 |
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# FPGA BANK 0, 1, 2

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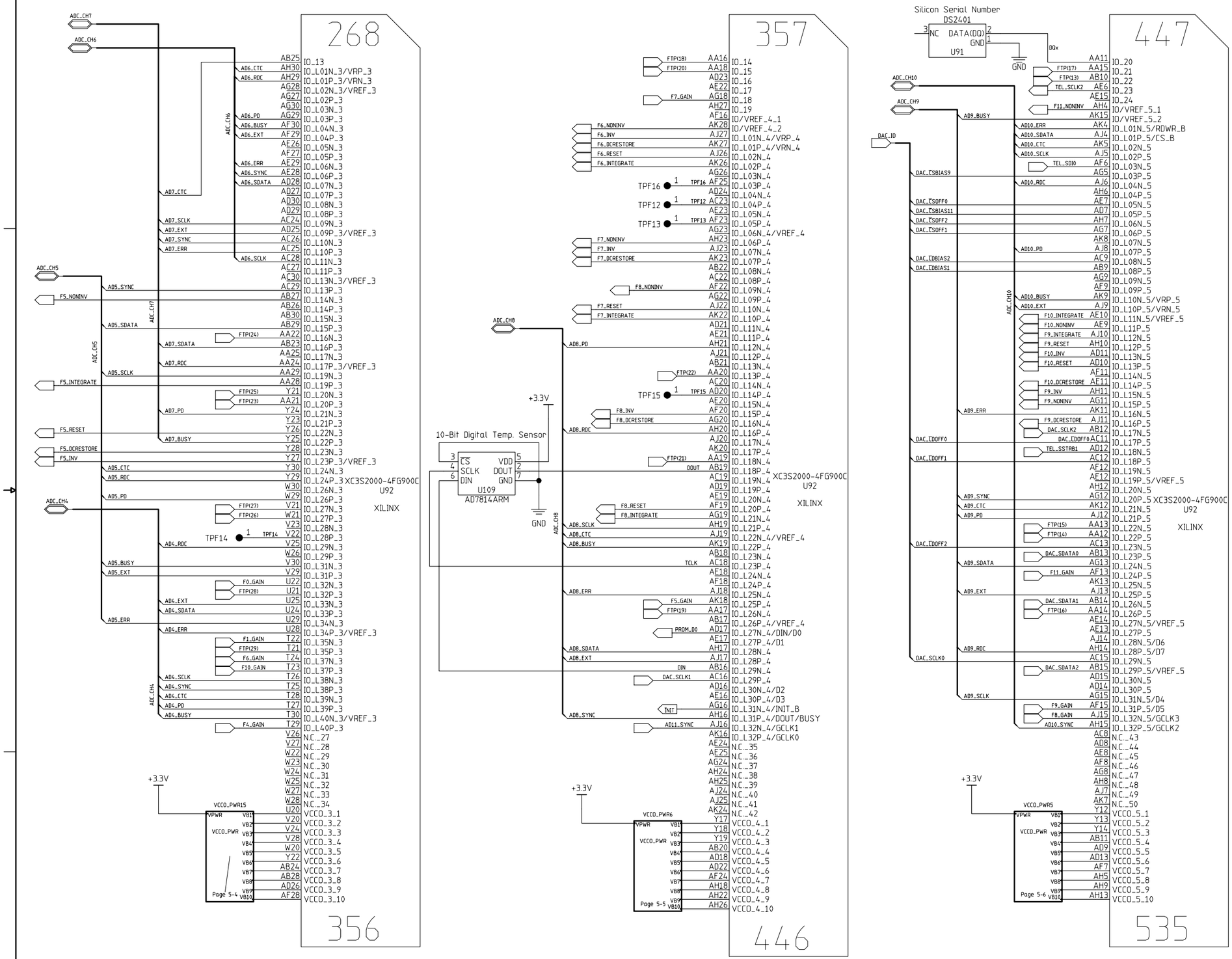
| D | 173605 | Schematic Page 01 of 05 | C |

H=8ND; V=4LA

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# FPGA BANK 3, 4, 5

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| D | 173605 | Schematic Page 02 of 05 | C |

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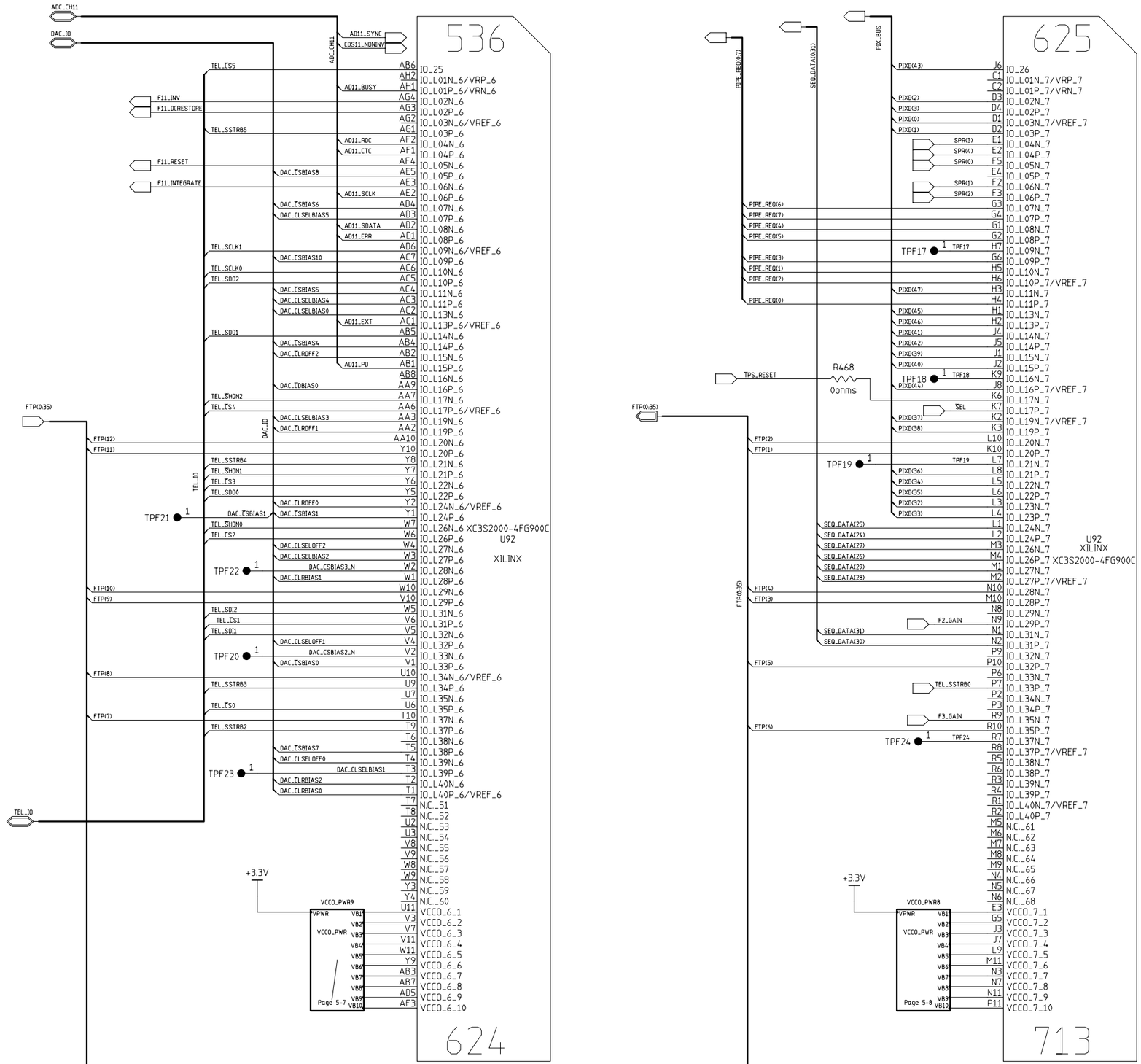


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| Page 4-3 | DRAWN | David Huffman | DATE Nov. 3, 2005 |
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# FPGA BANK 6, 7

| SIZE | DRAWING NUMBER | | REV |
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| D | 173605 | Schematic Page 03 of 05 | C |

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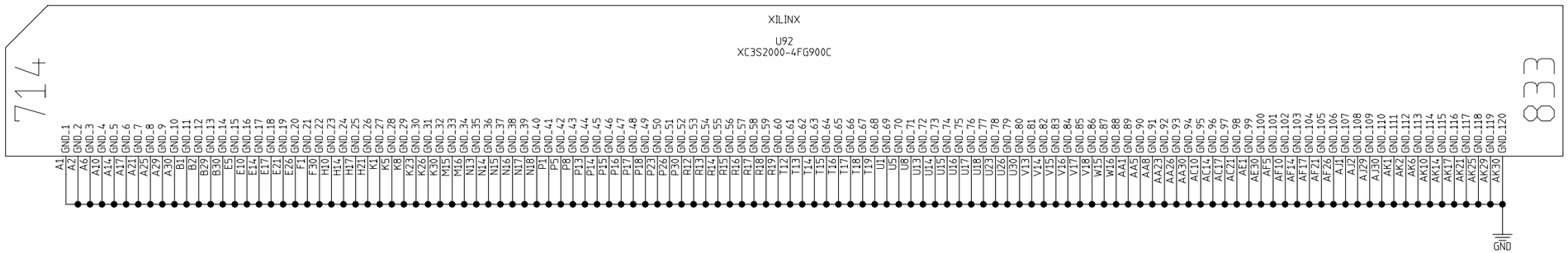


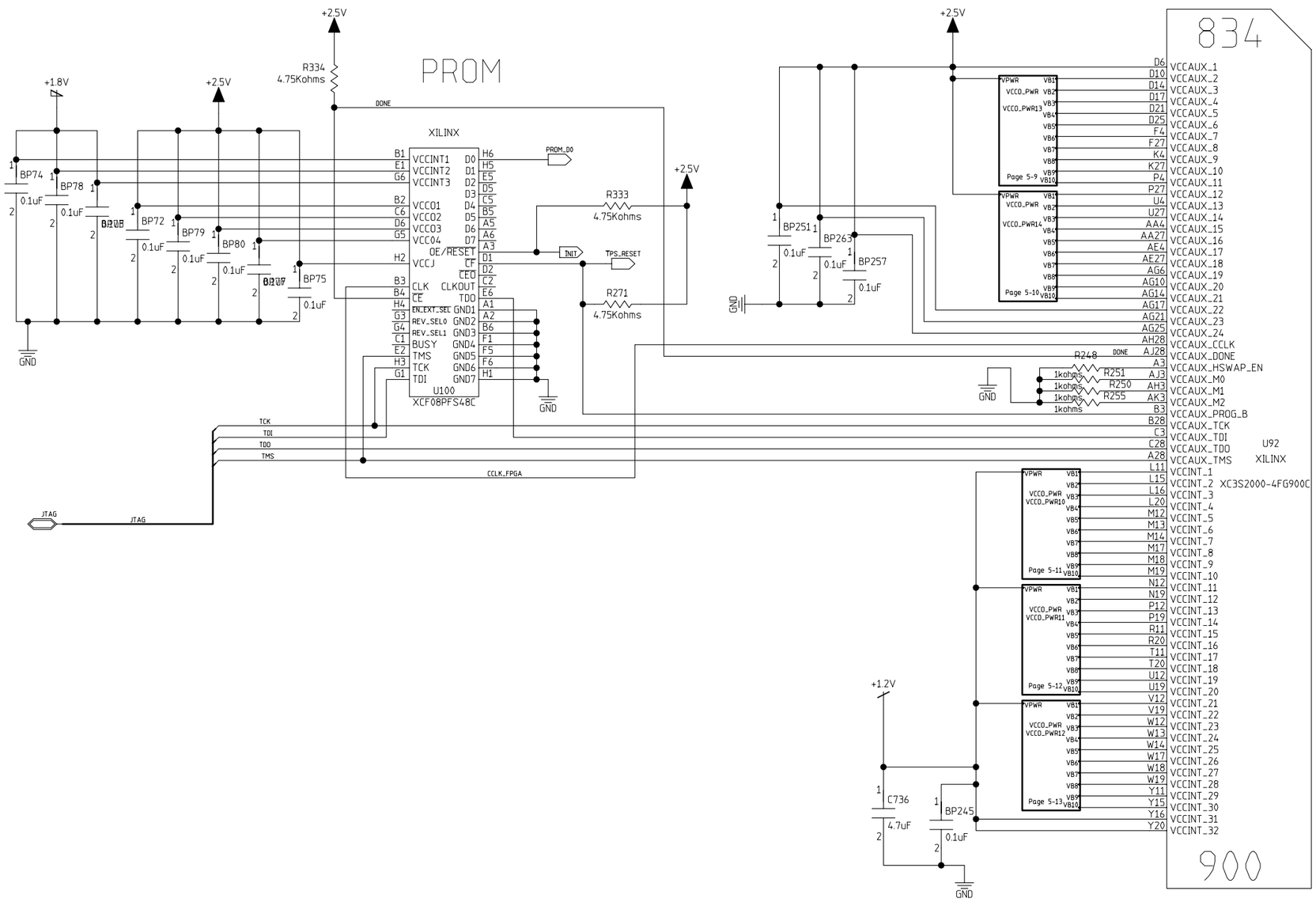


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# PROM Power & Ground

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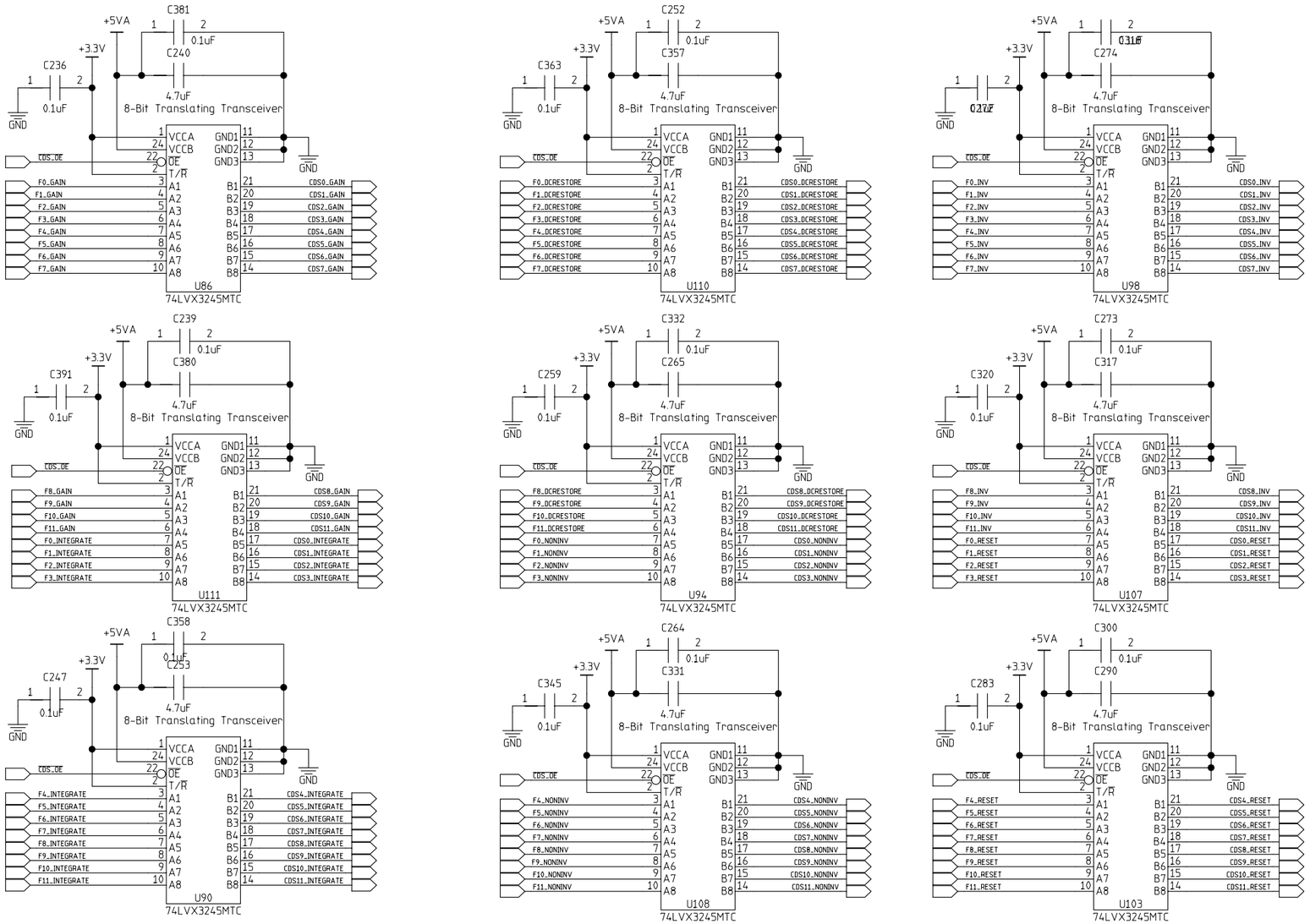


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# Level Translators

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H:8ND; V:4LA