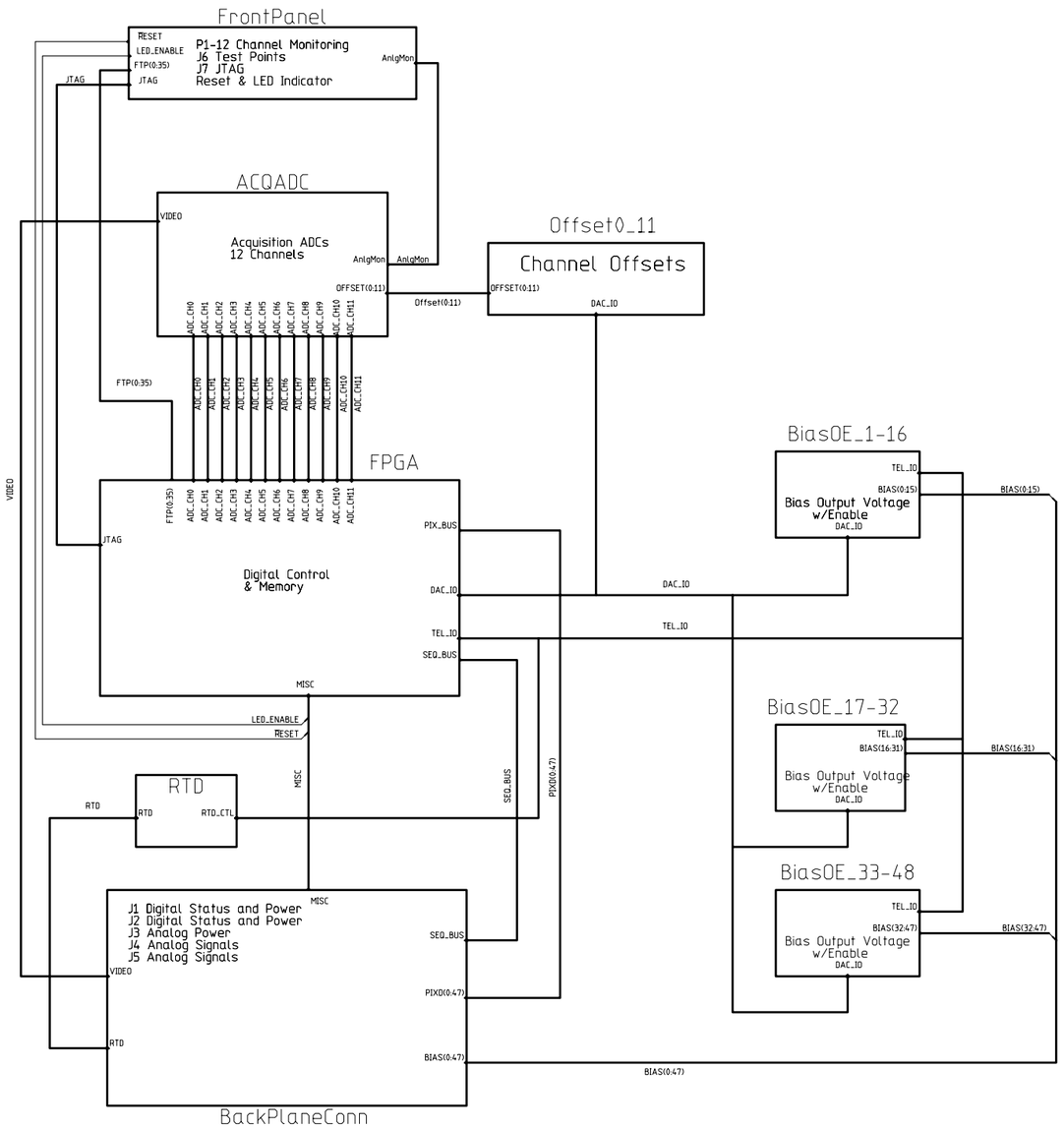

Page #	# of Pages		
1	main		
2		ACQADC	
3		X 12	Front_End_V4
4	4	FPGA	
5		X 13	VCCO_PWR
6		RTD	
7			TelADC
8	4	BackPlaneConn	
9		BiasOE_1-16	
7			TelADC
10			BUFDAC
17			SLEW
11		VRefBuf	
12		BiasOE_17-32	
7		X 2	TelADC
10		X 4	BUFDAC
13		BiasOE_33-48	
7		X 2	TelADC
10		X 4	BUFDAC
14		FrontPanel	
15		Offset0_11	
16		X 3	OFFSET

MODIFIED 2006-01-31 2:11:20 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 1	DRAWN	David Huffman	DATE Nov. 3, 2005
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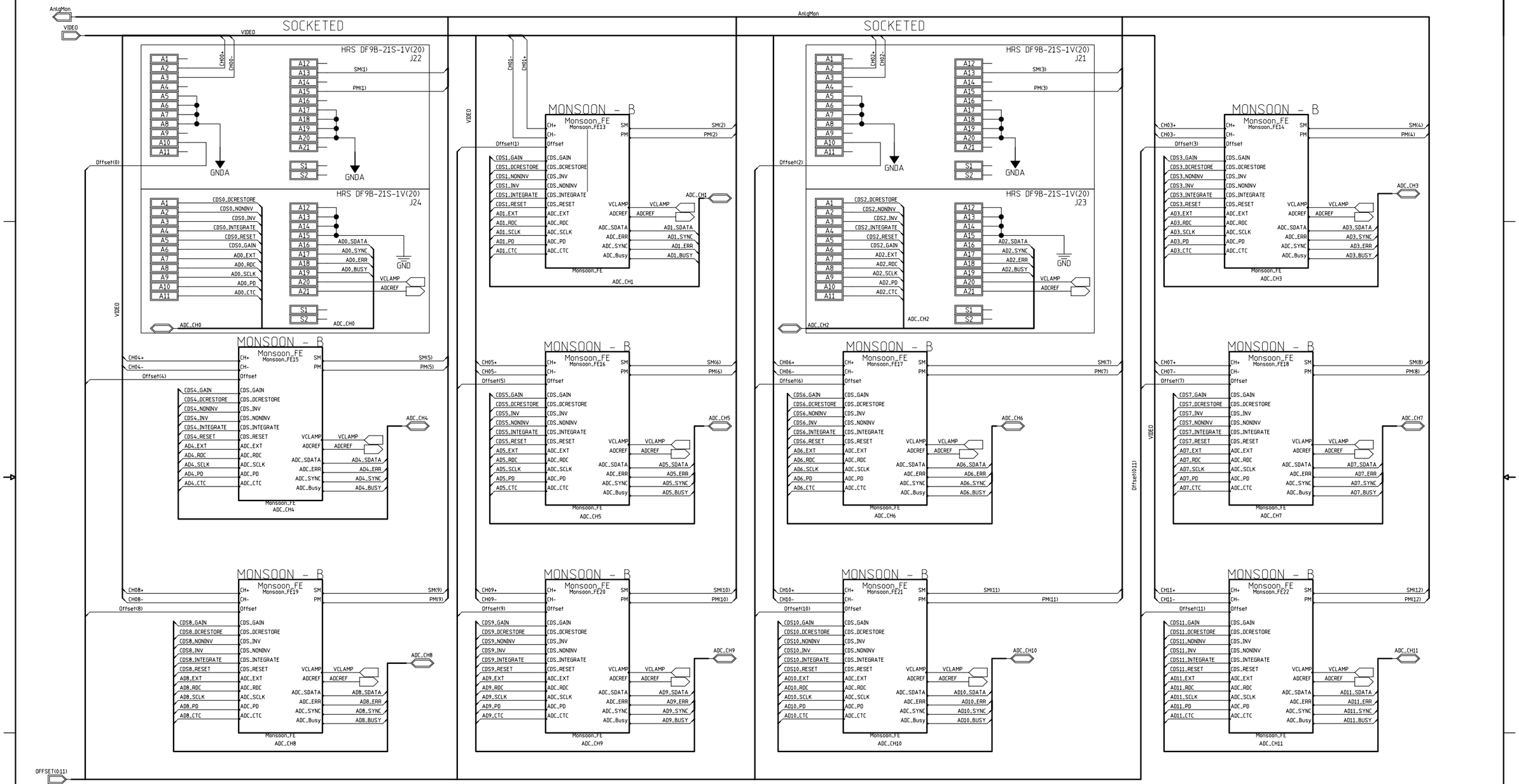
D:\des_camera\ccdacq_sch_monsoon\ccdacq_schematic.prj

ACQUISITION BOARD TOP LEVEL

SIZE	DRAWING NUMBER		REV
D	drawing number	Schematic Page 01 of 01	C

H=8ND; V=4LA


AnlgMon
VIDEO
SOCKETED
HRS DF9B-21S-1V(20)
J22
J24
J21
J23
GNDA
GND
MONSOON - B
Monsoon_FE
Monsoon_FE13
Monsoon_FE14
Monsoon_FE15
Monsoon_FE16
Monsoon_FE17
Monsoon_FE18
Monsoon_FE19
Monsoon_FE20
Monsoon_FE21
Monsoon_FE22
ADC_CH0
ADC_CH1
ADC_CH2
ADC_CH3
ADC_CH4
ADC_CH5
ADC_CH6
ADC_CH7
ADC_CH8
ADC_CH9
ADC_CH10
ADC_CH11
OFFSET(0:11)
VRefBuf
Top Level
MODIFIED 2006-03-31 1:26:04 PM
EED Department
Page 2
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
DRAWN David Huffman DATE Nov. 3, 2005
CHECKED checked DATE date
APPROVED approved DATE date
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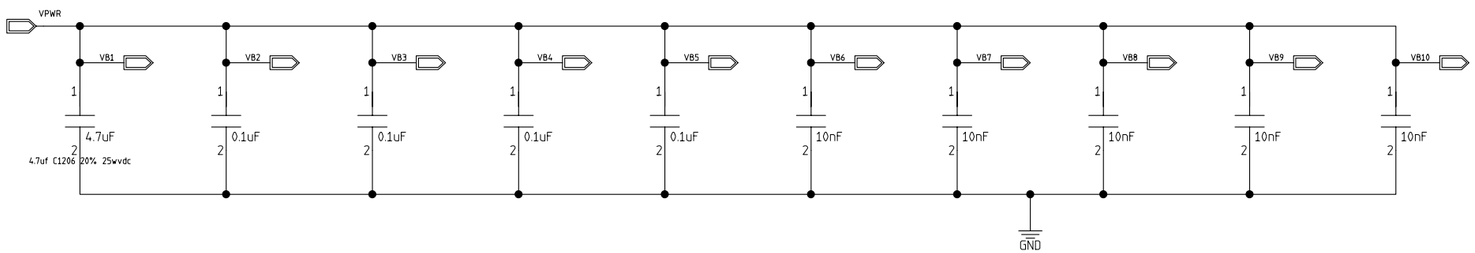
D:\des_camera\ccdacq_sch_monsoon\ccdacq_schematic.prj
ACQUISITION ADCs
SIZE D
DRAWING NUMBER drawing number
Schematic Page 01 of 01
REV C
H=8ND; V=4LA

Top Level

Previous View



MODFIED 2006-01-17 2:39:58 PM			
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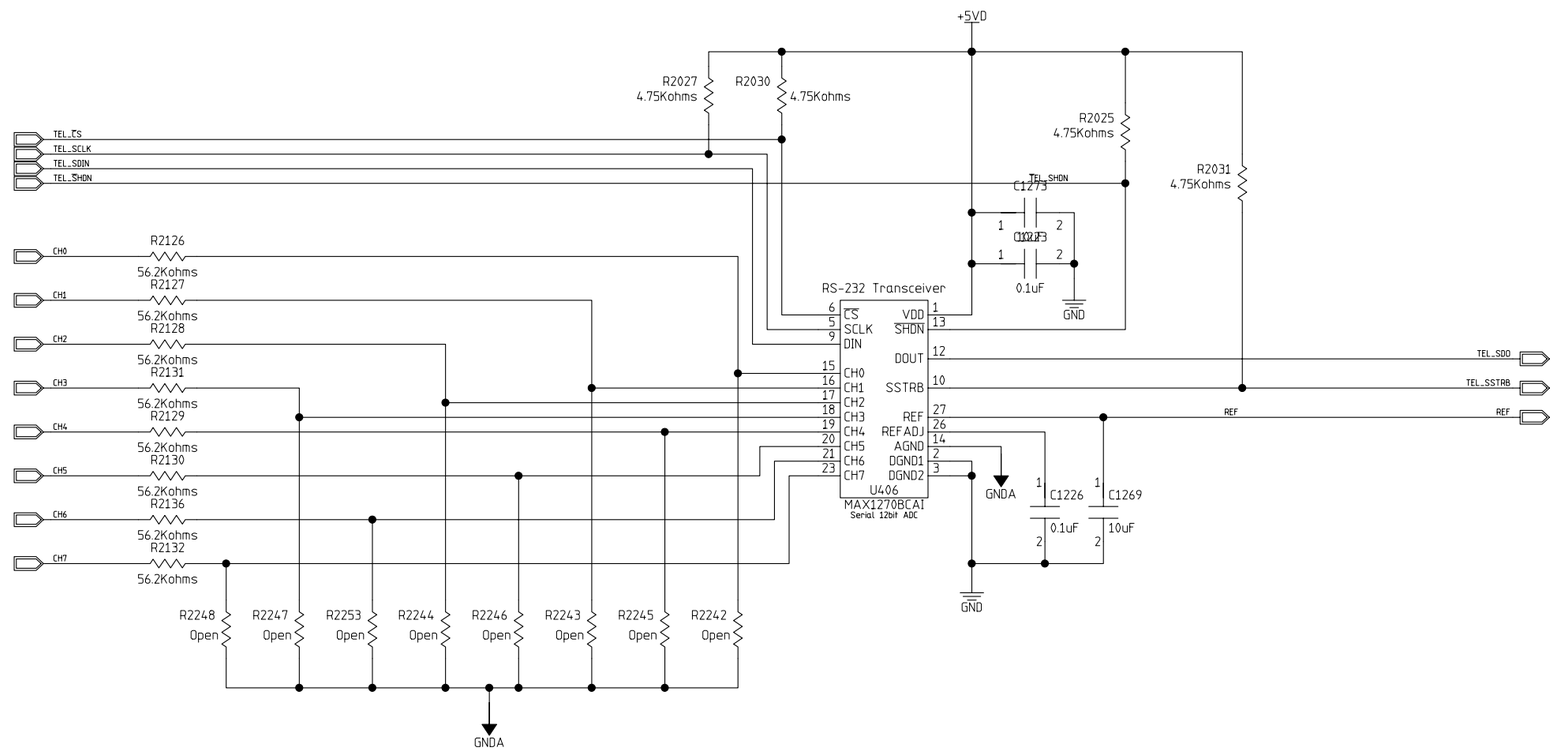
Power Rail By-Passing

SIZE	DRAWING NUMBER	REV
D	Schematic Page 01 of 01 drawing number	C

H=8ND; V=4LA

Top Level

Previous View



MODIFIED 2006-02-08 10:53:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 7 RTD- Tel	DRAWN	David Huffman	DATE Nov. 3, 2005
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	APPROVED	approved	DATE date

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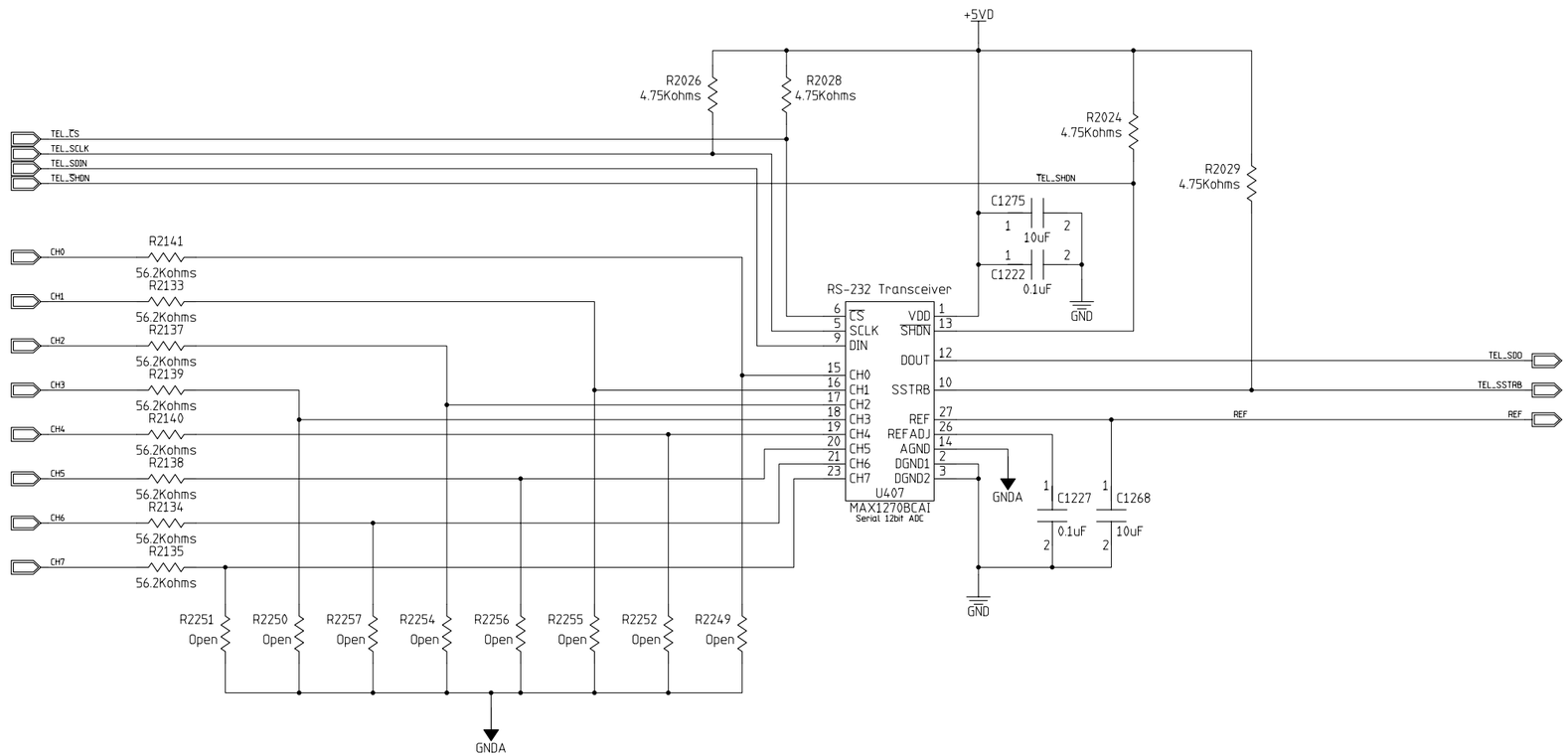
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER	REV
D	drawing number (Schematic Page 01 of 01)	C

H=8ND; V=4LA

Top Level

Previous View



TELEMETRY CHANNELS BIAS 0-7

MODFIED 2006-02-08 10:53:16 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 7	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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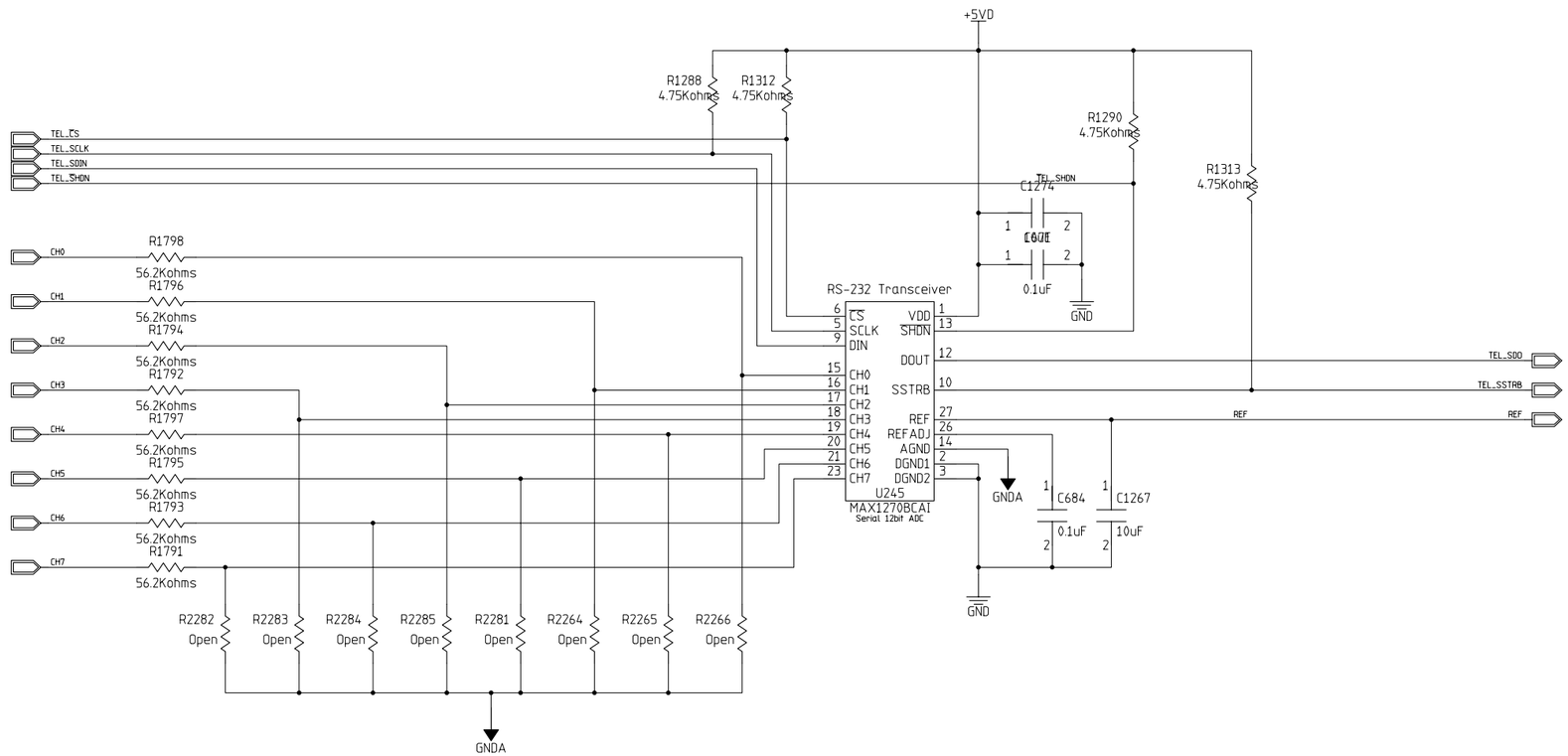
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER	REV
D	Schematic Page 01 of 01 drawing number	C

H=8ND, V=4LA

Top Level

Previous View



TELEMETRY CHANNELS BIAS 16-23

MODFIED 2006-02-08 10:53:16 AM			
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	APPROVED	approved	DATE date

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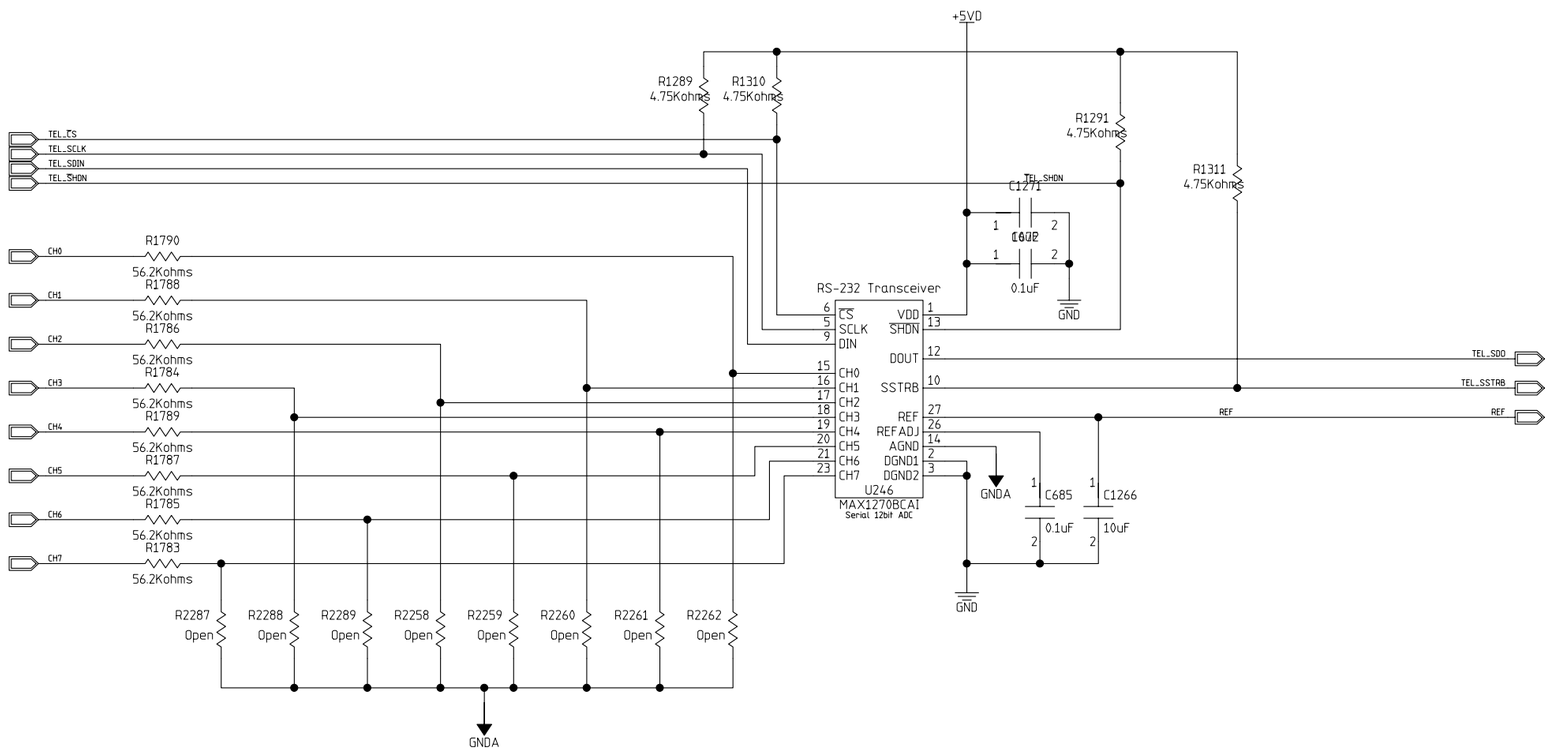
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER	REV
D	Schematic Page 01 of 01 drawing number	C

H=8ND, V=4LA

Top Level

Previous View



TELEMETRY CHANNELS BIAS 24-31

MODFIED 2006-01-30 7:46:00 AM			
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Page 7	DRAWN	David Huffman	DATE Nov. 3, 2005
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	APPROVED	approved	DATE date

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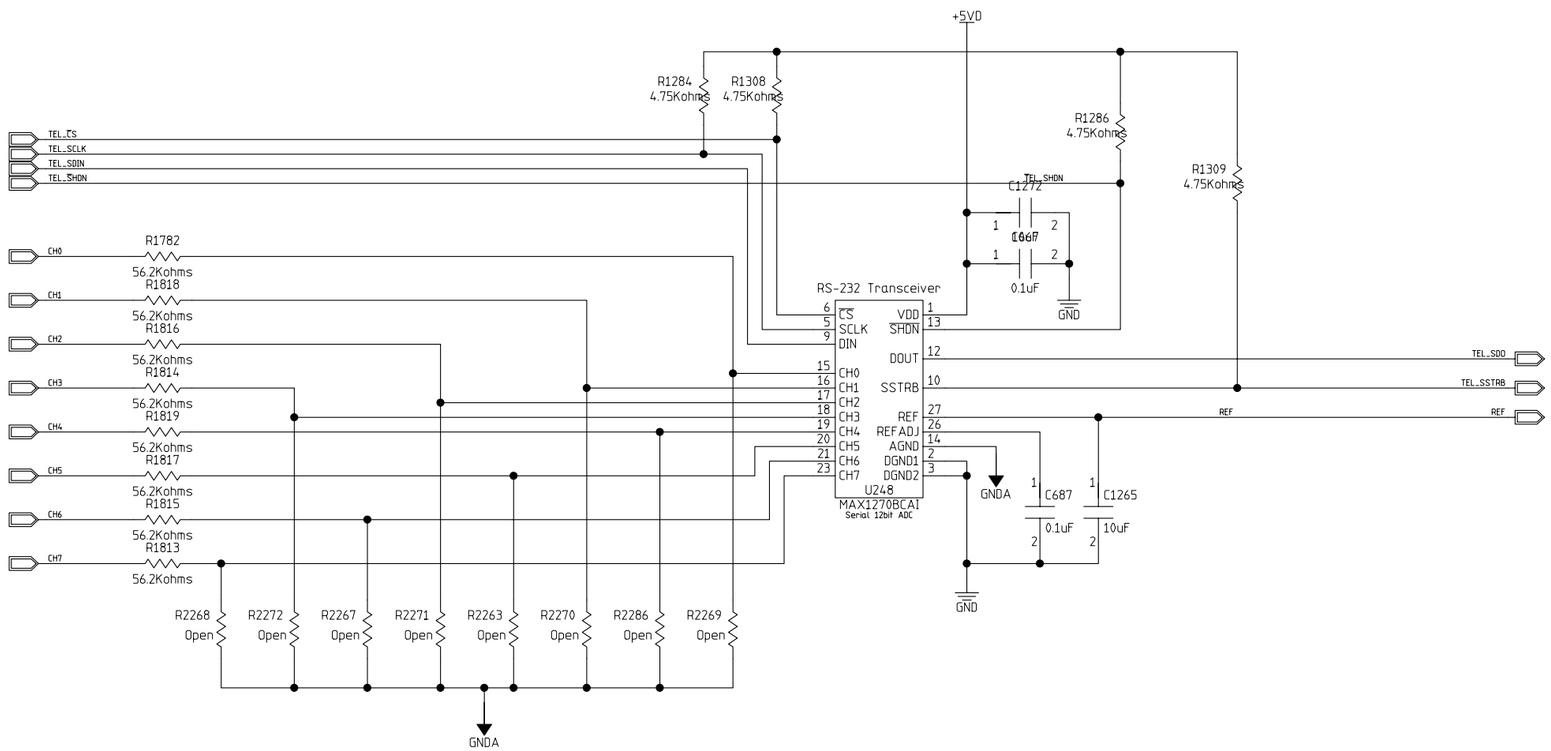
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER	REV
D	drawing number (Schematic Page 01 of 01)	C

H=8ND; V=4LA

Top Level

Previous View



TELEMETRY CHANNELS BIAS 32-39

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Page 7	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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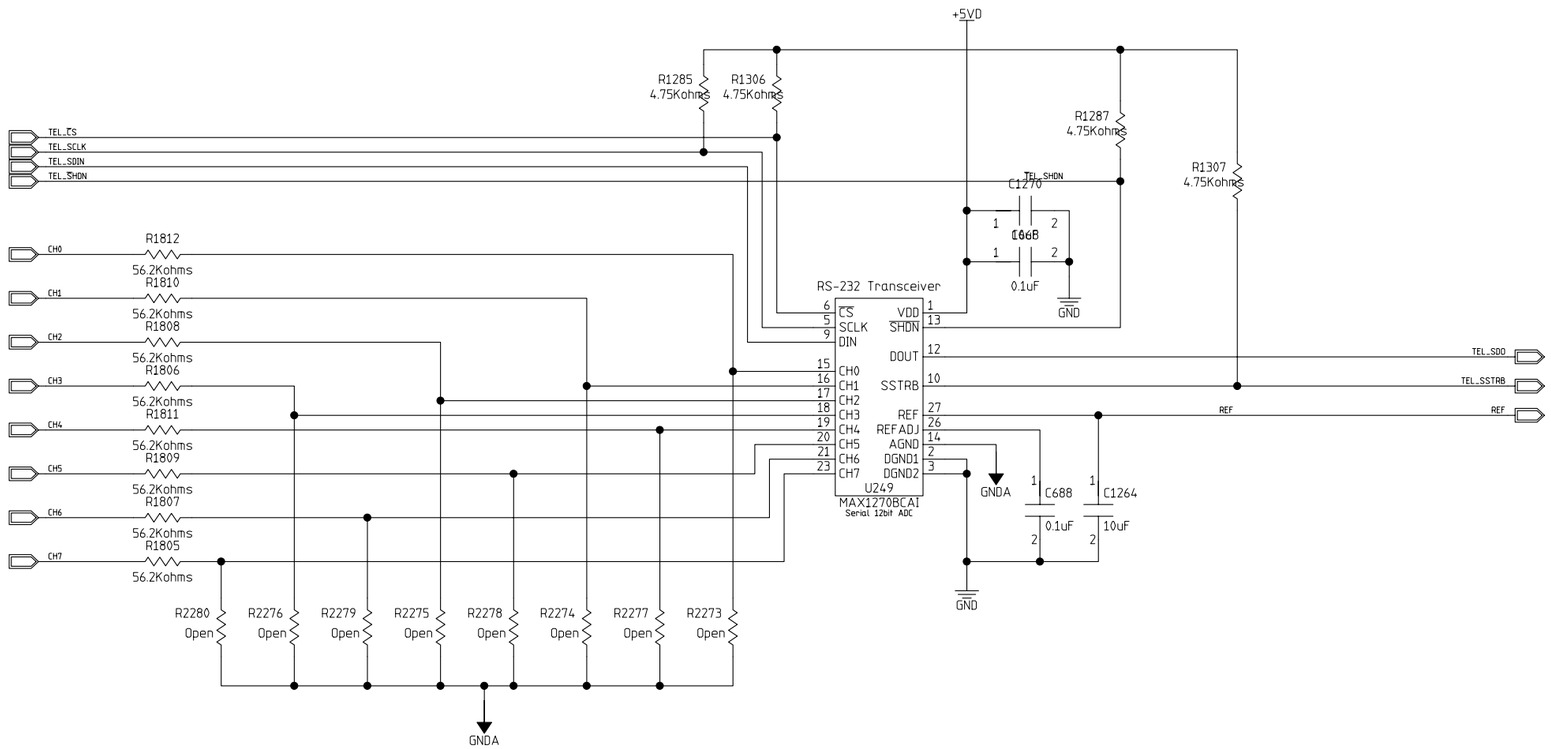
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER	REV
D	drawing number (Schematic Page 01 of 01)	C

H=8ND; V=4LA

Top Level

Previous View



TELEMETRY CHANNELS BIAS 40-47

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	APPROVED	approved	DATE date

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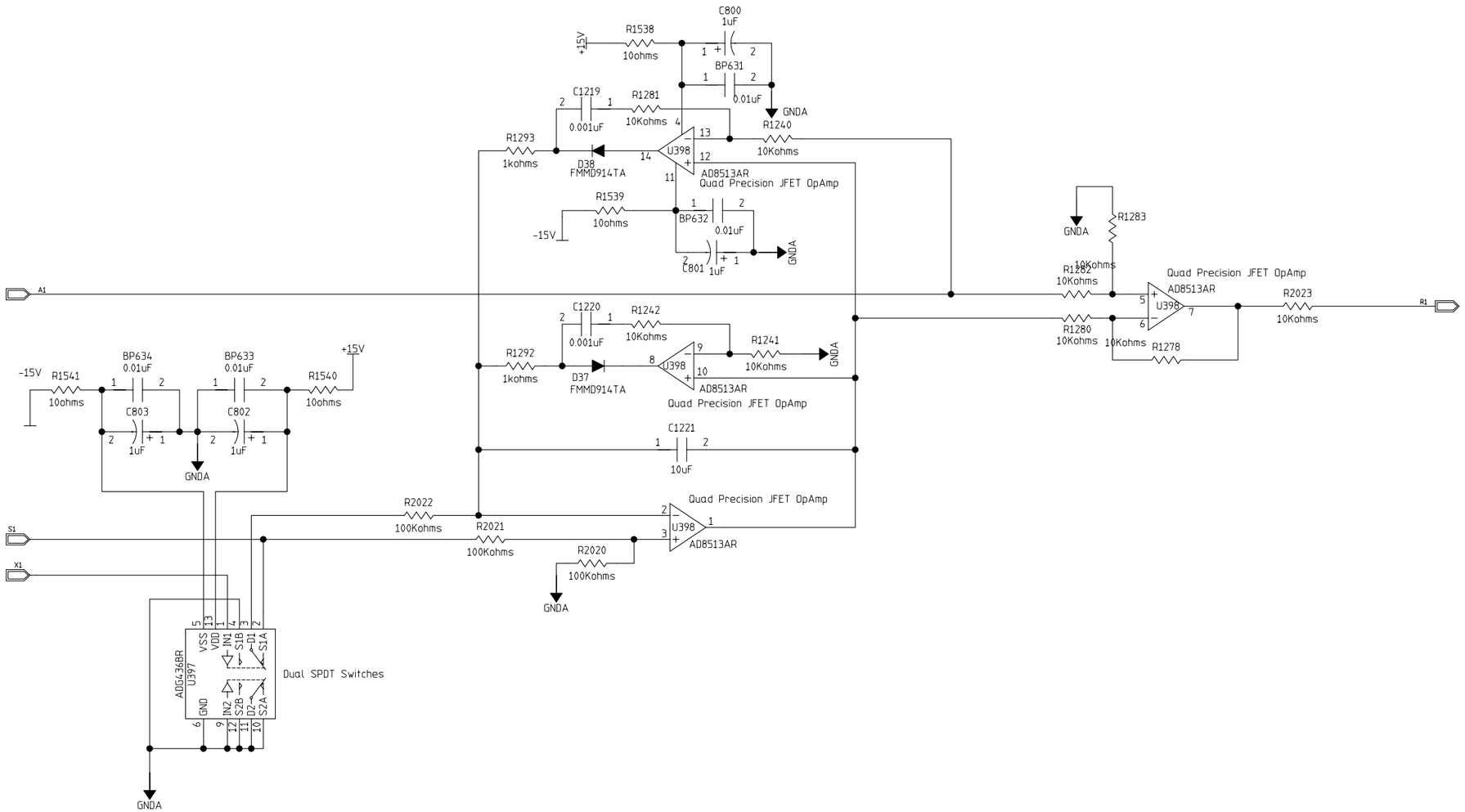
8-Channel Telemetry ADC

SIZE	DRAWING NUMBER	REV
D	drawing number (Schematic Page 01 of 01)	C

H=8ND; V=4LA

Top Level

Previous View



MODFIED 2006-01-31 2:30:08 PM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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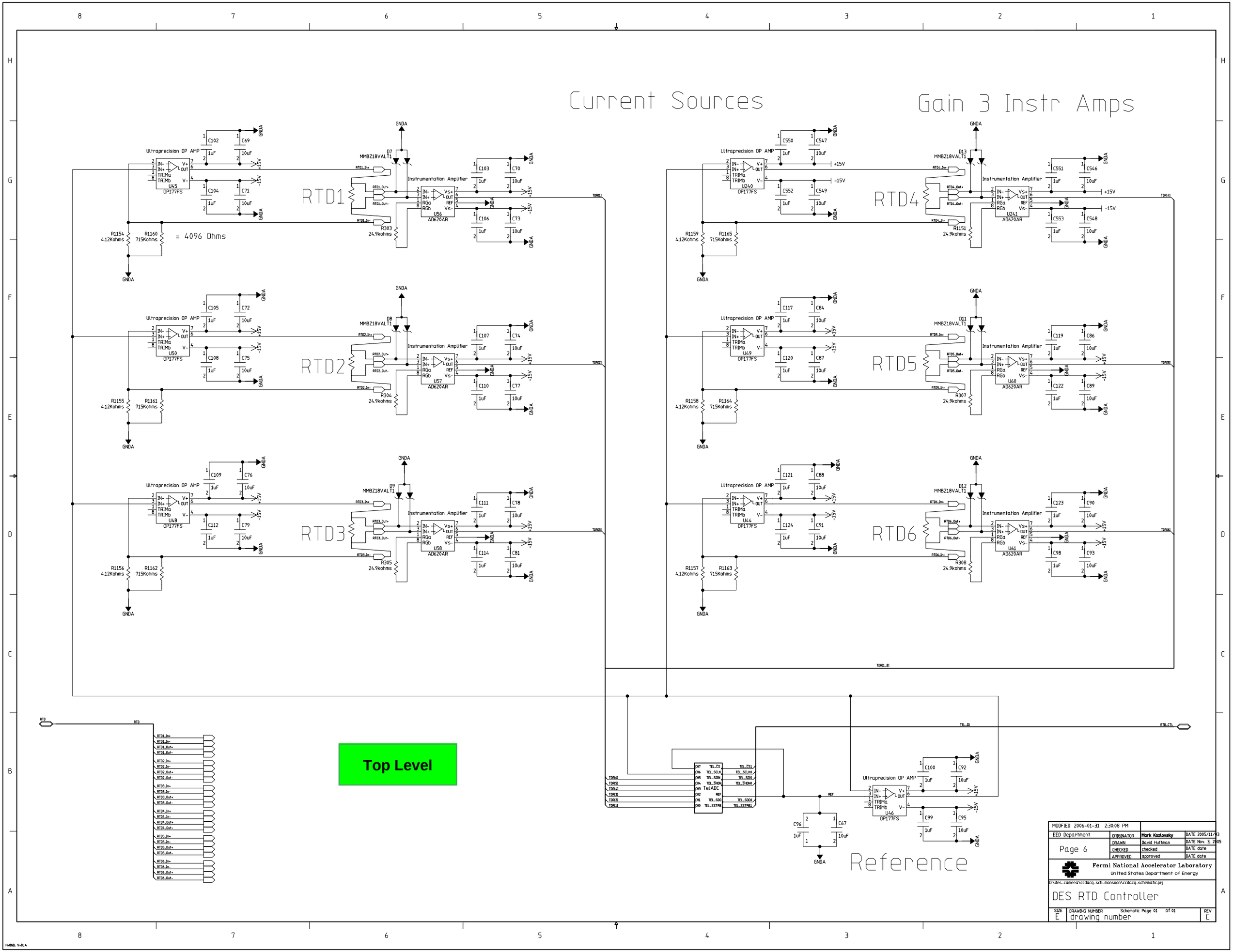
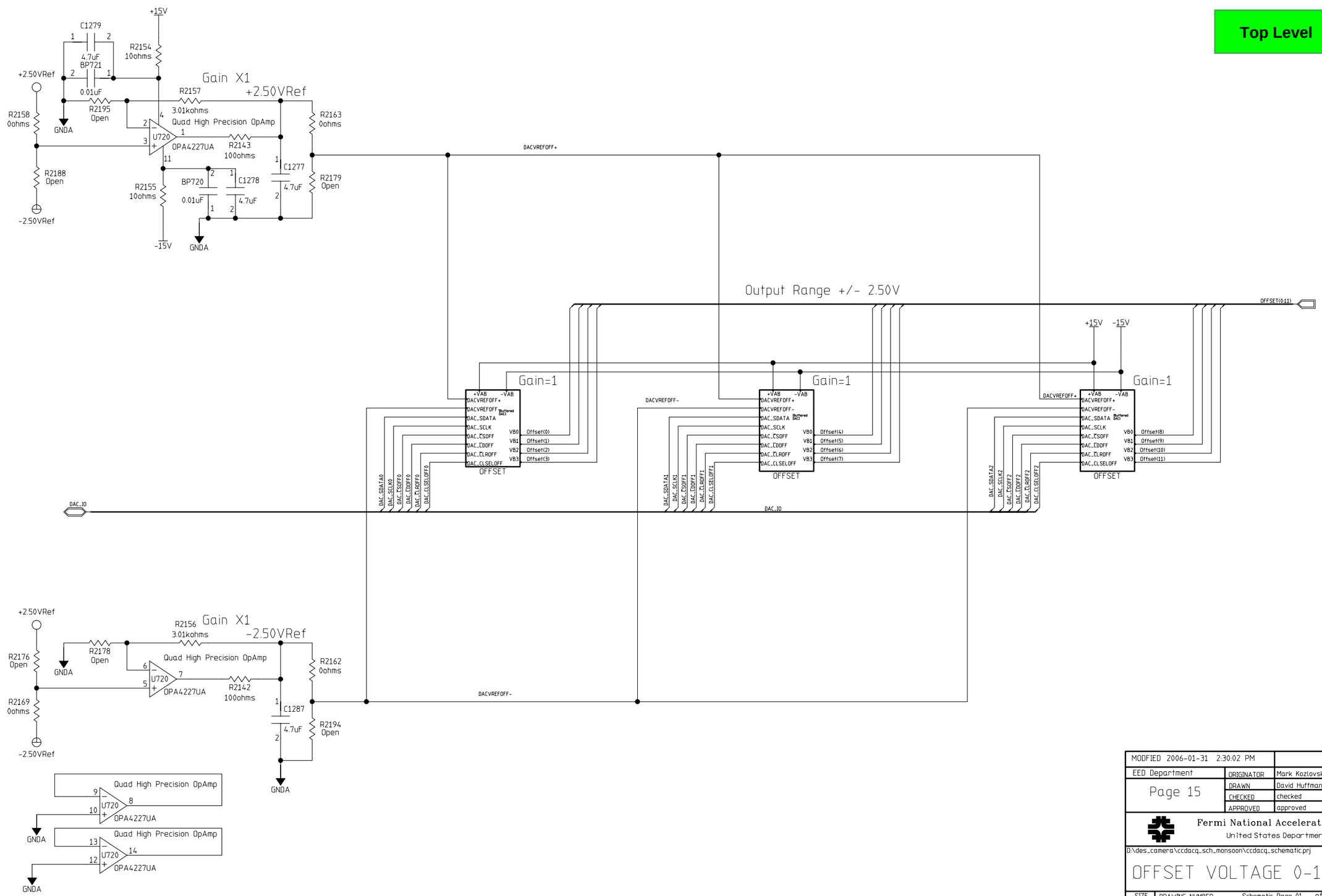
SLEW CONTROL

SIZE	DRAWING NUMBER		REV
D	drawing number	Schematic Page 01 of 01	C

H=8ND; V=4LA


Current Sources
Gain 3 Instr Amps
Ultraprecision OP AMP
Instrumentation Amplifier
RTD1
RTD2
RTD3
RTD4
RTD5
RTD6
= 4096 Ohms
Top Level
Reference
TelADC
MODIFIED 2006-01-31 2:30:08 PM
EED Department
Page 6
Mark Kaczovsky
David Huffman
Fermi National Accelerator Laboratory
United States Department of Energy
DES RTD Controller
drawing number



MODIFIED 2006-01-31 2:30:02 PM			
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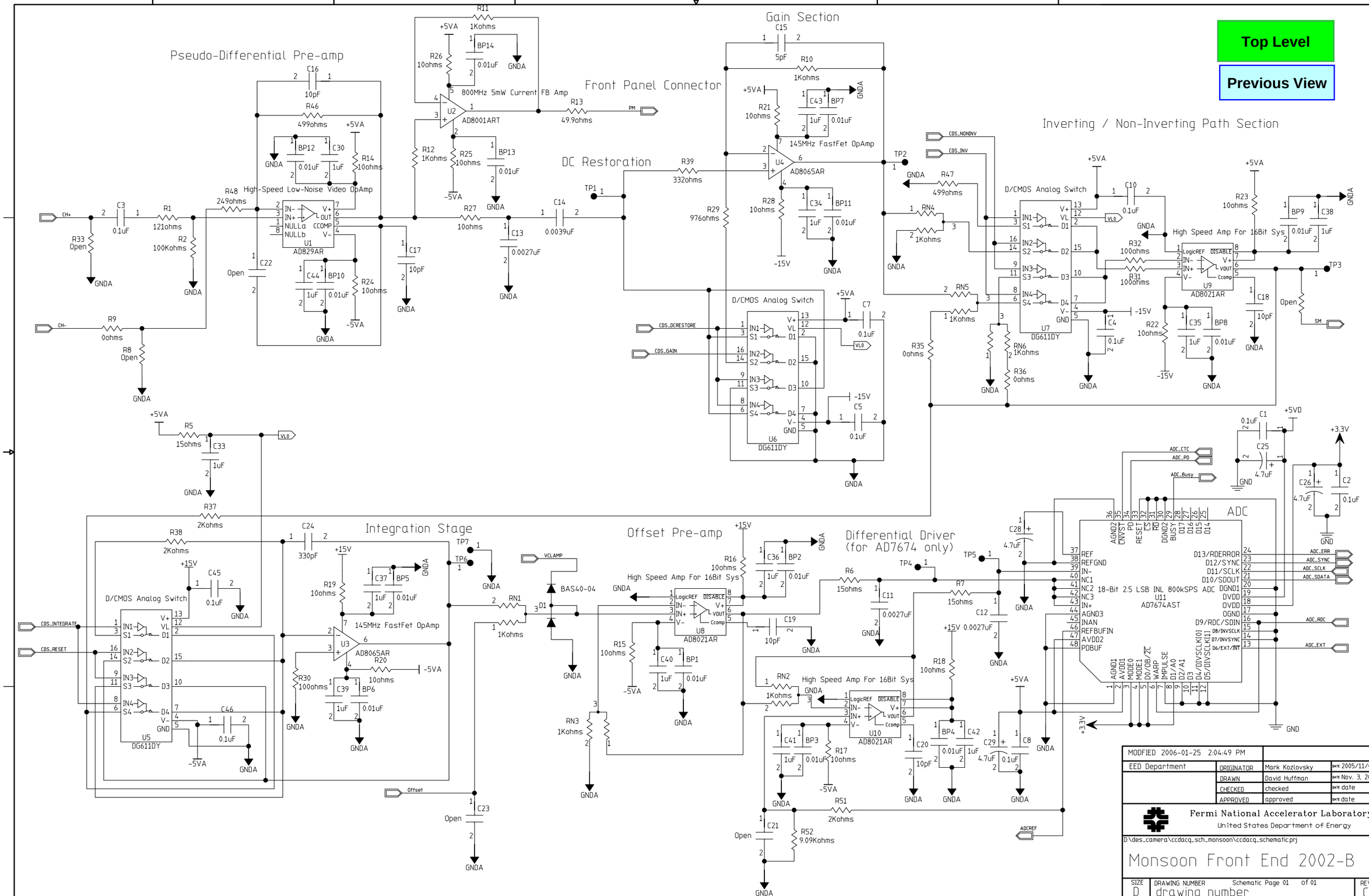
OFFSET VOLTAGE 0-11

SIZE	DRAWING NUMBER	REV
D	Schematic Page 01 of 01 drawing number	C

H=8ND, V=4LA


Top Level
Previous View
Pseudo-Differential Pre-amp
High-Speed Low-Noise Video OpAmp
AD829AR
800MHz 5mW Current FB Amp
AD8001ART
Front Panel Connector
DC Restoration
Gain Section
145MHz FastFet OpAmp
AD8065AR
Inverting / Non-Inverting Path Section
D/CMOS Analog Switch
DG611DY
High Speed Amp For 16Bit Sys
AD8021AR
Integration Stage
Offset Pre-amp
Differential Driver
(for AD7674 only)
ADC
AD7674AST
18-Bit 2.5 LSB INL 800kSPS ADC
MODIFIED 2006-01-25 2:04:49 PM
EED Department
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
DRAWN David Huffman DATE Nov. 3, 2005
CHECKED checked DATE date
APPROVED approved DATE date
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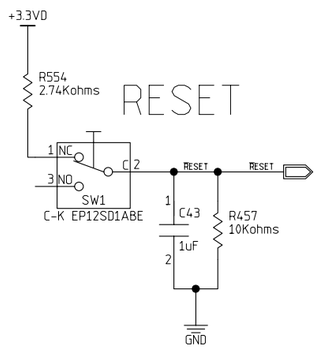
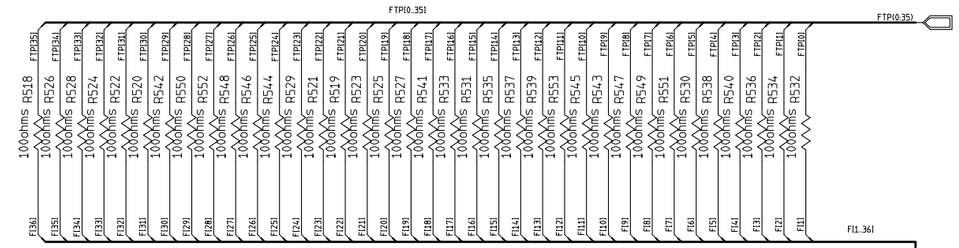
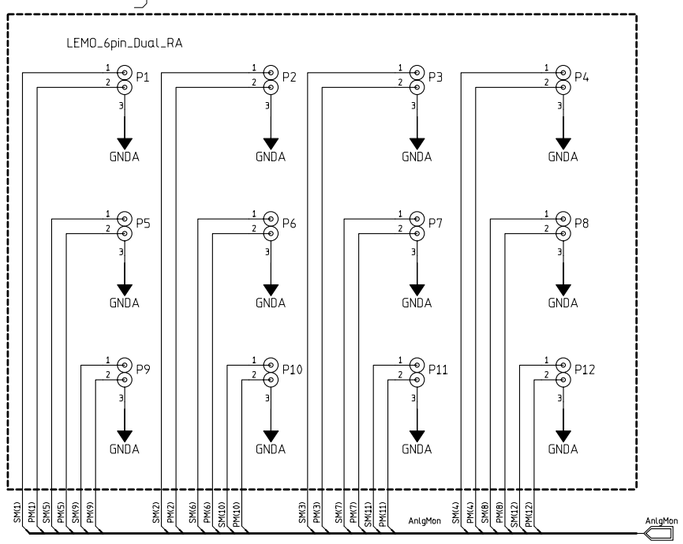
Monsoon Front End 2002-B
SIZE D
DRAWING NUMBER drawing number
Schematic Page 01 of 01
REV C

Top Level

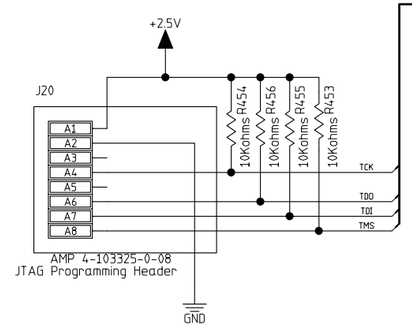




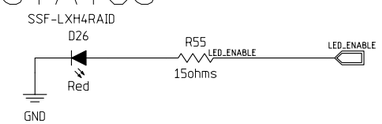
Analog Test Points



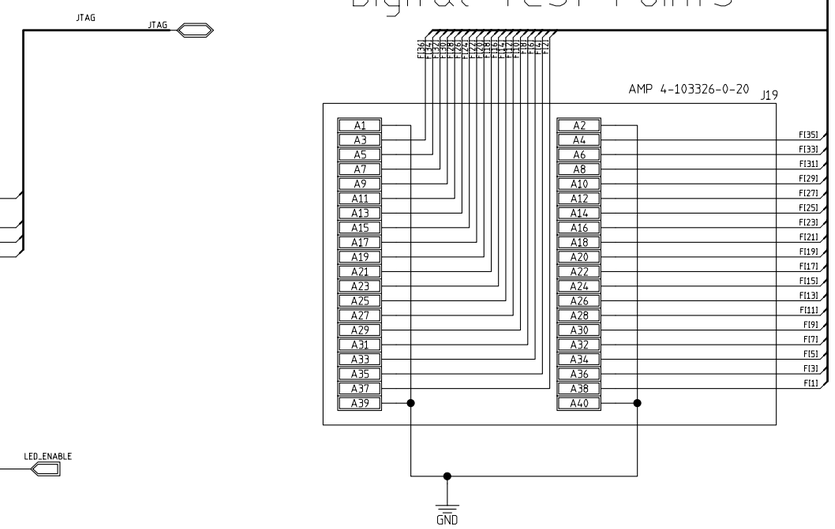
JTAG



STATUS



Digital Test Points



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J6 Test Points/ Analog Mon
J7 JTAG

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D	drawing number	Schematic Page 01 of 01	C

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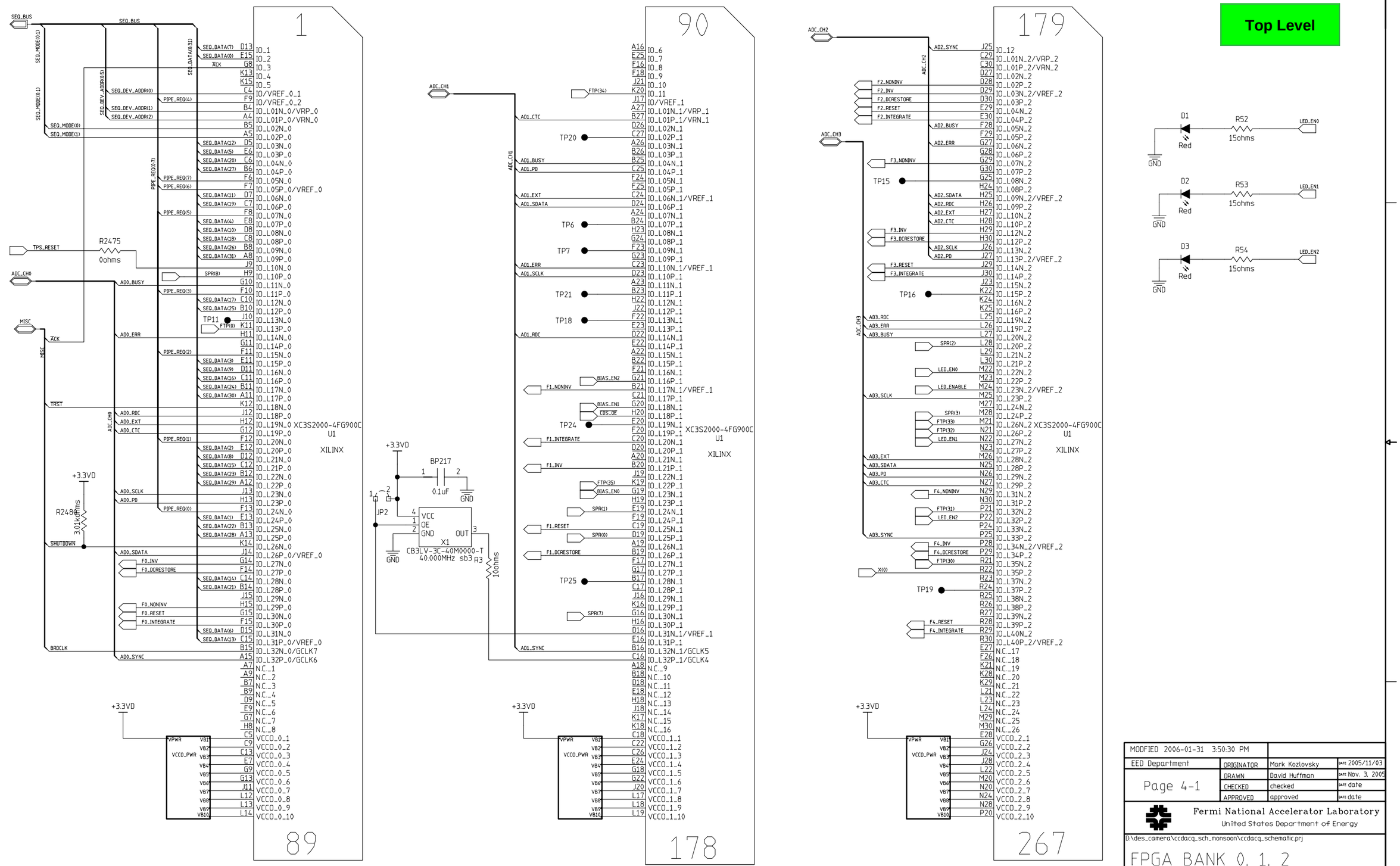

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Page 4-1	DRAWN	David Huffman	DATE Nov. 3, 2005
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	APPROVED	approved	DATE date

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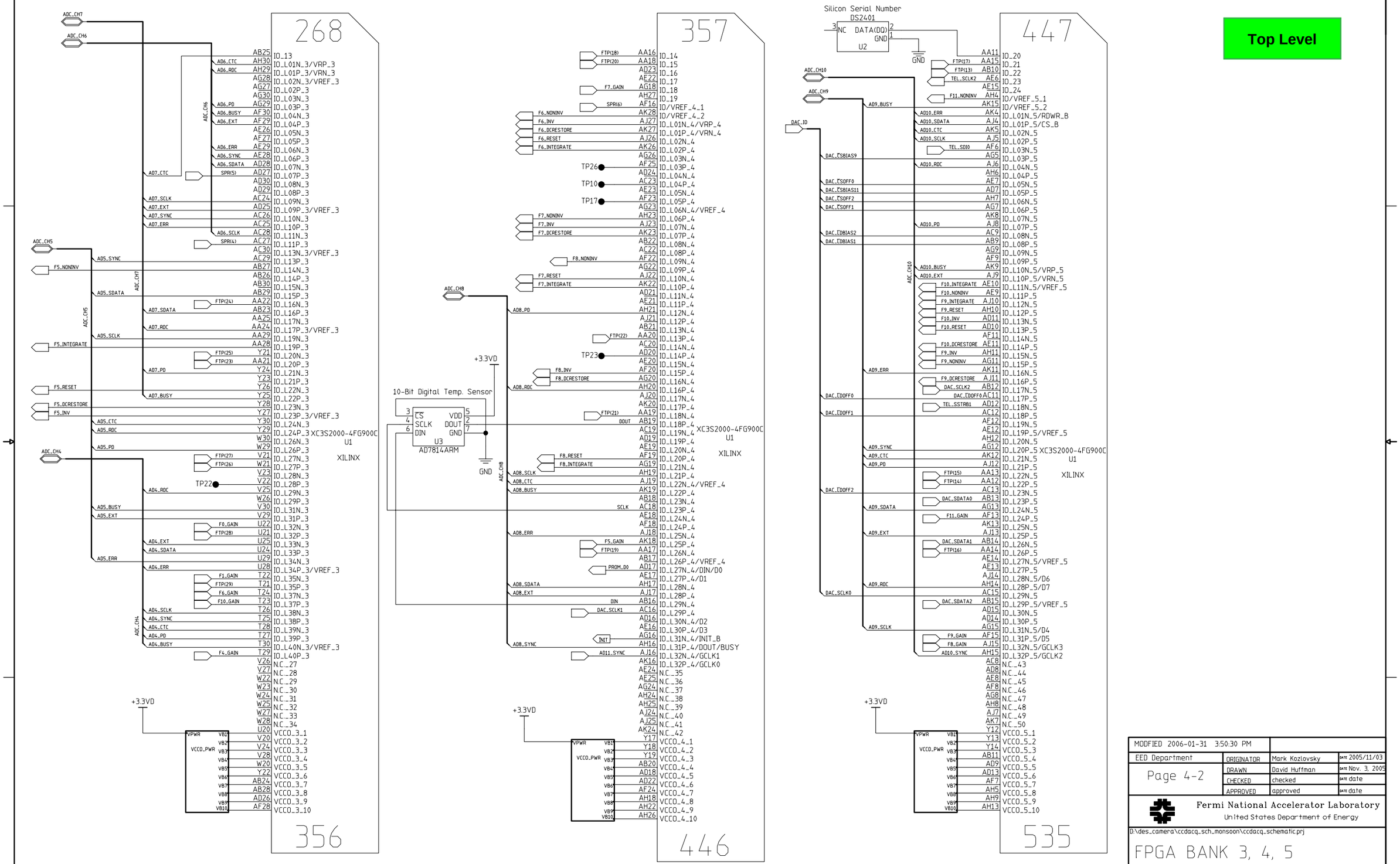
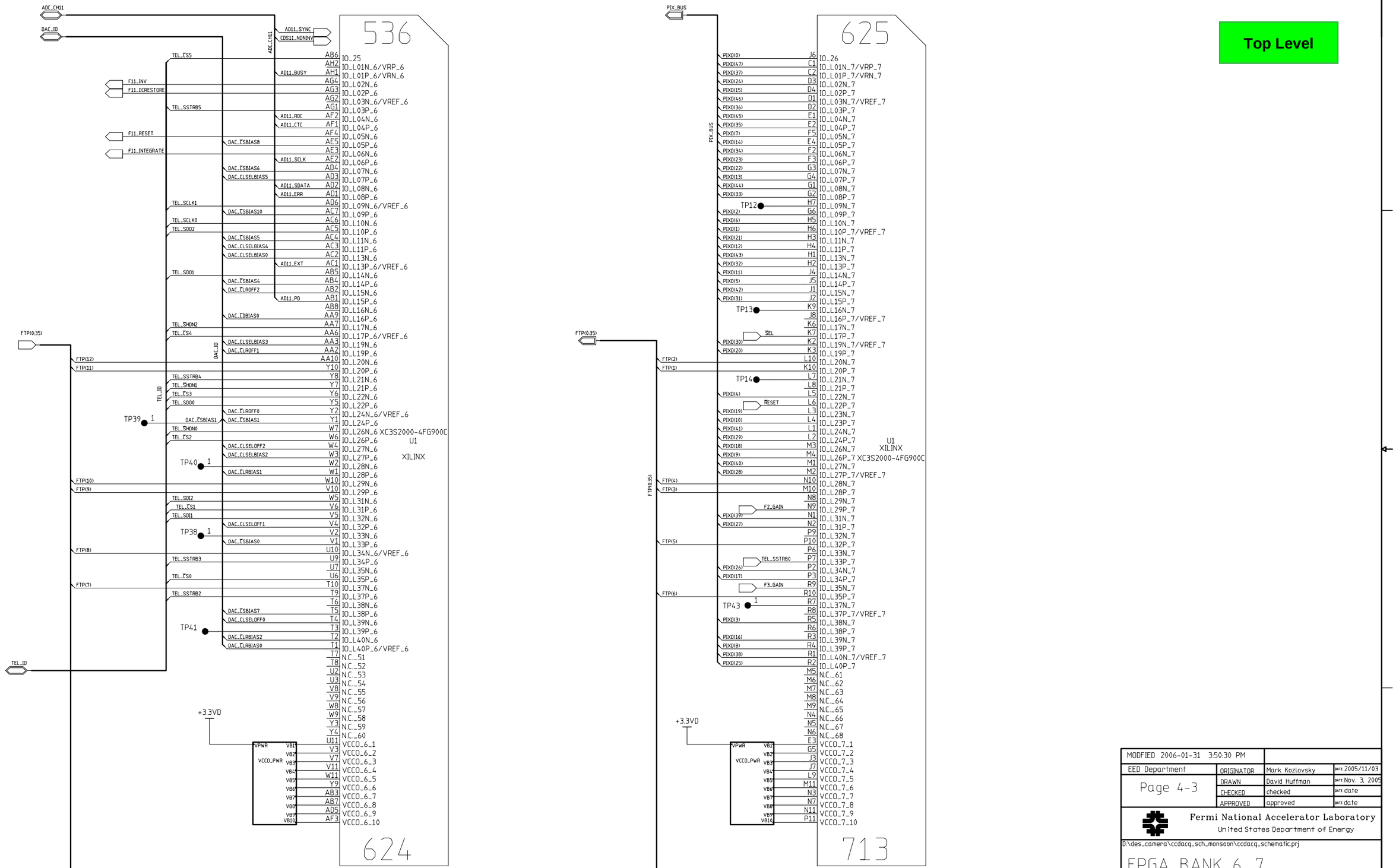
FPGA BANK 0, 1, 2

SIZE	DRAWING NUMBER		REV
D	drawing number	Schematic Page 01 of 05	C

H=8ND; V=4LA


Top Level
268
357
447
356
446
535
XC3S2000-4FG900C
U1
XILINX
10-Bit Digital Temp. Sensor
AD7814ARM
U3
Silicon Serial Number
DS2401
U2
+3.3VD
GND
MODIFIED 2006-01-31 3:50:30 PM
EED Department
Page 4-2
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
DRAWN David Huffman DATE Nov. 3, 2005
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
D:\des_camera\ccdacq_sch_monsoon\ccdacq_schematic.prj
FPGA BANK 3, 4, 5
SIZE D
DRAWING NUMBER drawing number
Schematic Page 02 of 05
REV C



MODFIED 2006-01-31 3:50:30 PM			
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Page 4-3	DRAWN	David Huffman	DATE Nov. 3, 2005
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	APPROVED	approved	DATE date

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FPGA BANK 6, 7

SIZE	DRAWING NUMBER	REV
D	drawing number	C

Schematic Page 03 of 05

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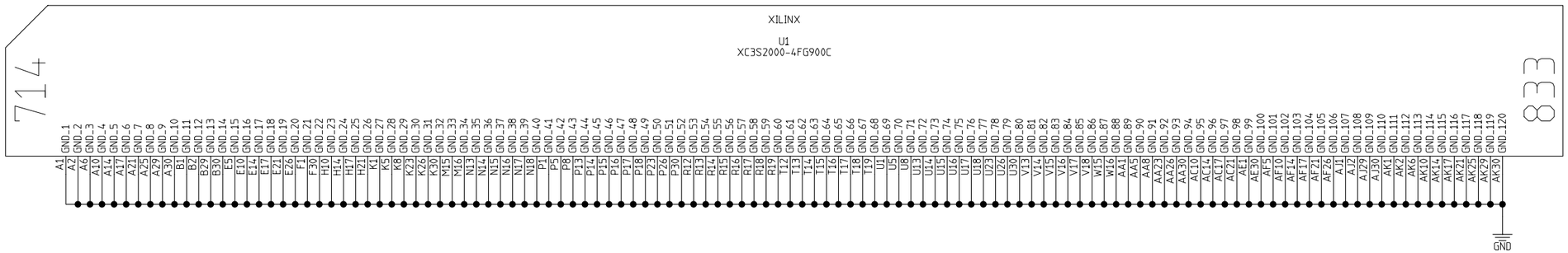
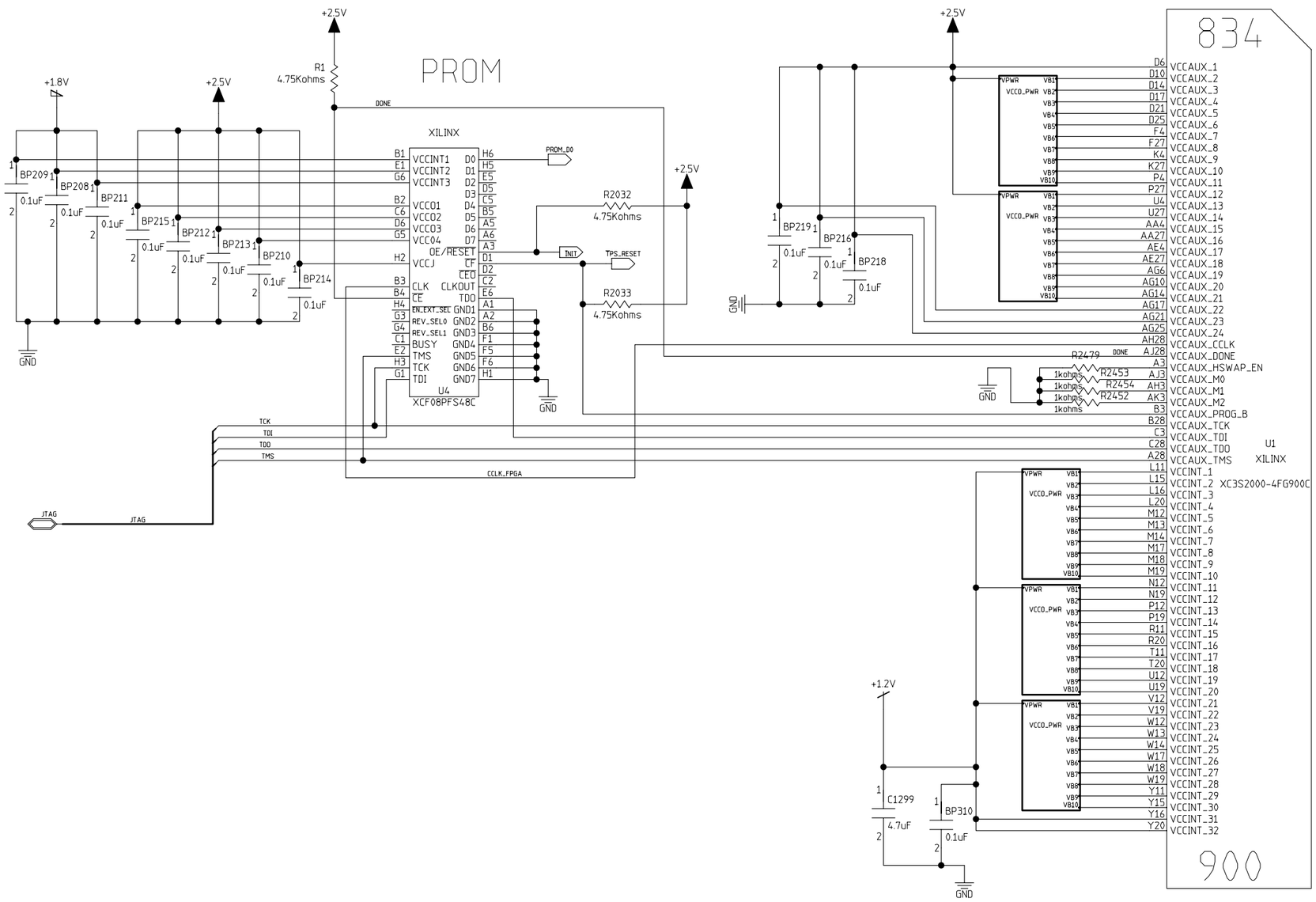


Top Level



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	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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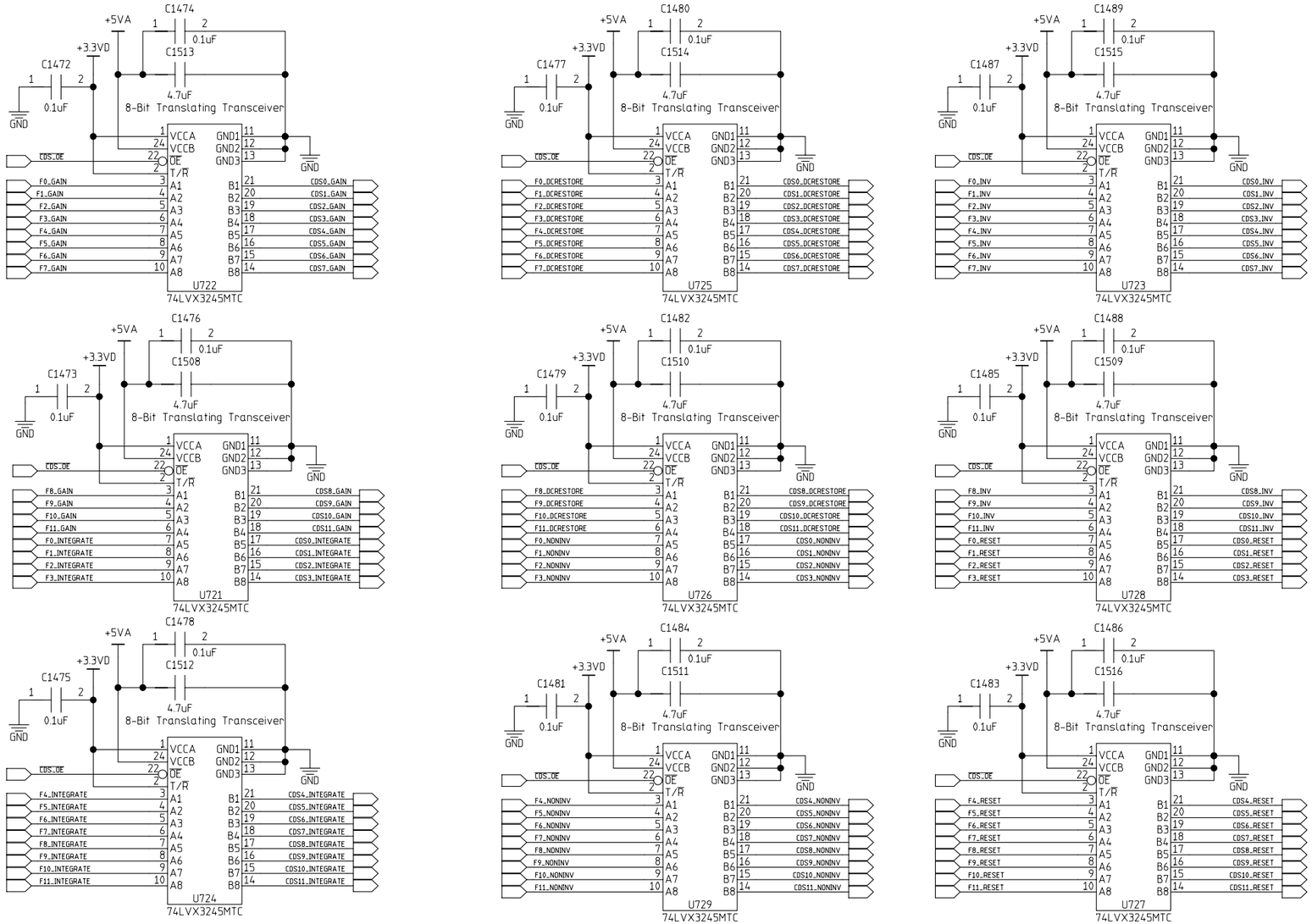
PROM Power & Ground

SIZE	DRAWING NUMBER		REV
D	drawing number	Schematic Page 04 of 05	C

H=8ND; V=4LA



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	DRAWN	David Huffman	DATE Nov. 3, 2005
	CHECKED	checked	DATE date
	APPROVED	approved	DATE date

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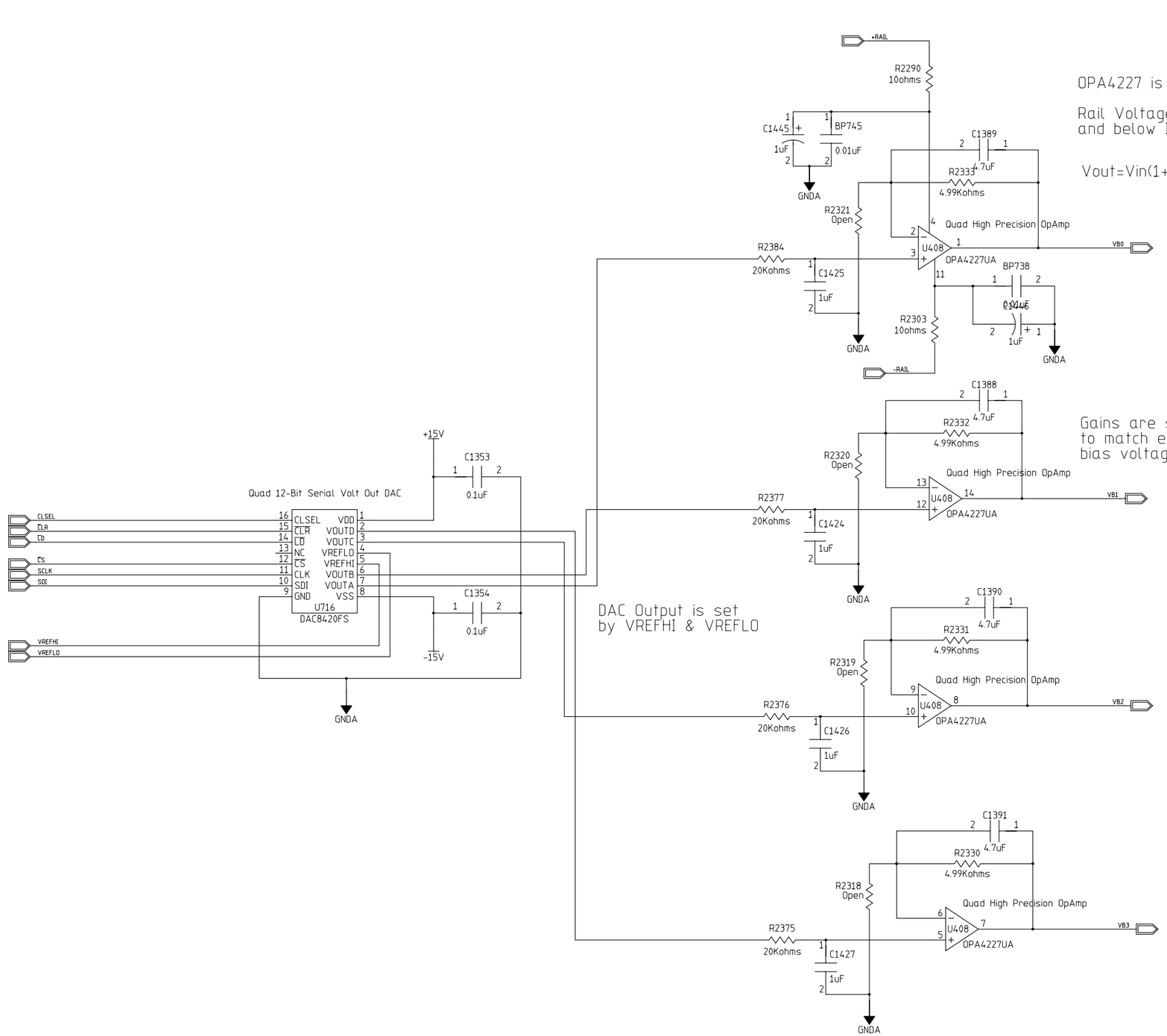
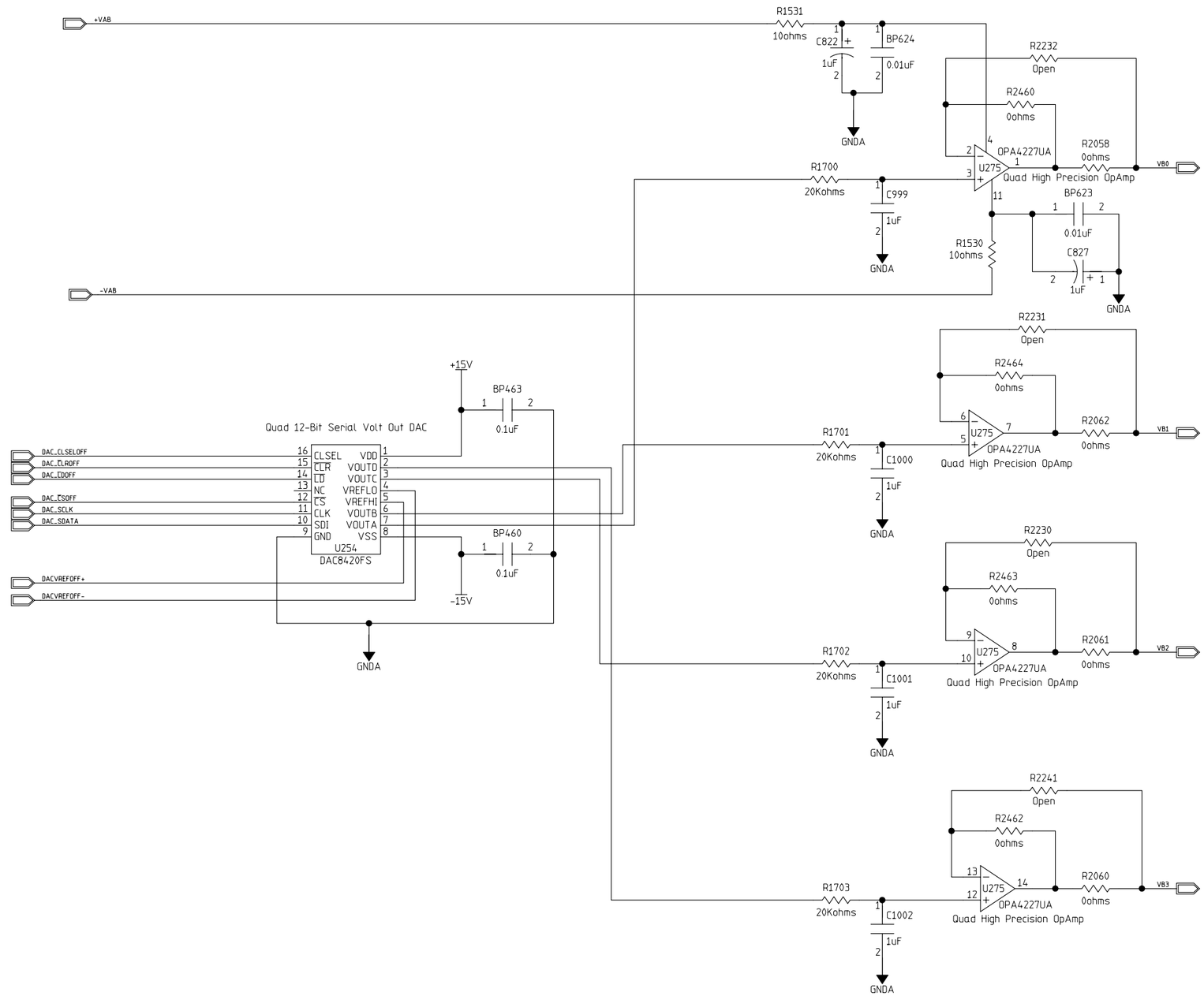
Level Translators

SIZE	DRAWING NUMBER	REV
D	drawing number (Schematic Page 05 of 05)	C

H=8ND; V=4LA


Top Level
Previous View
OPA4227 is good for 36V Rail-Rail
Rail Voltages are set 5V above and below Input Levels
Vout=Vin(1+Rf/Ri)
GAIN=1
Gains are set to match each bias voltage need.
DAC Output is set by VREFHI & VREFLO
Quad 12-Bit Serial Volt Out DAC
U716
DAC8420FS
Quad High Precision OpAmp
U408
OPA4227UA
+RAIL
-RAIL
+15V
-15V
GNDA
VB0
VB1
VB2
VB3
CLSEL
CLR
LD
CS
SCLK
SDI
VREFHI
VREFLO
R2290 10ohms
R2303 10ohms
R2384 20Kohms
R2377 20Kohms
R2376 20Kohms
R2375 20Kohms
R2321 Open
R2320 Open
R2319 Open
R2318 Open
R2333 4.99Kohms
R2332 4.99Kohms
R2331 4.99Kohms
R2330 4.99Kohms
C1445 1uF
BP745 0.01uF
C1389 4.7uF
C1425 1uF
BP738 0.01uF
C1446 1uF
C1388 4.7uF
C1424 1uF
C1390 4.7uF
C1426 1uF
C1391 4.7uF
C1427 1uF
C1353 0.1uF
C1354 0.1uF
MODIFIED 2006-01-31 2:30:06 PM
EED Department
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
DRAWN David Huffman DATE Nov. 3, 2005
CHECKED checked DATE date
APPROVED approved DATE date
Fermi National Accelerator Laboratory
United States Department of Energy
D:\des_camera\ccdacq_sch_monsoon\ccdacq_schematic.prj
4 Channel Buffered DAC - VSUB Ramp Control
BIAS 0,1
SIZE D
DRAWING NUMBER drawing number
Schematic Page 01 of 01
REV C
H=8ND; V=4LA



Top Level

Previous View

OFFSET DAC CHANNELS 0-3

MODFIED 2006-01-26 8:23:26 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
Page 16	DRAWN	David Huffman	DATE Nov. 3, 2005
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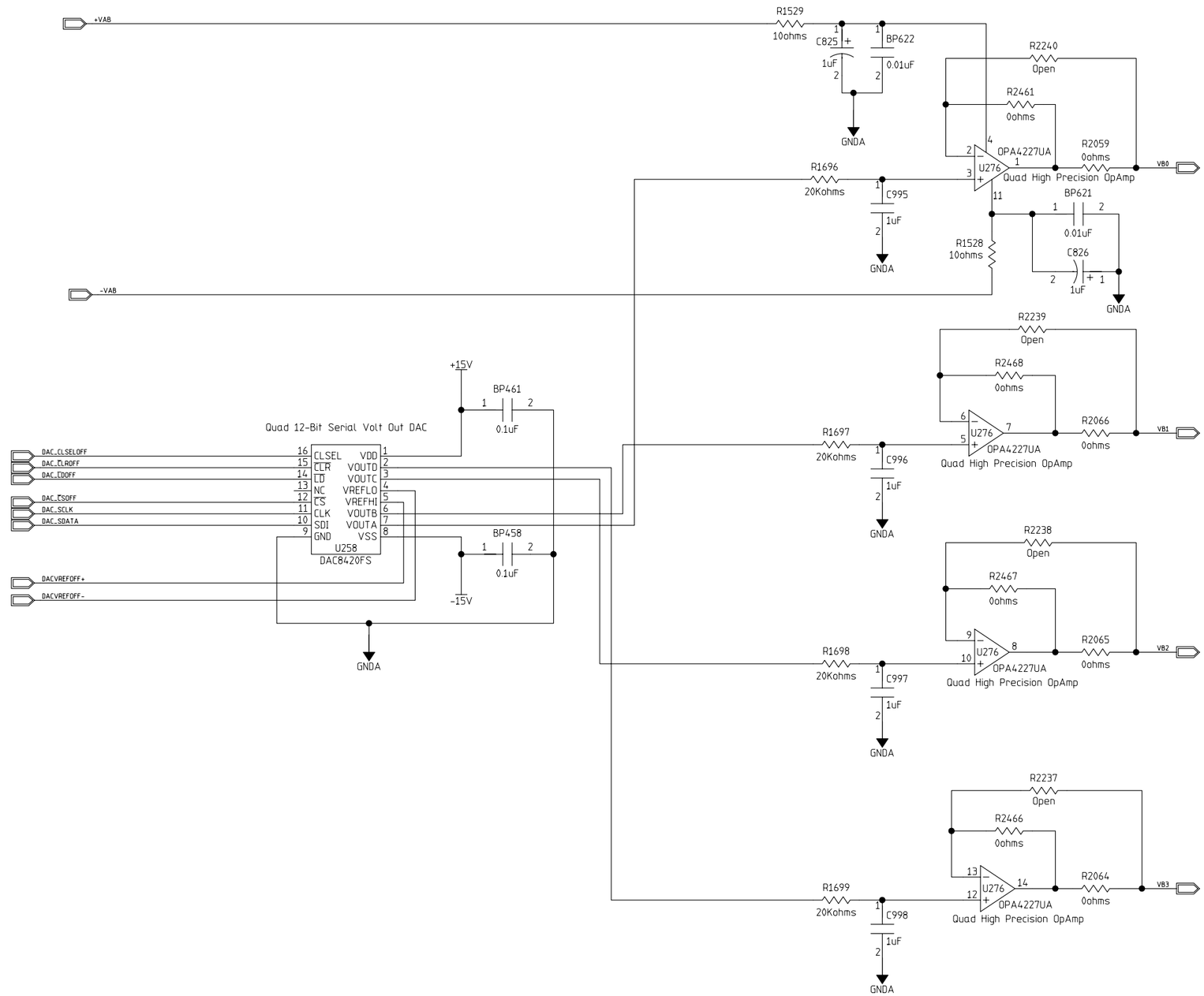
OFFSET DAC

SIZE	DRAWING NUMBER	REV
D	drawing number (Schematic Page 01 of 01)	C

H=8ND; V=4LA



Top Level

Previous View

OFFSET DAC CHANNELS 4-7

MODFIED 2006-01-26 8:23:26 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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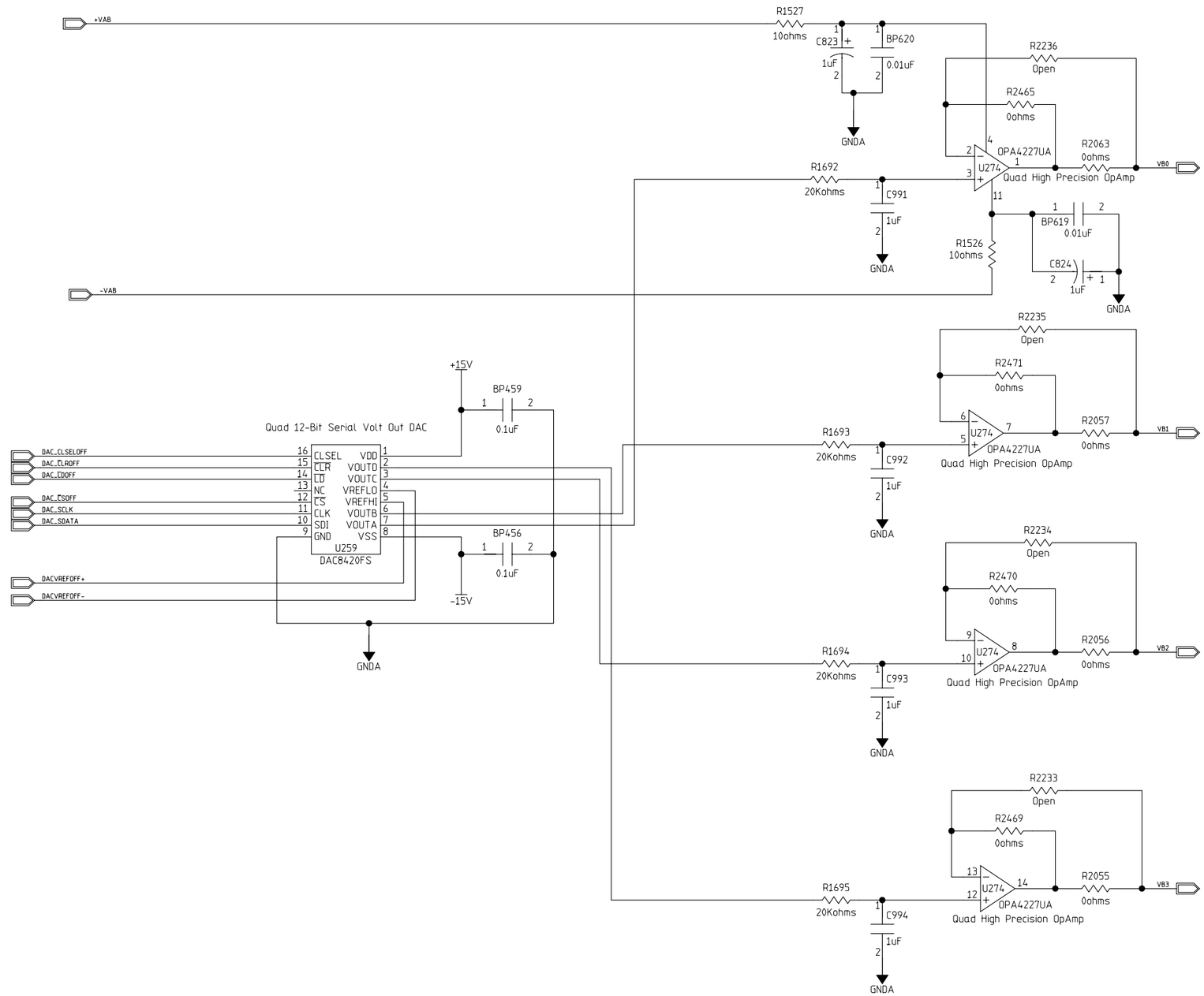
OFFSET DAC

SIZE	DRAWING NUMBER	REV
D	drawing number (Schematic Page 01 of 01)	C

H=8ND; V=4LA



Top Level

Previous View

OFFSET DAC CHANNELS 8-11

MODFIED 2006-01-26 8:23:26 AM			
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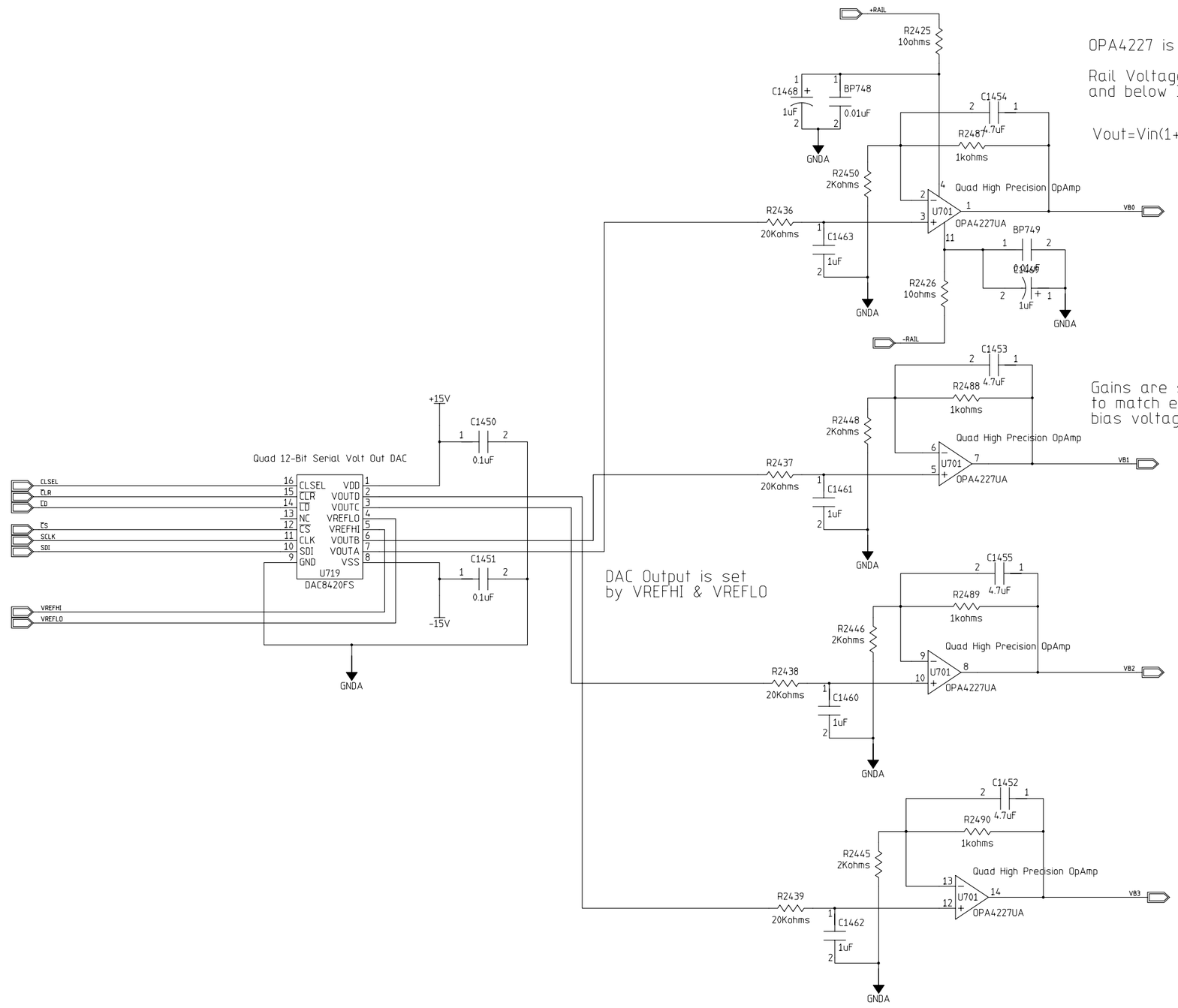
OFFSET DAC

SIZE	DRAWING NUMBER	REV
D	drawing number Schematic Page 01 of 01	C

H=8ND; V=4LA



Top Level

Previous View

MODIFIED 2006-01-30 7:51:46 AM			
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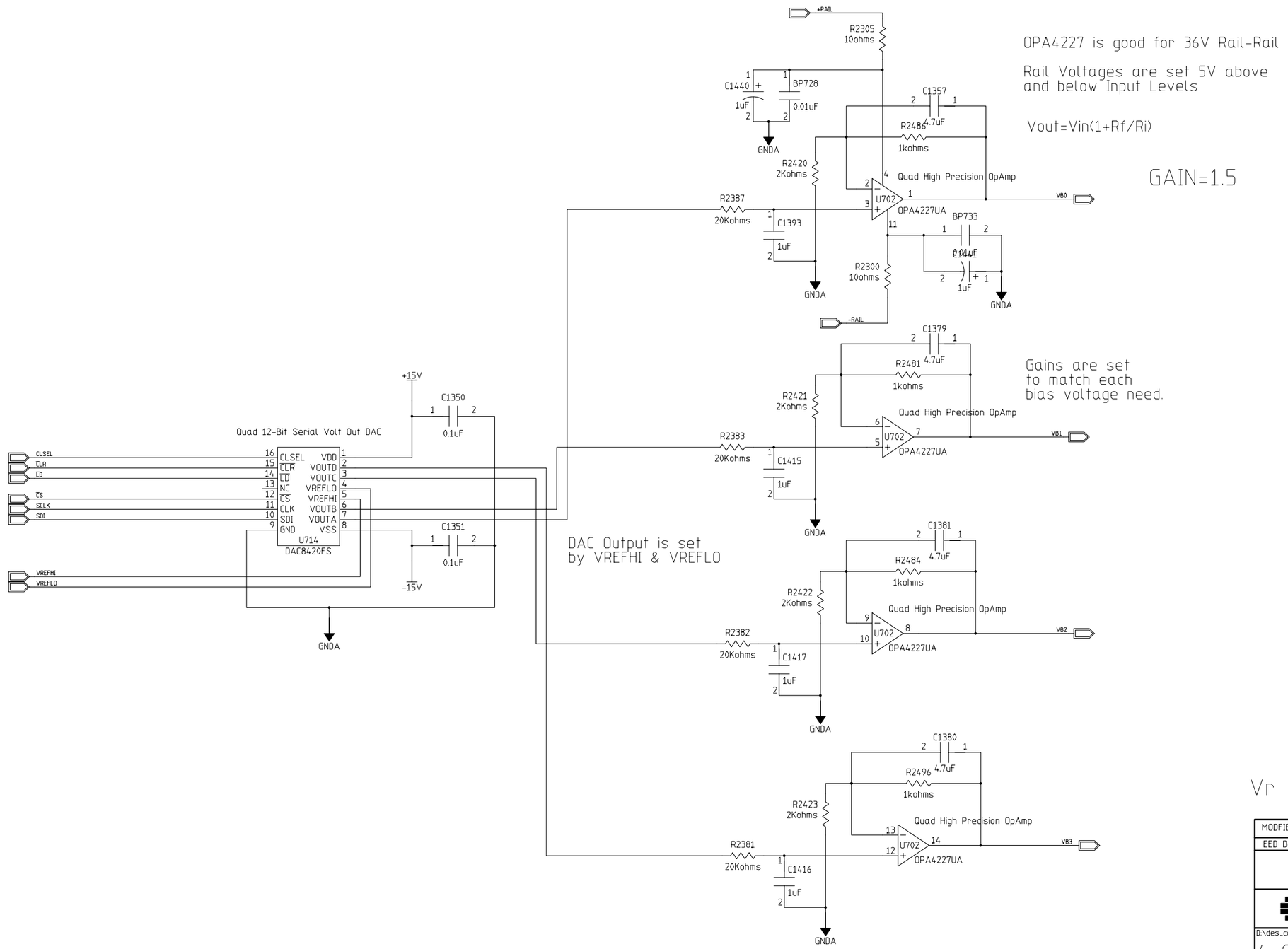
4 Channel Buffer DAC - VR

SIZE	DRAWING NUMBER	REV
D	drawing number (Schematic Page 01 of 01)	C

H=8ND; V=4LA

Top Level

Previous View



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above
and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=1.5

Gains are set
to match each
bias voltage need.

Vr BIAS CHANNELS 20-23

MODFIED 2006-01-30 7:51:46 AM			
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4 Channel Buffer DAC - VR

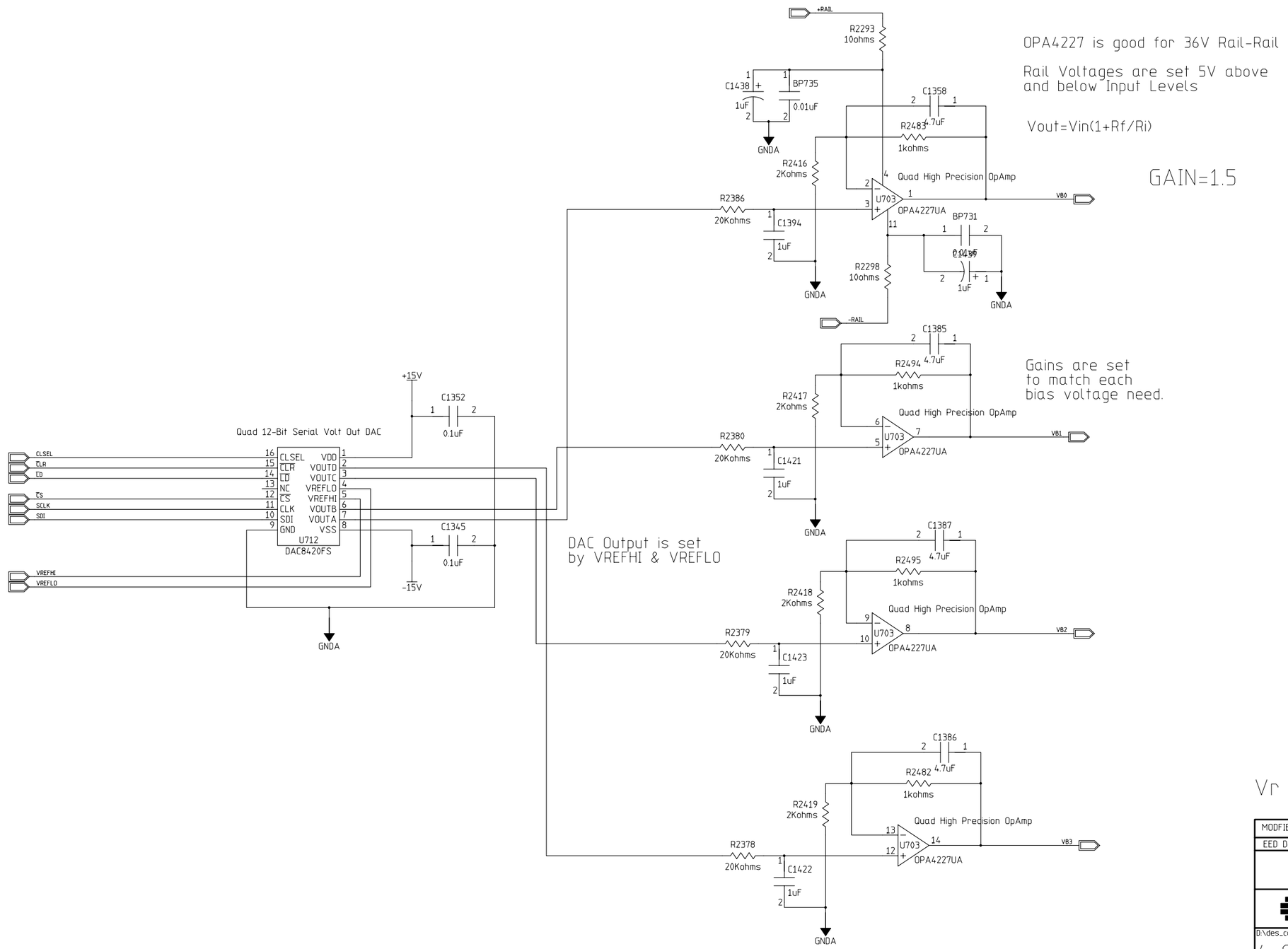
SIZE	DRAWING NUMBER	REV
D	drawing number	C

Schematic Page 01 of 01

H:8ND; V:4LA

Top Level

Previous View



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above
and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=1.5

Gains are set
to match each
bias voltage need.

Vr BIAS CHANNELS 24-27

MODFIED 2006-01-30 7:51:46 AM			
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4 Channel Buffer DAC - VR

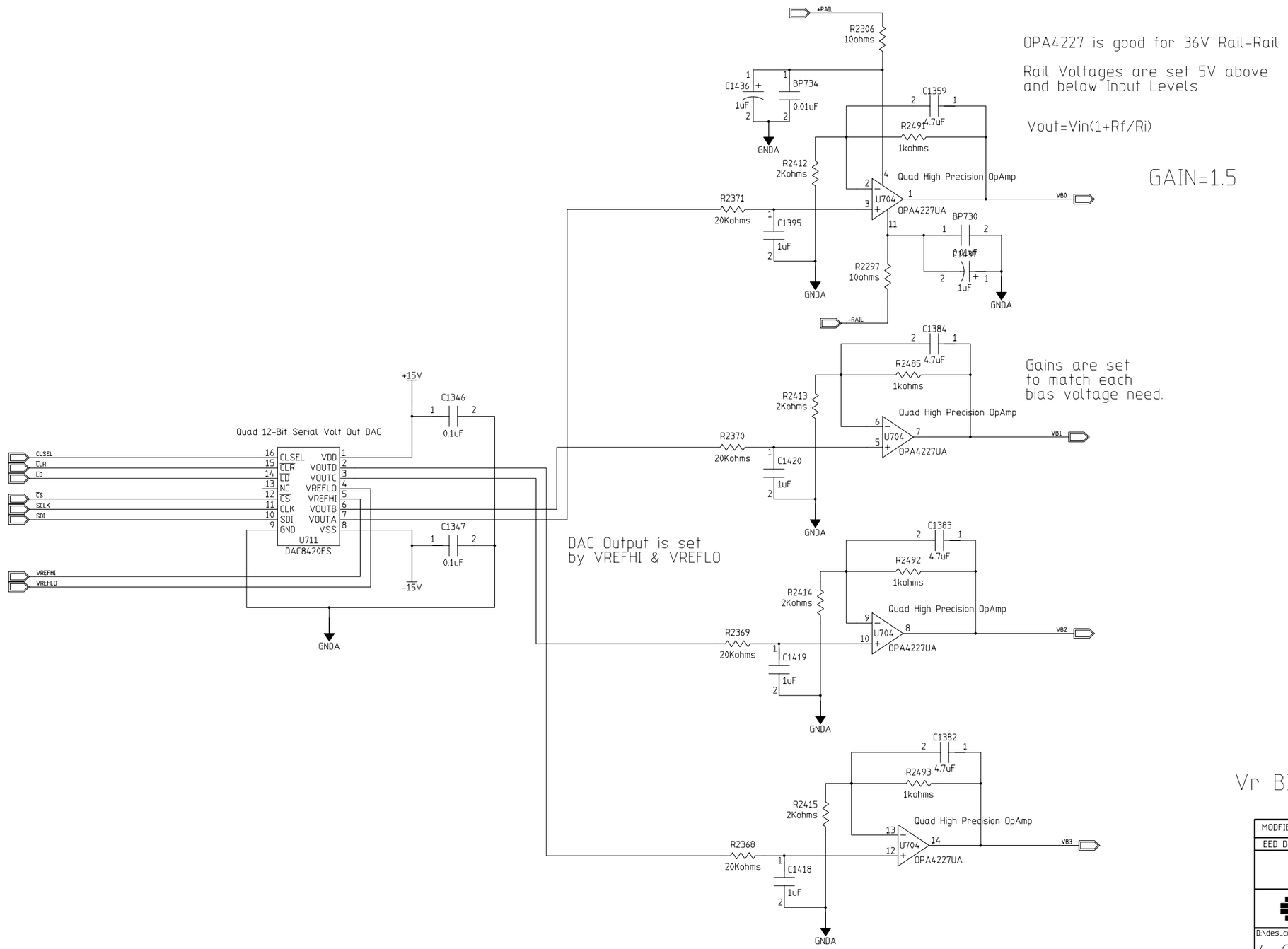
SIZE	DRAWING NUMBER	REV
D	drawing number	C

Schematic Page 01 of 01

H:8ND; V:4LA

Top Level

Previous View



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=1.5

Gains are set to match each bias voltage need.

DAC Output is set by VREFHI & VREFLO

Vr BIAS CHANNELS 28-31

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4 Channel Buffer DAC - VR

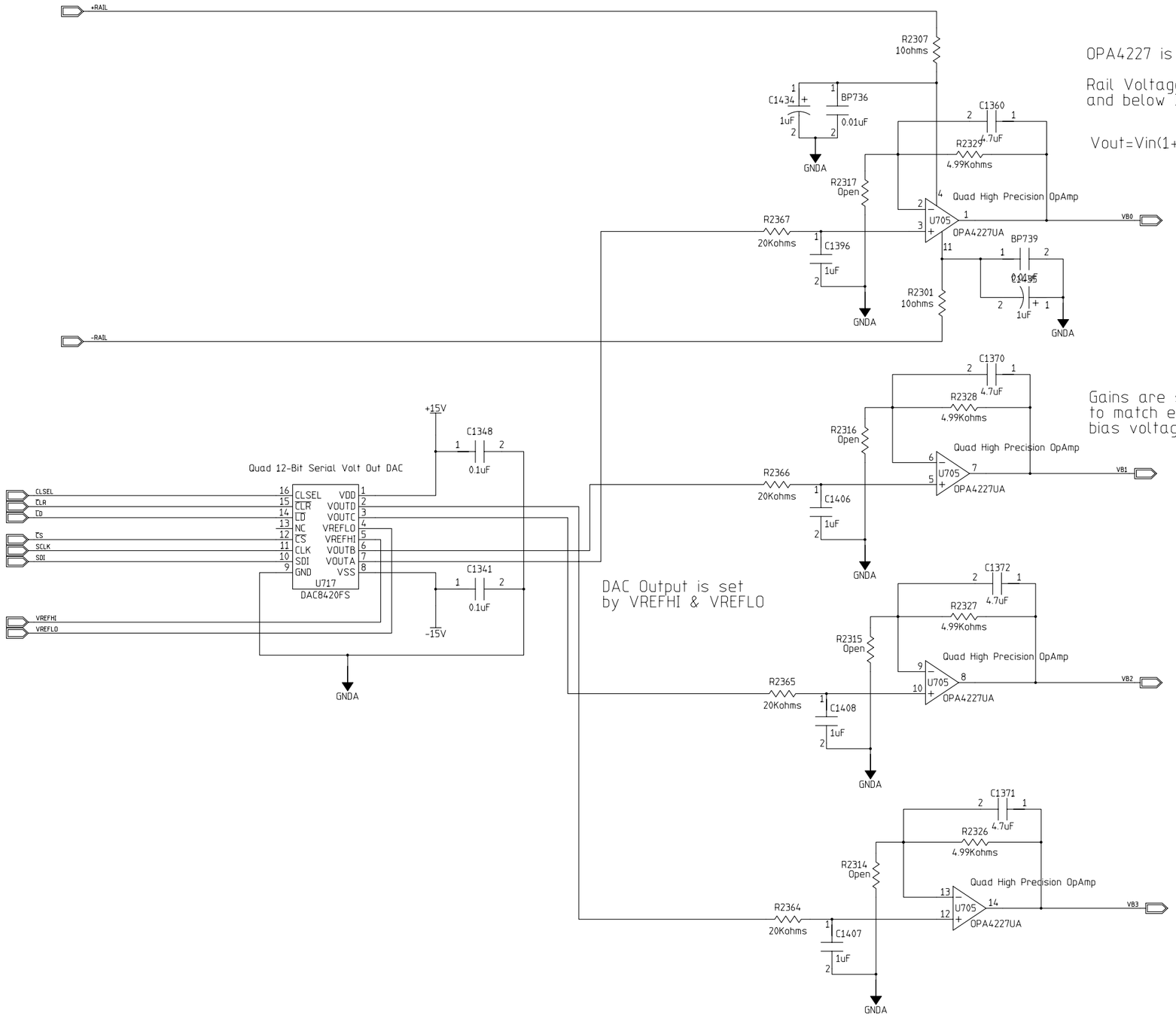
SIZE	DRAWING NUMBER	REV
D	drawing number	C

Schematic Page 01 of 01

H:8ND; V:4LA

Top Level

Previous View



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=1.0

Gains are set to match each bias voltage need.

DAC Output is set by VREFHI & VREFLO

Vog BIAS CHANNELS 32-35

MODFIED 2006-01-26 8:28:40 AM			
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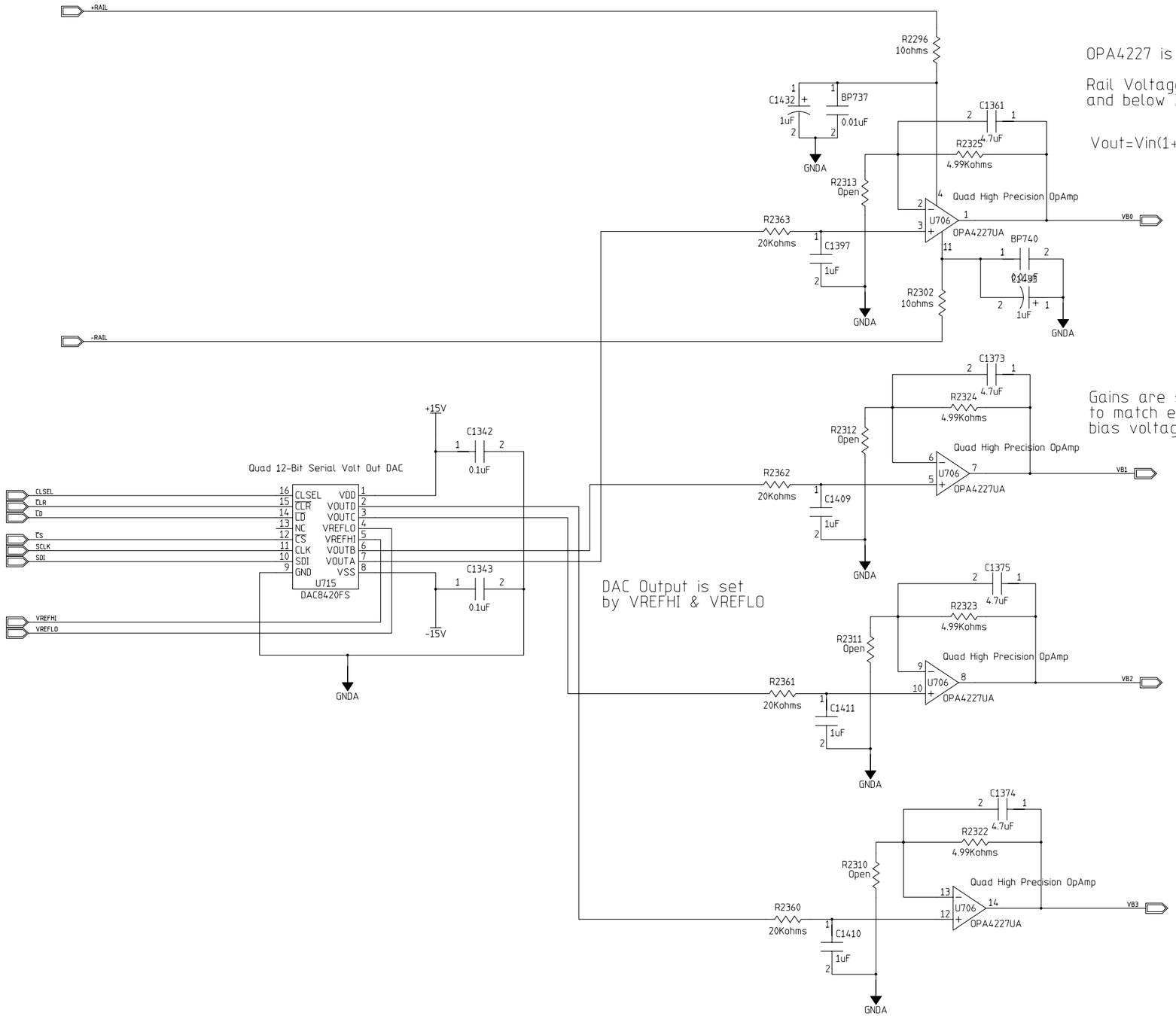
4 Channel Buffer DAC - Vog

SIZE	DRAWING NUMBER	REV
D	drawing number Schematic Page 01 of 01	C

H=8ND; V=4LA



Top Level

Previous View

OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above
and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=1.0

Gains are set
to match each
bias voltage need.

Vog BIAS CHANNELS 36-39

MODFIED 2006-01-26 8:28:40 AM			
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	APPROVED	approved	DATE date

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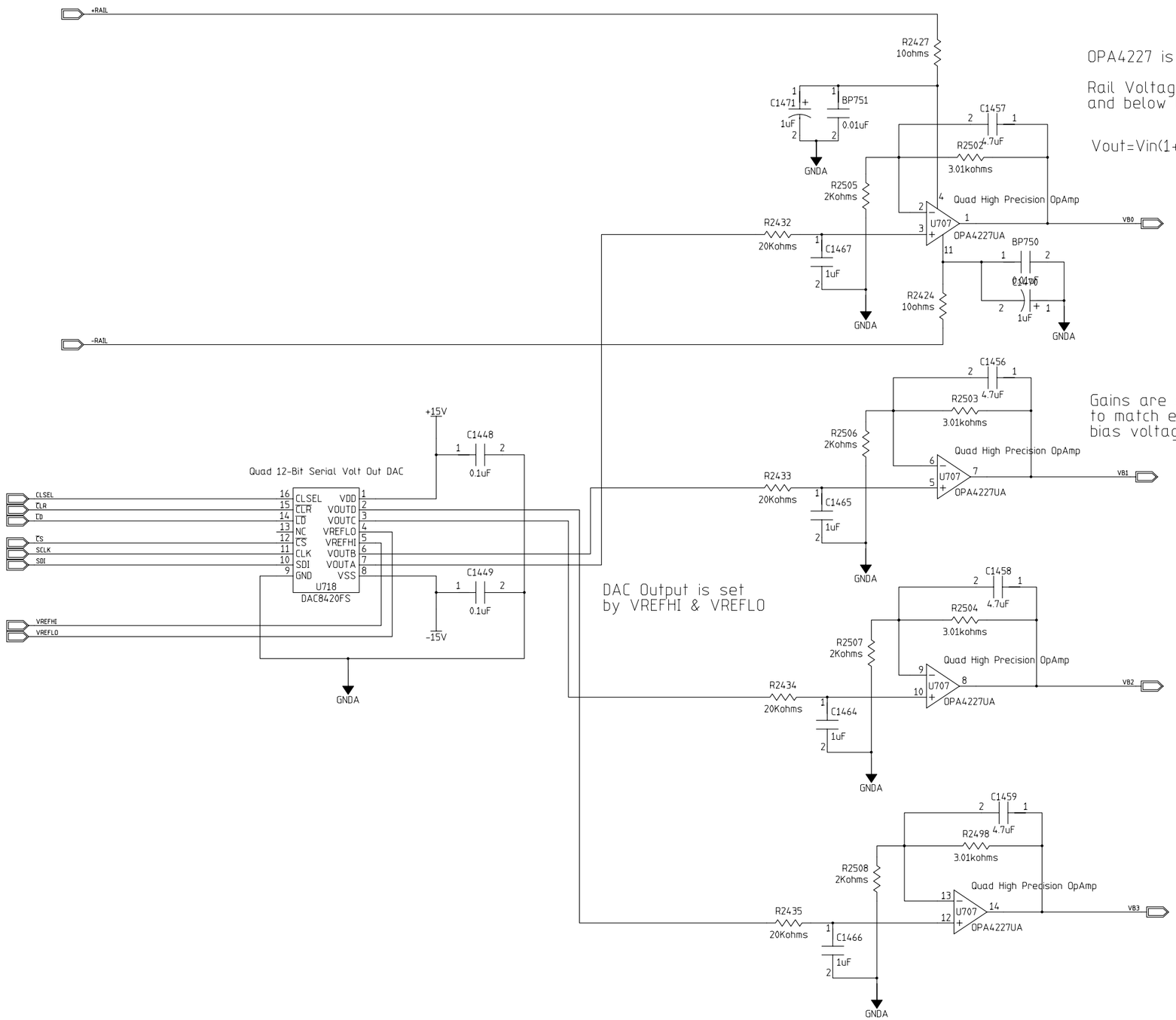
4 Channel Buffer DAC - Vog

SIZE	DRAWING NUMBER	REV
D	drawing number Schematic Page 01 of 01	C

H=8ND; V=4LA



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=2.5

Gains are set to match each bias voltage need.

DAC Output is set by VREFHI & VREFLO

Top Level

Previous View

Vdd BIAS CHANNELS 40-43

MODFIED 2006-01-30 7:57:26 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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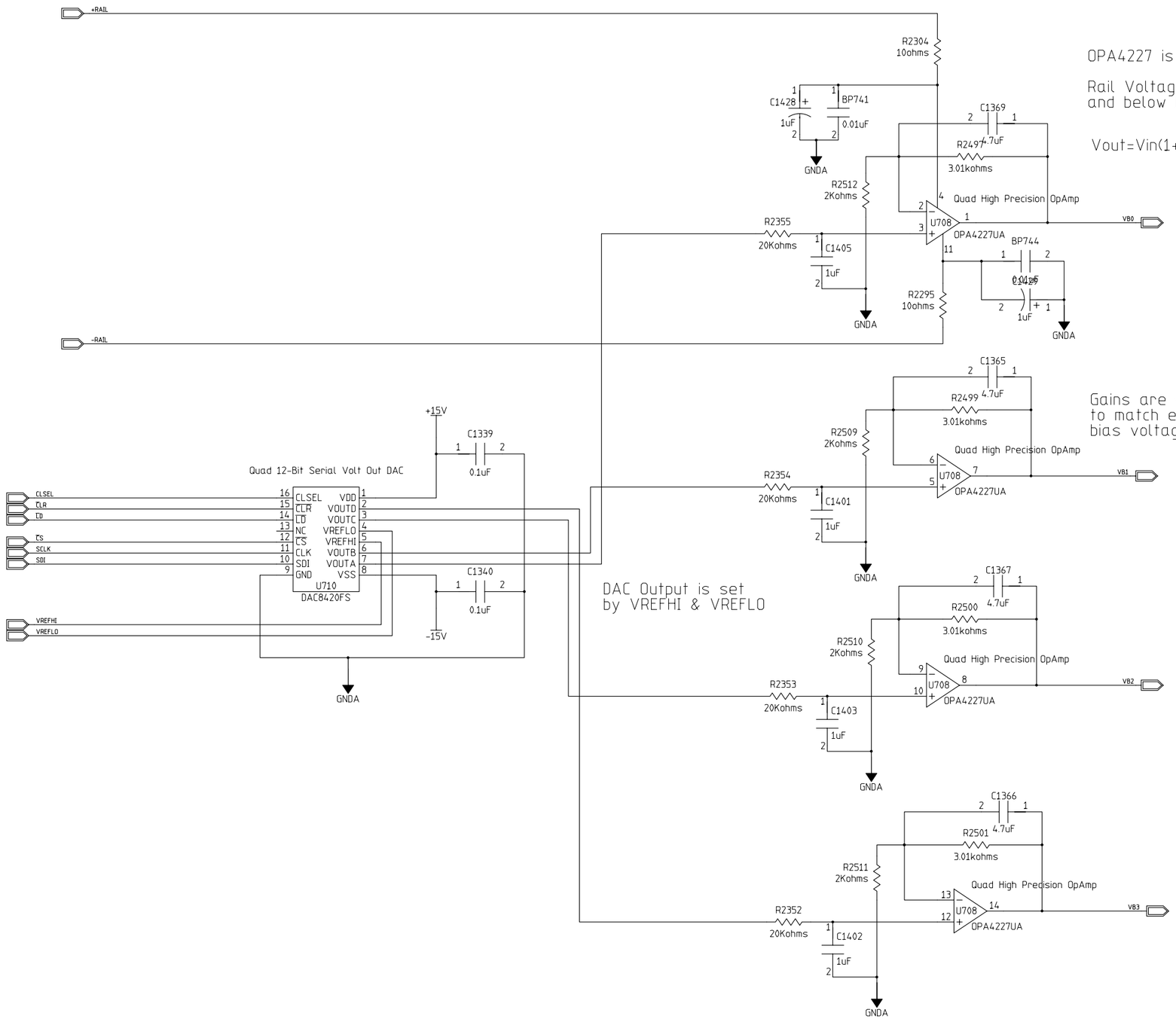
4 Channel Buffered DAC - VDD

SIZE	DRAWING NUMBER	REV
D	drawing number Schematic Page 01 of 01	C

H=8ND; V=4LA



OPA4227 is good for 36V Rail-Rail

Rail Voltages are set 5V above
and below Input Levels

Vout=Vin(1+Rf/Ri)

GAIN=2.5

Gains are set
to match each
bias voltage need.

Vdd BIAS CHANNELS 44-47

MODFIED 2006-01-30 7:57:26 AM			
EED Department	ORIGINATOR	Mark Kozlovsky	DATE 2005/11/03
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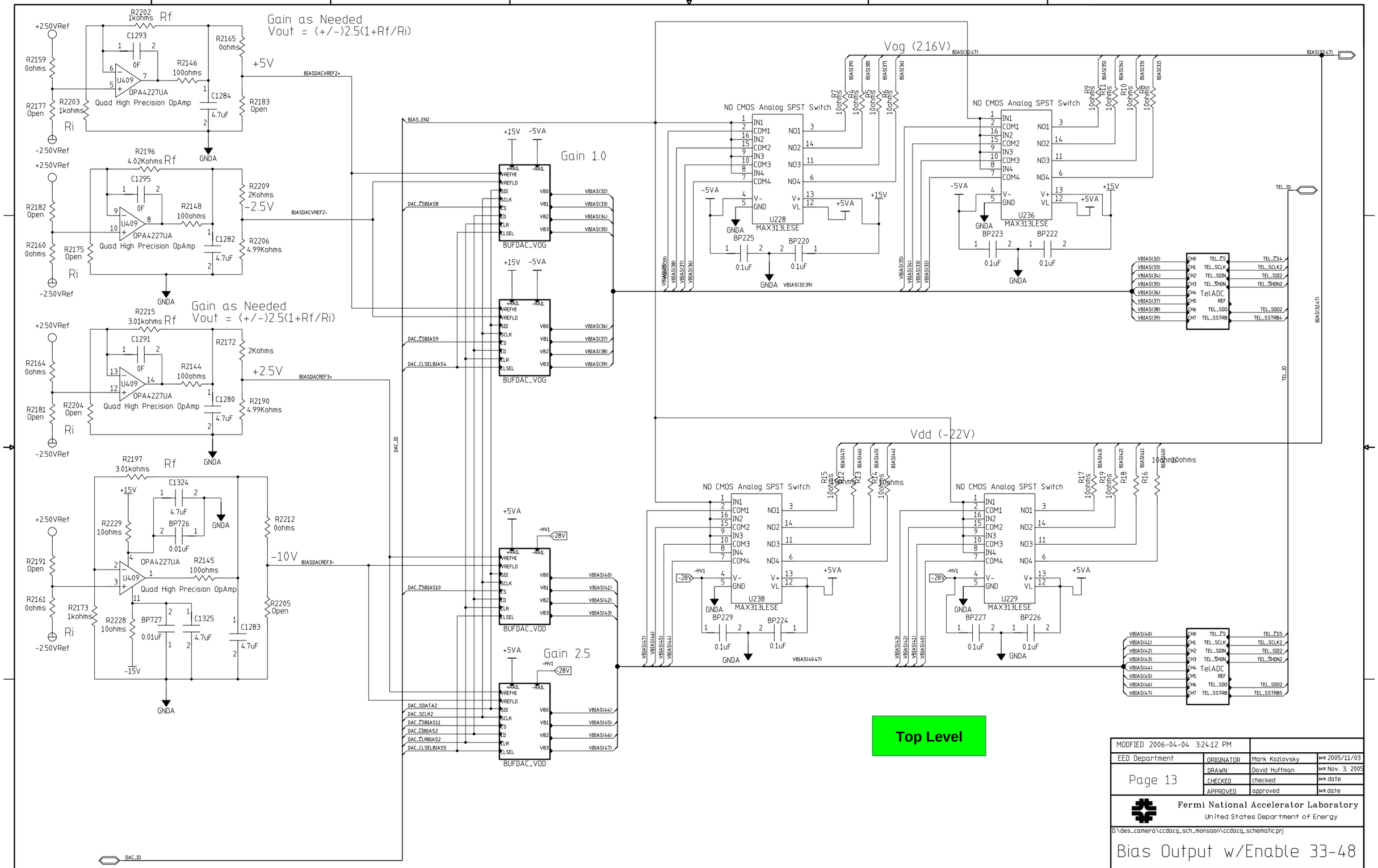
4 Channel Buffered DAC - VDD

SIZE	DRAWING NUMBER	REV
D	drawing number Schematic Page 01 of 01	C

H=8ND; V=4LA



MODFIED 2006-04-04 3:24:12 PM			
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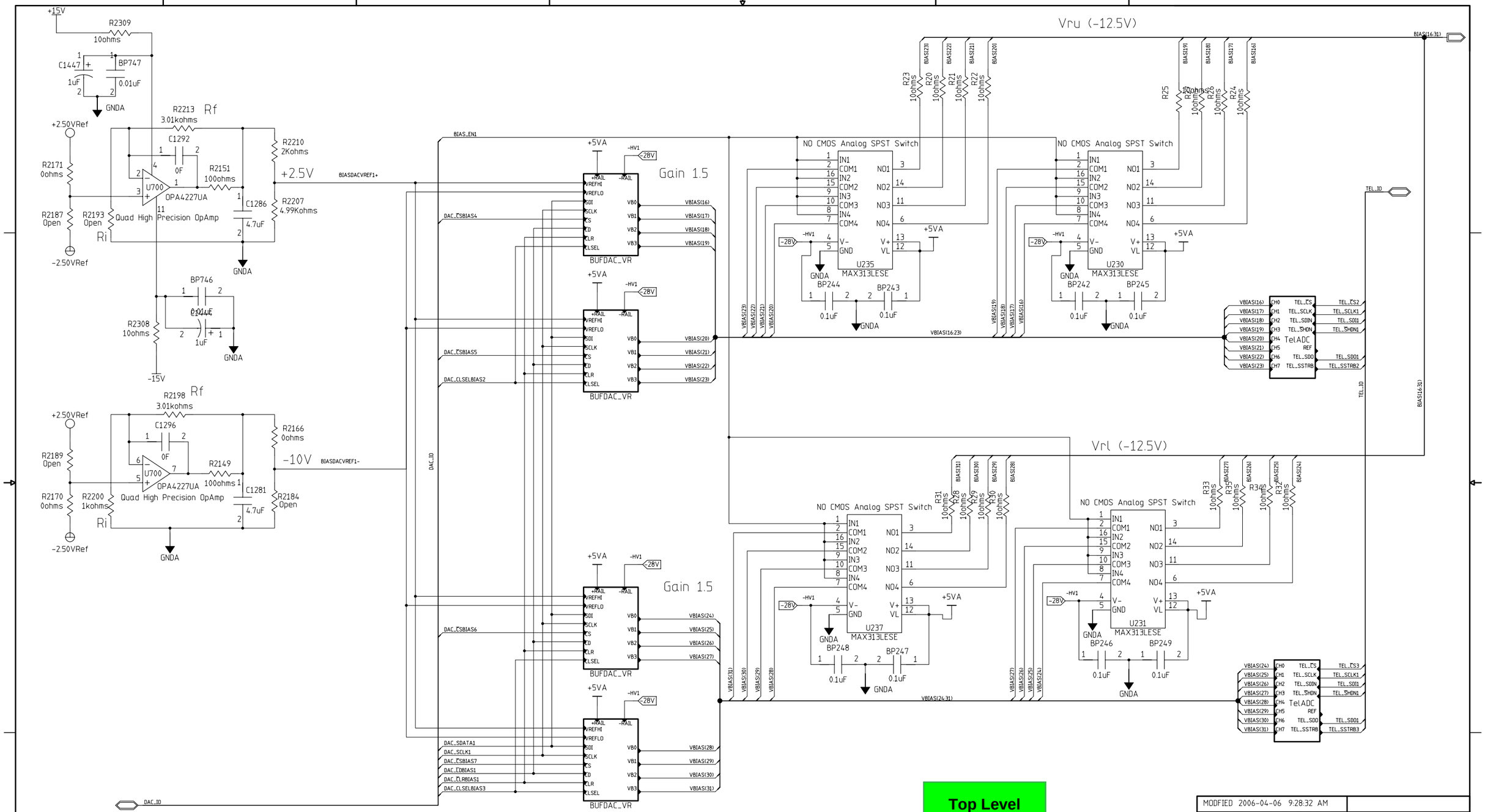
Bias Output w/Enable 33-48

SIZE	DRAWING NUMBER	REV
D	Schematic Page 01 of 01 drawing number	C

H=8ND; V=4LA



MODIFIED 2006-04-06 9:28:32 AM

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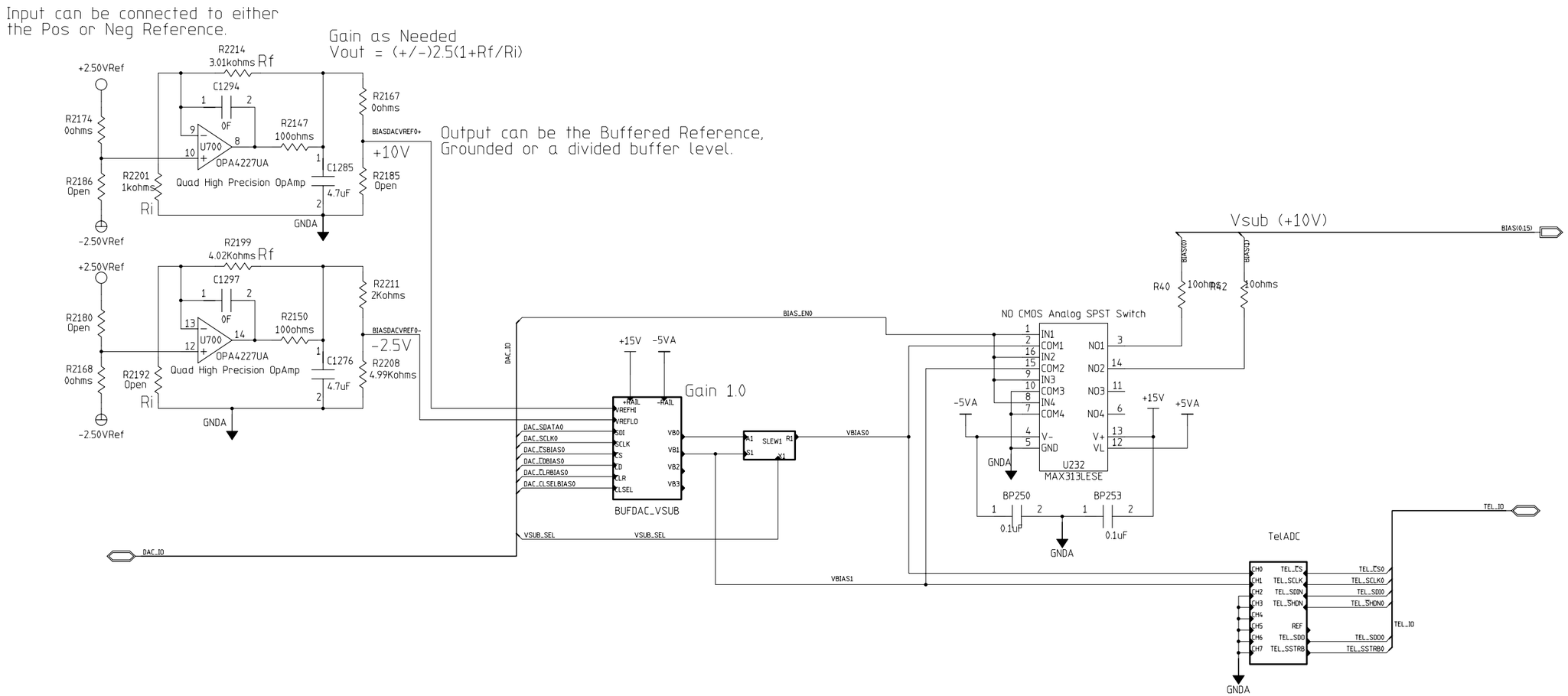
Bias Output w/Enable 17-32

SIZE	DRAWING NUMBER		REV
D	drawing number	Schematic Page 01 of 01	C

H=BND. V=4LA

Top Level



MODFIED 2006-04-06 9:28:36 AM			
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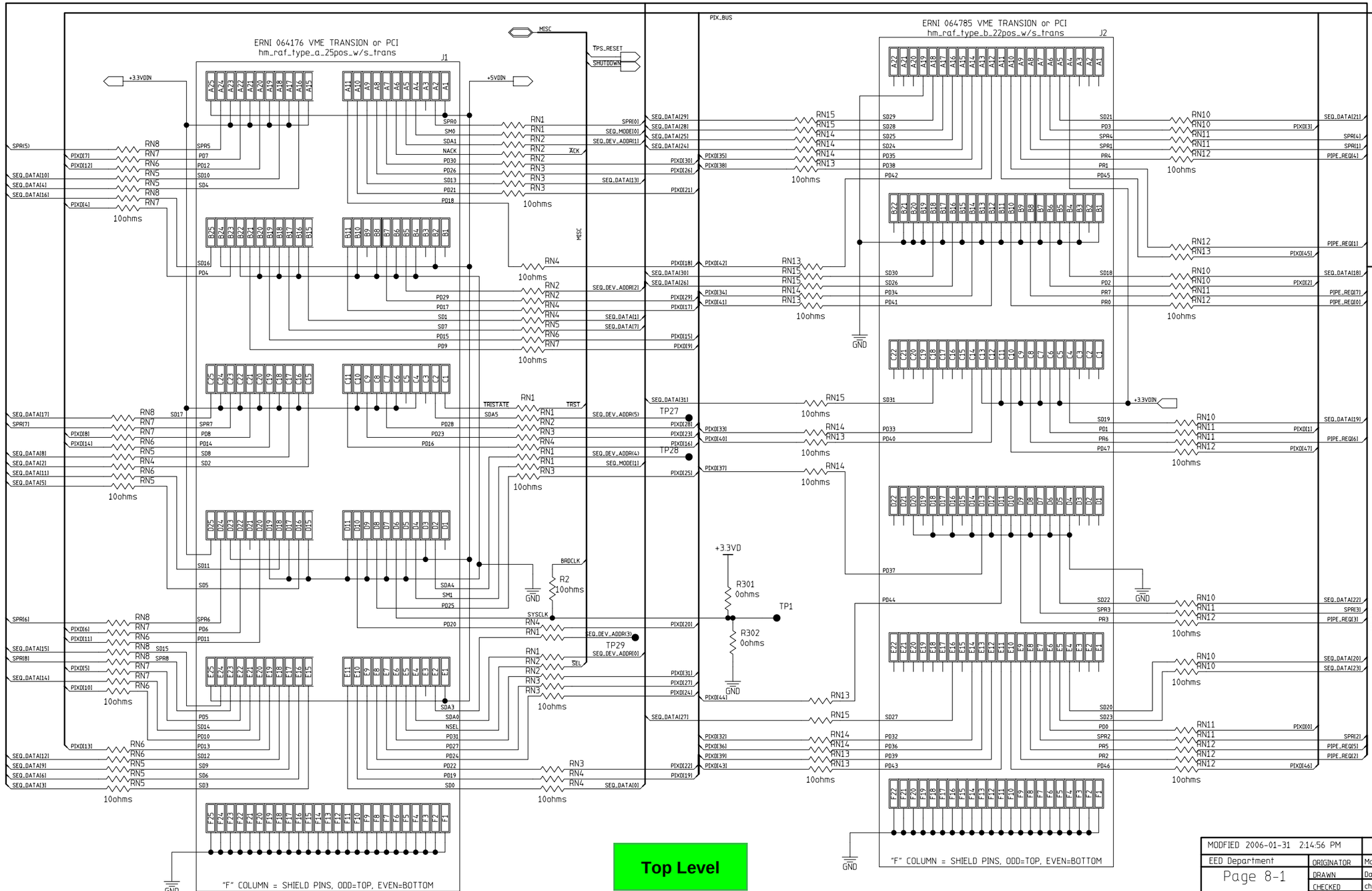
Bias Output w/Enable 1-16

SIZE	DRAWING NUMBER		REV
D	drawing number	Schematic Page 01 of 01	C

H=BND; V=4LA



Top Level

MODIFIED 2006-01-31 2:14:56 PM			
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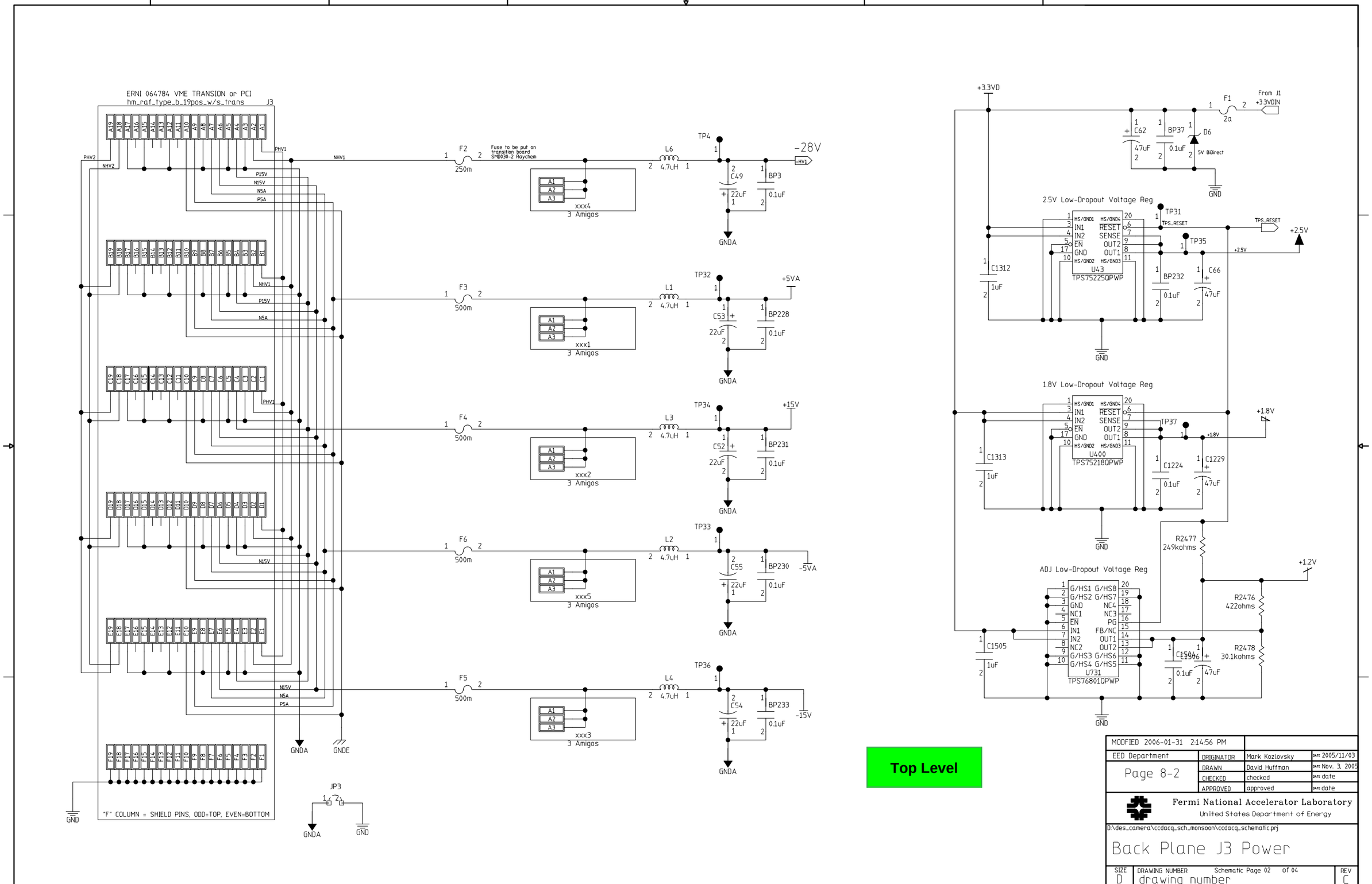
Back Plane J1 J2

SIZE	DRAWING NUMBER		REV
D	drawing number	Schematic Page 01 of 04	C

H:8ND; V:4LA


ERNI 064784 VME TRANSION or PCI
hm_raf_type_b_19pos_w/s_trans
J3
"F" COLUMN = SHIELD PINS, ODD=TOP, EVEN=BOTTOM
PHV1
PHV2
NHV1
NHV2
P15V
N15V
N5A
P5A
F2 250m
F3 500m
F4 500m
F6 500m
F5 500m
Fuse to be put on transition board SM0030-2 Raychem
L6 4.7uH
L1 4.7uH
L3 4.7uH
L2 4.7uH
L4 4.7uH
TP4
TP32
TP34
TP33
TP36
-28V
+5VA
+15V
-5VA
-15V
-HV1
C49 22uF
C53 22uF
C52 22uF
C55 22uF
C54 22uF
BP3 0.1uF
BP228 0.1uF
BP231 0.1uF
BP230 0.1uF
BP233 0.1uF
xxx4
xxx1
xxx2
xxx5
xxx3
3 Amigos
A1
A2
A3
GNDA
GNDE
GND
JP3
+3.3VD
From J1
+3.3VDIN
F1 2a
C62 47uF
BP37 0.1uF
D6 5V BiDirect
2.5V Low-Dropout Voltage Reg
TP31
TPS_RESET
TP35
+2.5V
C1312 1uF
BP232 0.1uF
C66 47uF
U43
TPS75225QPWP
HS/GND1
IN1
IN2
EN
GND
HS/GND2
HS/GND4
RESET
SENSE
OUT2
OUT1
HS/GND3
1.8V Low-Dropout Voltage Reg
TP37
+1.8V
C1313 1uF
C1224 0.1uF
C1229 47uF
U400
TPS75218QPWP
R2477 249kohms
ADJ Low-Dropout Voltage Reg
+1.2V
R2476 422ohms
R2478 30.1kohms
C1505 1uF
C1506 0.1uF
C1506 47uF
U731
TPS76801QPWP
G/HS1
G/HS2
GND
NC1
EN
IN1
IN2
NC2
G/HS3
G/HS4
G/HS8
G/HS7
NC4
NC3
PG
FB/NC
OUT1
OUT2
G/HS6
G/HS5
Top Level
MODFIED 2006-01-31 2:14:56 PM
EED Department
Page 8-2
ORIGINATOR Mark Kozlovsky DATE 2005/11/03
DRAWN David Huffman DATE Nov. 3, 2005
CHECKED checked DATE date
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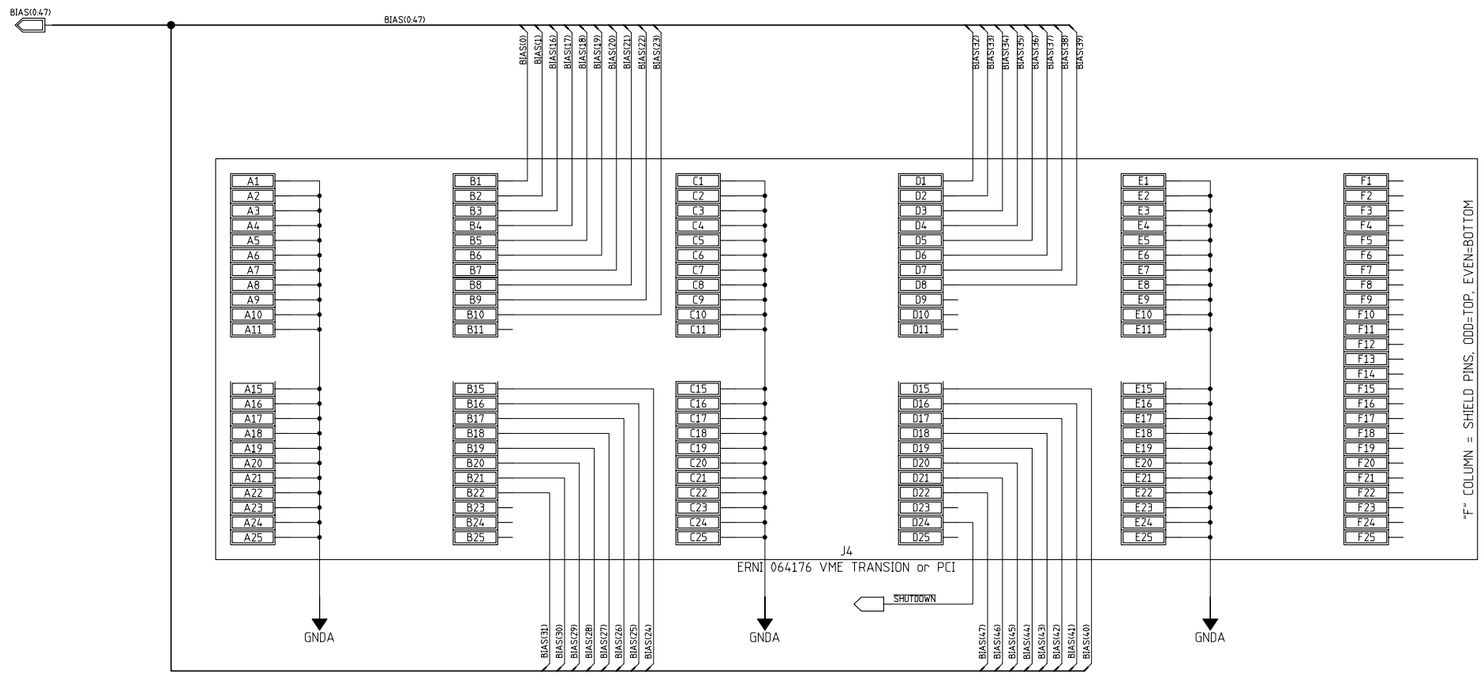
D:\des_camera\ccdacq_sch_monsoon\ccdacq_schematic.prj
Back Plane J3 Power
SIZE D
DRAWING NUMBER drawing number
Schematic Page 02 of 04
REV C
H=8ND; V=4LA

Top Level



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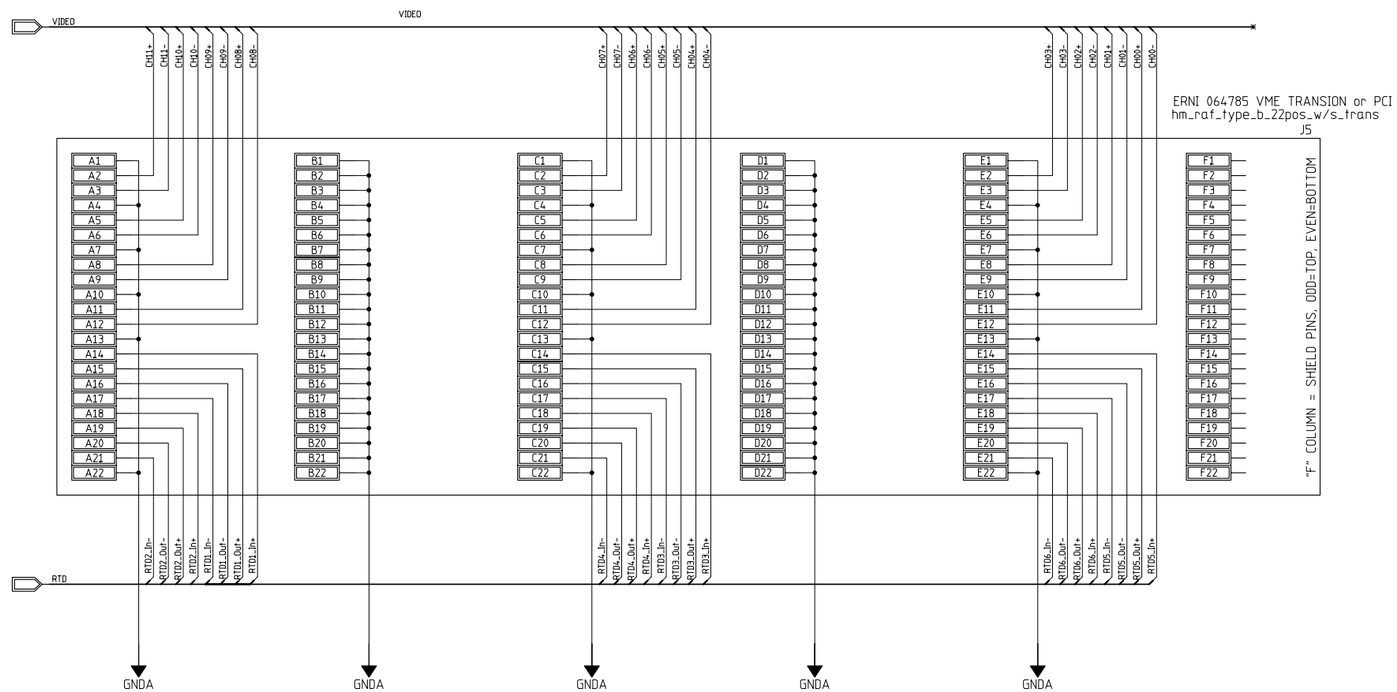
DIGITAL OUTPUTS & BIAS J4

SIZE	DRAWING NUMBER		REV
D	drawing number	Schematic Page 03 of 04	C

H=8ND; V=4LA

Top Level



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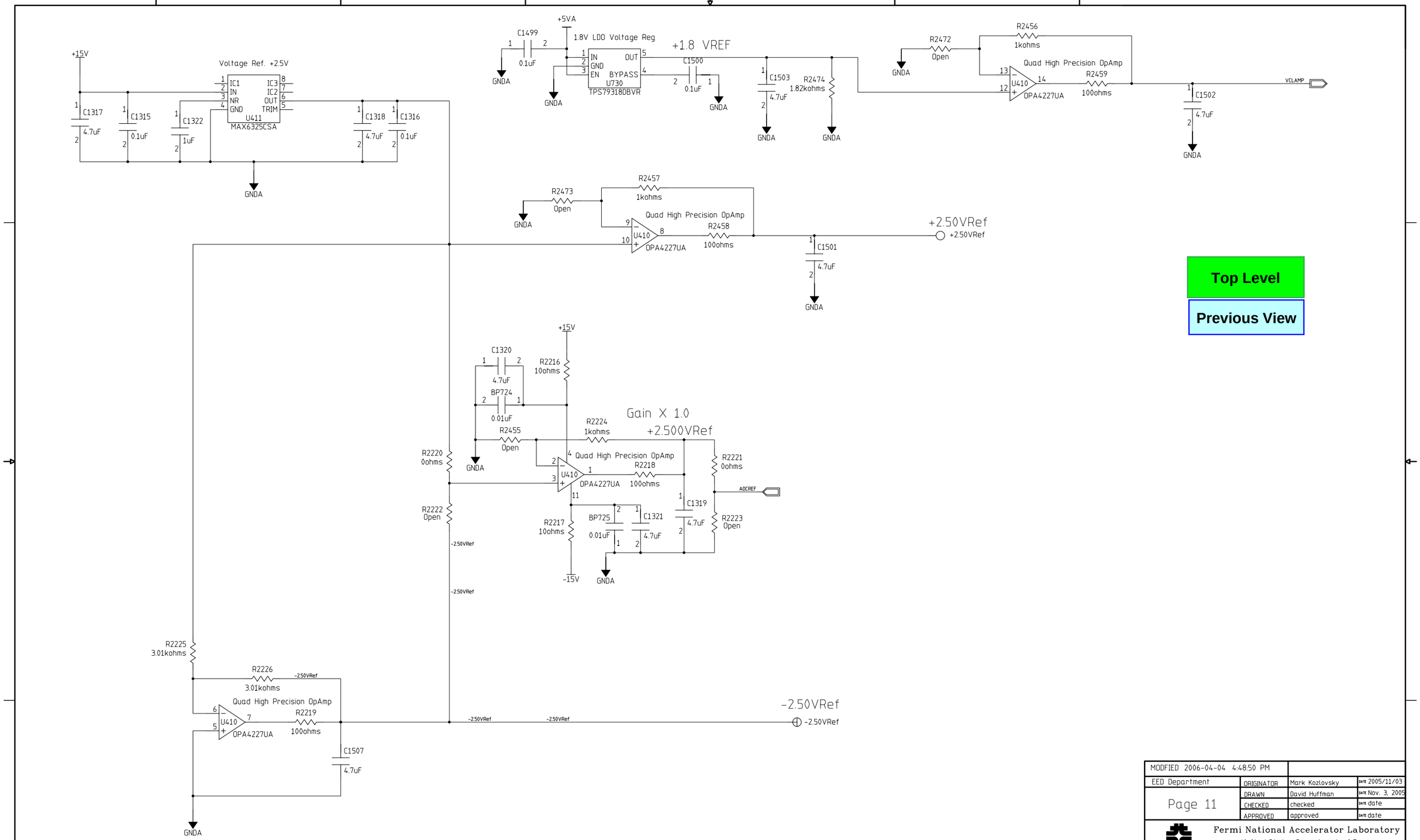
VIDEO INPUTS & RTD INPUTS J5

SIZE	DRAWING NUMBER	REV
D	Schematic Page 04 of 04 drawing number	C

H=8ND, V=4LA



Top Level

Previous View

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ADC REFERENCE and CLAMP Voltages

SIZE	DRAWING NUMBER	REV
D	drawing number Schematic Page 01 of 01	C

H=BND, V=4LA