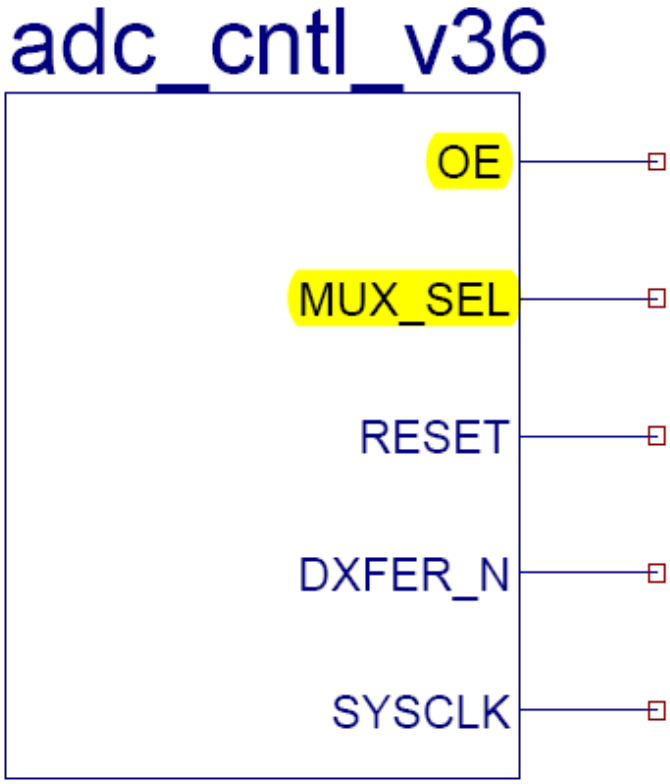
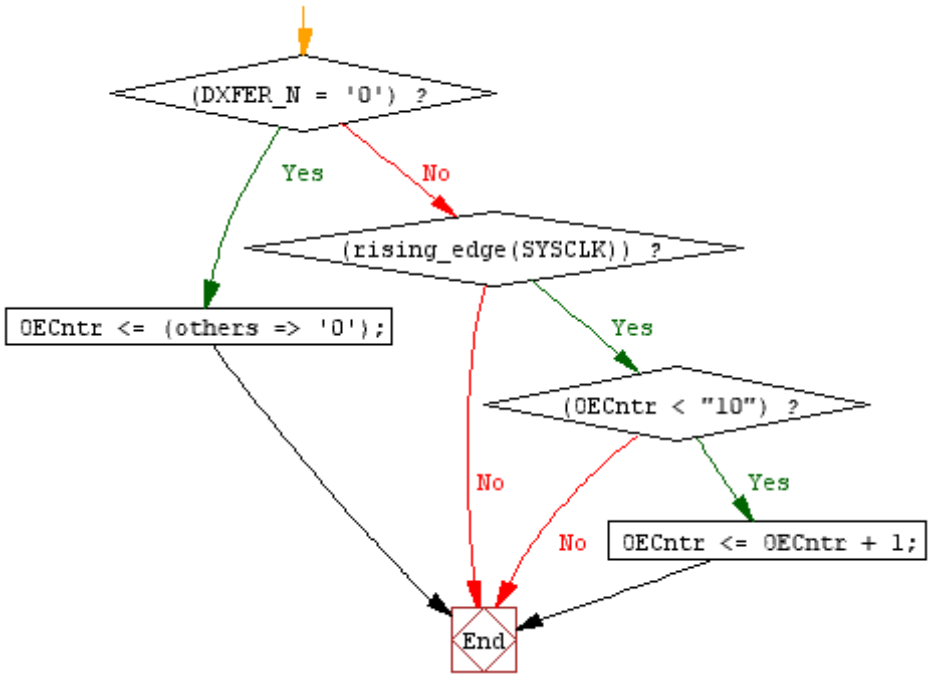
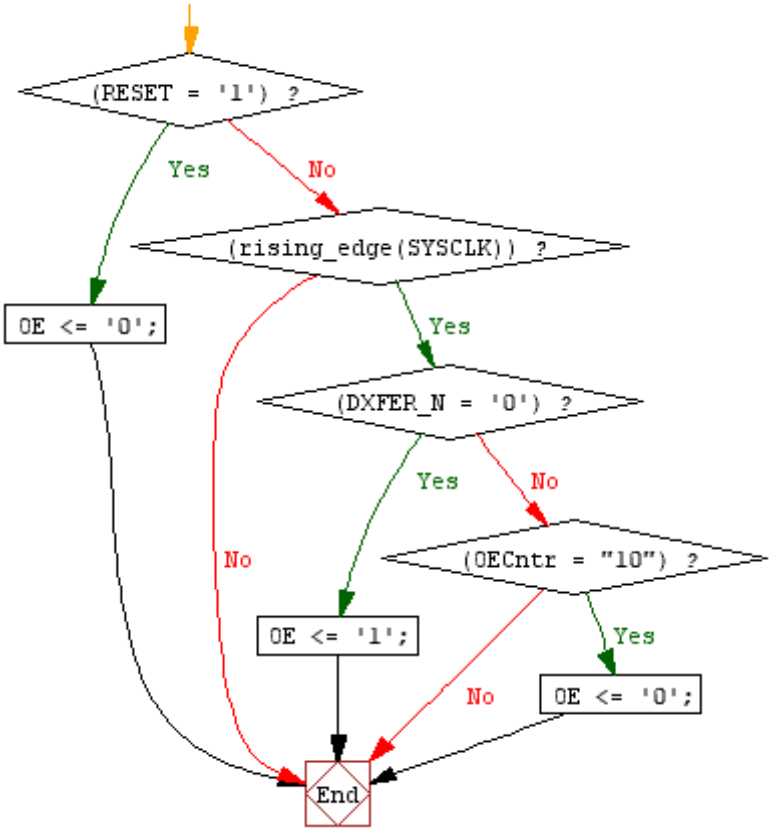
```
--- PORT DEFINITIONS :
--- CLK_EN    : OUTPUT TO THE ADC INTERFACE LOGIC TO ENABLE SERIAL ACQUISITION OF DATA
--- MUX_SEL   : SELECTS THE ACQUIRED PARALLEL DATA VIA THE MUX FOR XFER TO THE FPGA
--- OE        : ENABLES THE TRISTATE BUFFERS OF THE MUX DURING XFER
--- CTC_N     : COMMAND TO CONVERT STROBE TO BEGIN ADC CONVERSION
--- DXFER_N   : COMMAND TO XFER STROBE FROM THE FPGA
--- SYSCLK    : MASTER CLOCK SOURCE
--- RESET_N   : DISABLES THE TRISTATE BUFFERS ASYNCHRONOUSLY
--- BUSY_IN   : CASCADED BUSY SIG FROM ALL ADCs.
--- MODE_IN   : MODE SIGNAL FROM FPGA TO DETERMINE FAST / SLOW OPERATION
--- MODE_OUT  : LATCHED MODE SIGNAL TO THE ADC INTERFACE LOGIC.
--- TEST      : TEST OUTPUT THAT TOGGLES EACH CTC_N FOR STEP RESPONSE TESTING
```




```
DXFER_N   : in  std_logic;
SYSCLK    : in  std_logic;
RESET     : in  std_logic

MUX_SEL   : out std_logic;
OE        : out std_logic;
```

DxferCntr : process (DXFER_N, SYSCLK)



DxferEnable : process (RESET, SYSCLK)