```
-----------------------------------------------------------------------
-- DESCRIPTION  : 256 x 16 bit Ram bank to store various configuration data used
--              : to establish the hardware operating point.
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-- IMPLEMENTATION NOTES :
-- MEMORY MAP:
-- x00 => x0F   ADC CHANNEL 0 => 15 BANK 0 CONFIG DATA (ADC_CFG0_DATA - ?? BITS - READ / WRITE)
-- x10 => x1F   ADC CHANNEL 0 => 15 BANK 1 CONFIG DATA (ADC_CFG0_DATA - ?? BITS - READ / WRITE)
-- x20 => x2F   ADC CHANNEL 0 => 15 BANK 2 CONFIG DATA (ADC_CFG0_DATA - ?? BITS - READ / WRITE)
-- x30 => x3F   ADC CHANNEL 0 => 15 BANK 3 CONFIG DATA (ADC_CFG0_DATA - ?? BITS - READ / WRITE)
-- x40 => x4F   ADC CHANNEL 0 => 15 BANK 0 OFFSET DAC DATA (ADC_OFST_DATA - 12 BITS - READ / WRITE)
-- x50 => x5F   ADC CHANNEL 0 => 15 BANK 0 OFFSET DAC DATA (ADC_OFST_DATA - 12 BITS - READ / WRITE)
-- x60 => x6F   ADC CHANNEL 0 => 15 BANK 0 OFFSET DAC DATA (ADC_OFST_DATA - 12 BITS - READ / WRITE)
-- x70 => x7F   ADC CHANNEL 0 => 15 BANK 0 OFFSET DAC DATA (ADC_OFST_DATA - 12 BITS - READ / WRITE)
-- x80 => x9F   HV BIAS CHANNEL 0 => 31 BANK 0 SET VALUE (HVBIAS_SET_DATA - 12 BITS - READ / WRITE)
-- xA0 => xBF   HV BIAS CHANNEL 0 => 31 BANK 1 SET VALUE (HVBIAS_SET_DATA - 12 BITS - READ / WRITE)
-- xC0 => xDF   HV BIAS CHANNEL 0 => 31 TELEMETRY VALUE (HVBIAS_TEL_DATA - 12 BITS - READ / 0 BIT WRITE)
-- xE0 => XFF   HV BIAS CHANNEL 0 => 31 TELEMETRY CONFIG VALUE (HVBIAS_TCFG_DATA - 8 BITS READ / WRITE)
-----------------------------------------------------------------------
```
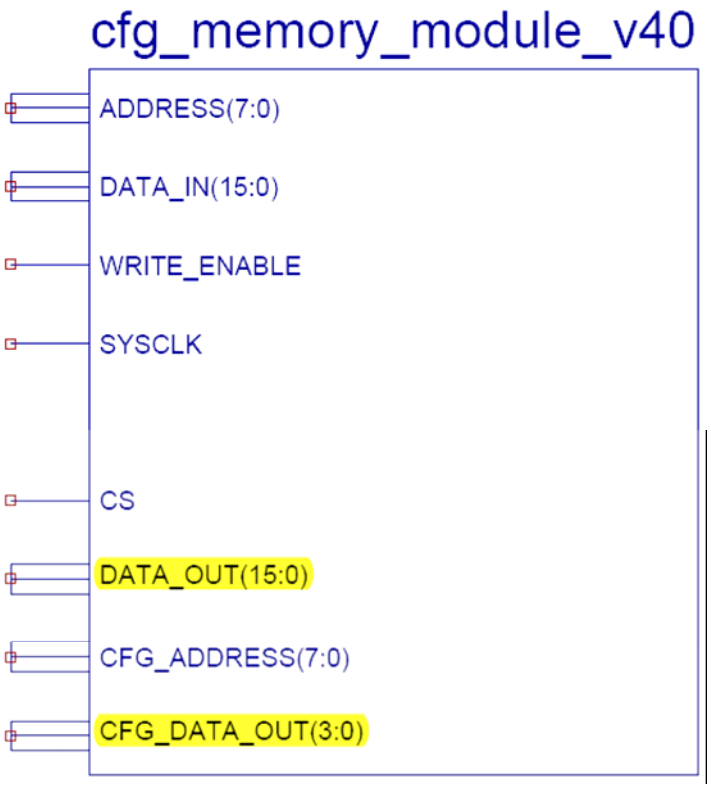
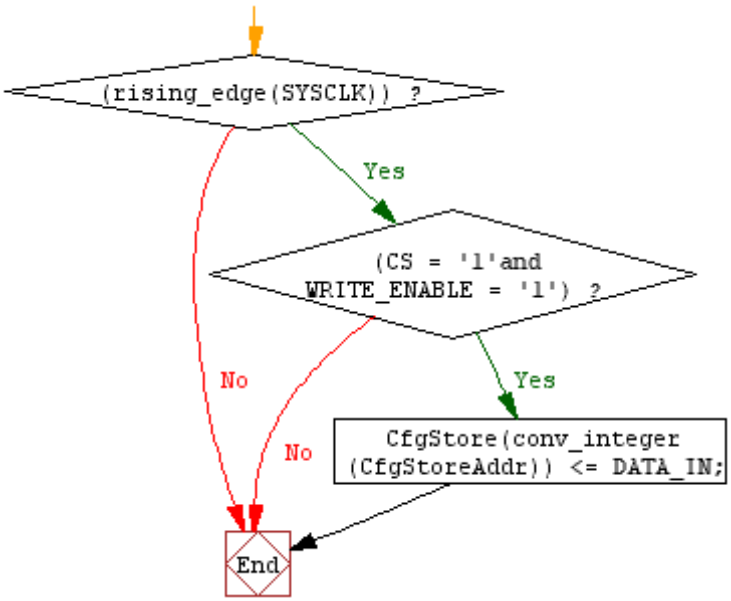
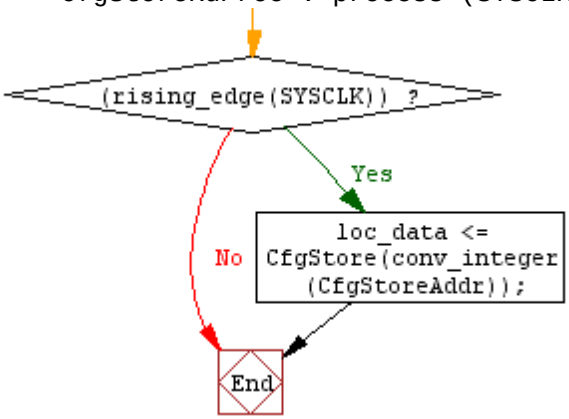




```
ADDRESS      : in  std_logic_vector(7 downto 0);
CFG_ADDRESS  : in  std_logic_vector(7 downto 0);
DATA_IN      : in  std_logic_vector(15 downto 0);
CS           : in  std_logic;
SYSCLK       : in  std_logic;
WRITE_ENABLE : in  std_logic
CFG_DATA_OUT : out std_logic_vector(3 downto 0);
DATA_OUT     : out std_logic_vector(15 downto 0);

type cfg_ram_type is array (255 downto 0) of std_logic_vector (15 downto 0);
signal CfgStore     : cfg_ram_type;                 -- Ram to store Configuration data
signal CfgStoreAddr : std_logic_vector(7 downto 0);
signal loc_data     : std_logic_vector(15 downto 0);


CfgStoreAddr <= ADDRESS when (CS = '1') else CFG_ADDRESS;
```

```
CfgStoreWrtProc : process (SYSCLK)
```




```
CfgStoreRdProc : process (SYSCLK)
```