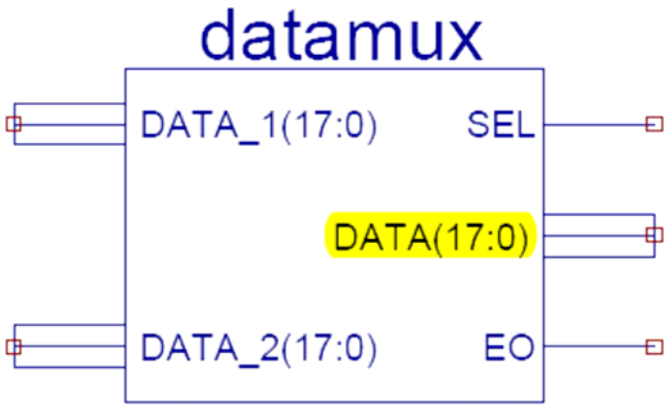
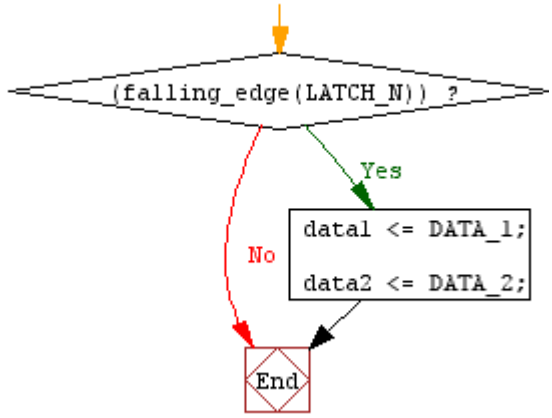
```
-----------------------------------------------------------------------
-- DESCRIPTION    :     IMPLEMENTS A BASIC ASYNCHRONOUS 18 BIT X 2 TO 1 MULTIPLEXOR
--               :   WITH TRISTATES OUTPUTS.
-----------------------------------------------------------------------
```




```
DATA_1 : in std_logic_vector(17 downto 0);
DATA_2 : in std_logic_vector(17 downto 0);
LATCH_N: in std_logic;
SEL    : in std_logic;
EO     : in std_logic;
DATA   : out std_logic_vector(17 downto 0)


signal data1, data2 : std_logic_vector(17 downto 0);

    DATA <= (others =>'Z') when (EO = '0') else
            data1 when(SEL = '0') else
            data2;


DataLatchProc : process(LATCH_N)
```