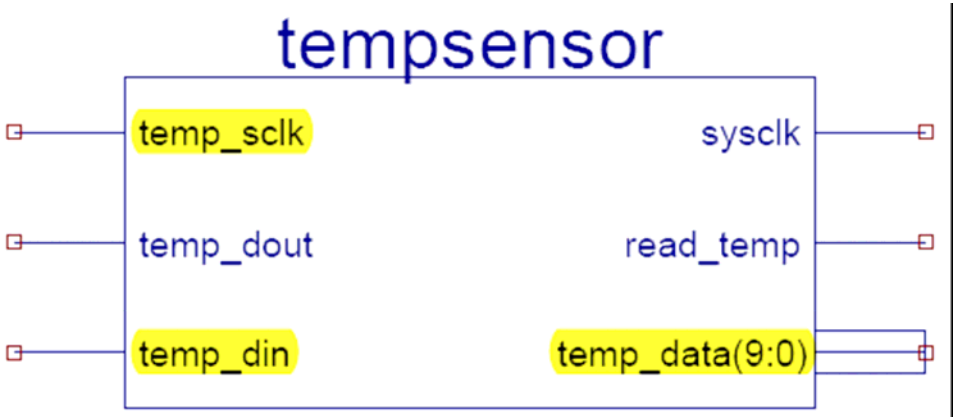
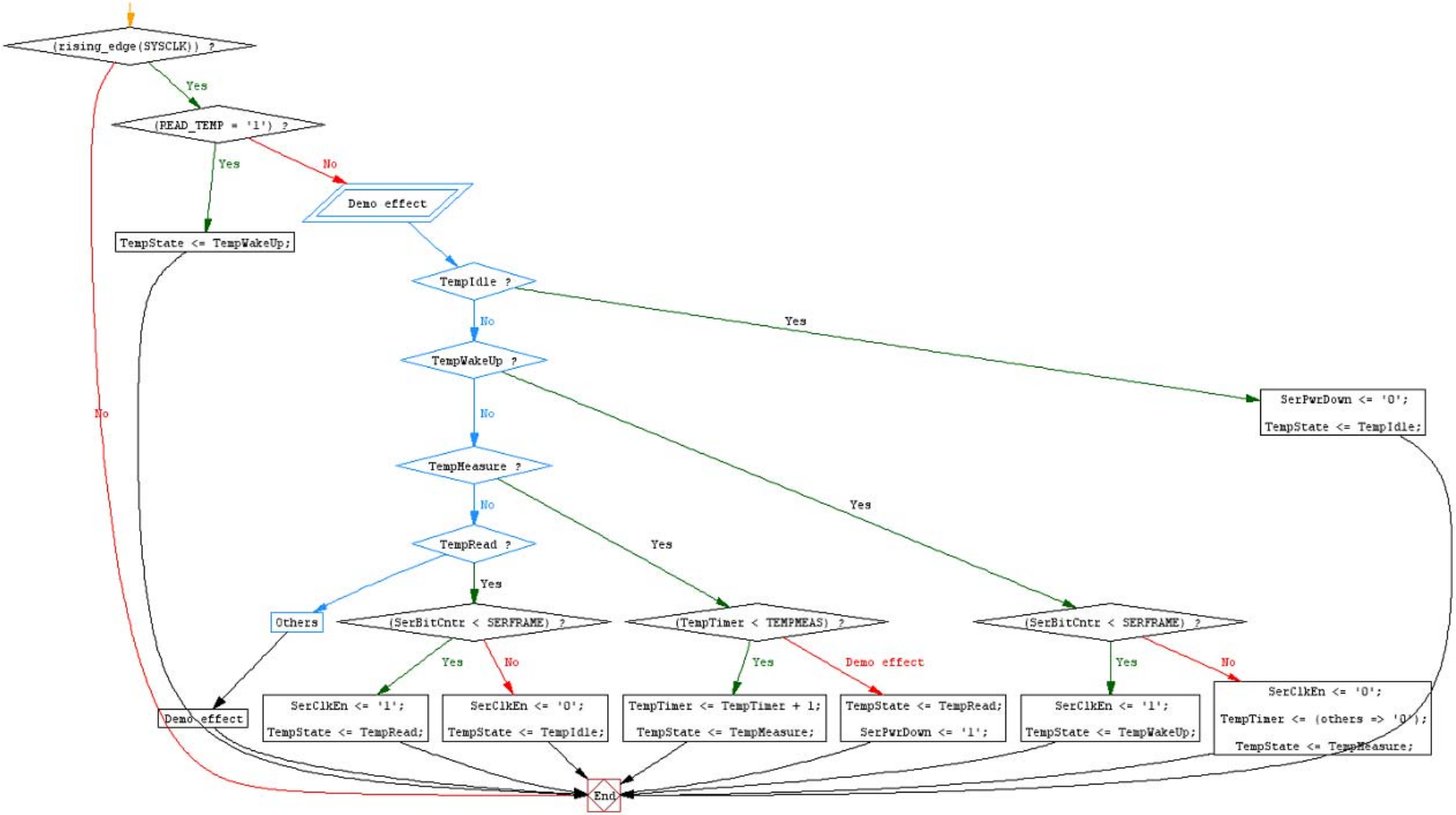
```
-----------------------------------------------------------------------
-- DESCRIPTION  :
-- INTERFACES A AD7814 3 WIRE TEMP SENSOR.
-----------------------------------------------------------------------
```



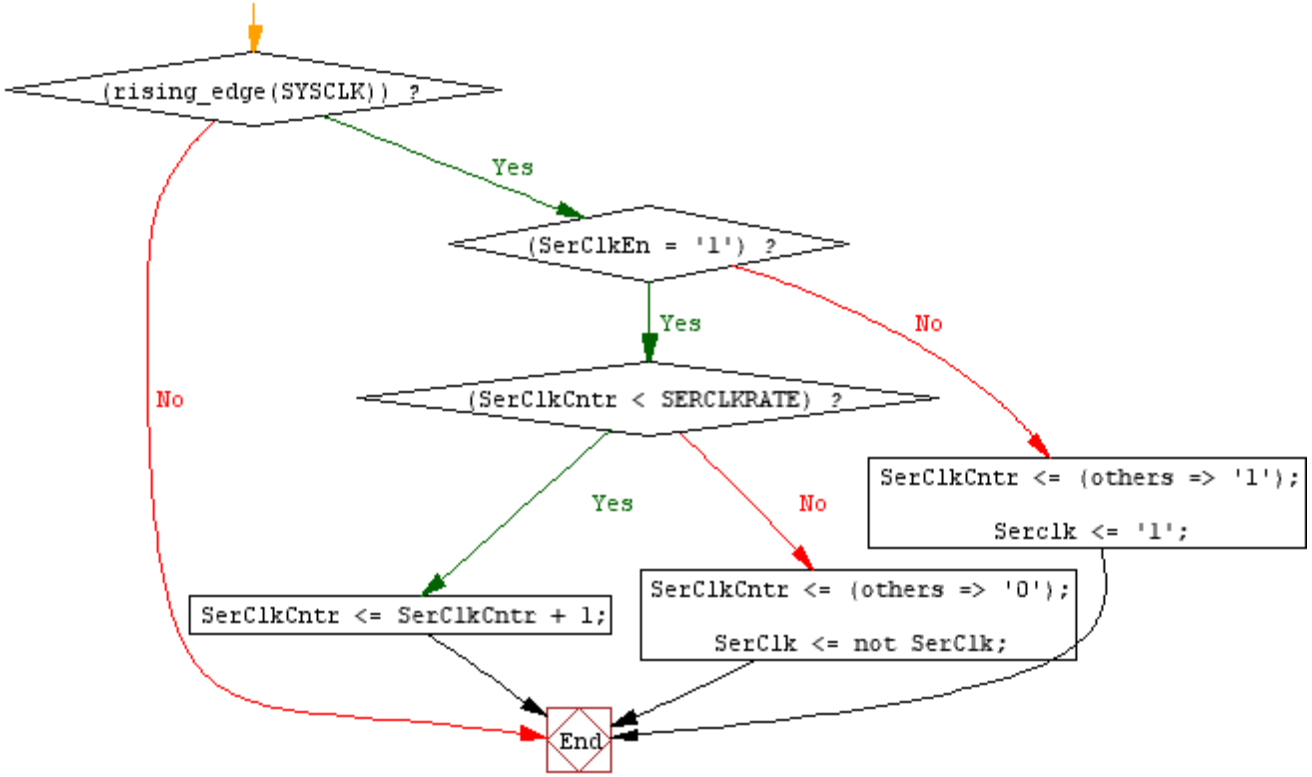

```
SYSCLK    : in  std_logic;
READ_TEMP : in  std_logic;
TEMP_DATA : out std_logic_vector(9 downto 0);
TEMP_DIN  : out std_logic;
TEMP_DOUT : in  std_logic;
TEMP_SCLK : out std_logic

constant SERCLKRATE : std_logic_vector(2 downto 0) := "010"; -- Clock period is currently set to 3 clk periods i.e 75ns per phase
constant SERFRAME   : std_logic_vector(4 downto 0) := "10000";       -- Number of bits in a serial frame
signal SerClkCntr   : std_logic_vector(2 downto 0);
signal SerBitCntr   : std_logic_vector(4 downto 0);
signal SerClk       : std_logic;                                     -- Actual serial clock signal
signal SerClkEn     : std_logic;                                     -- Enables serial clock to run
signal SerDataIn    : std_logic_vector(15 downto 0);                 -- Serial to parallel converter
signal SerDataOut   : std_logic_vector(15 downto 0);                 -- Parallel to serial converter
signal DataInLatch  : std_logic_vector(9 downto 0);                  -- Latched version of SerDataIn after acquisition.
constant TEMPMEAS   : std_logic_vector(9 downto 0) := "1111101000"; -- 1000 clock cycles is 25us.
type TempStateType is (TempIdle, TempWakeUp, TempMeasure, TempRead);
signal TempState    : TempStateType;
signal TempTimer    : std_logic_vector(9 downto 0);                  -- Timer counter to wait for sensor response
signal SerPwrDown   : std_logic;
```

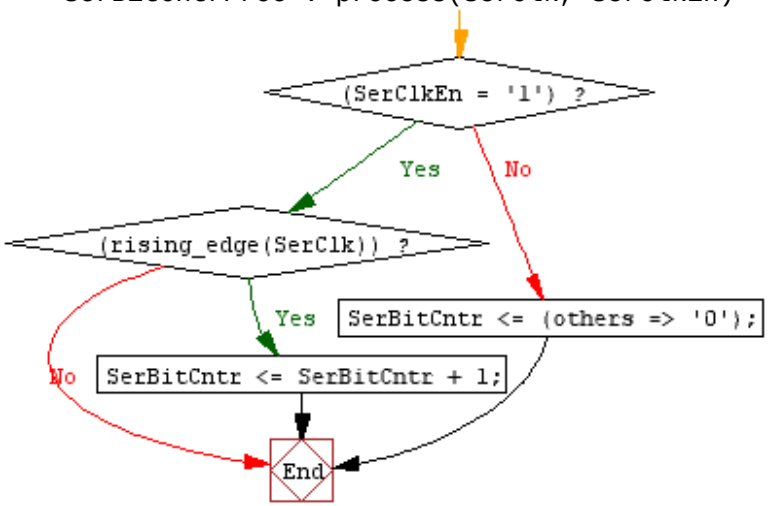
```
TempCtlProc : process(SYSCLK)
```



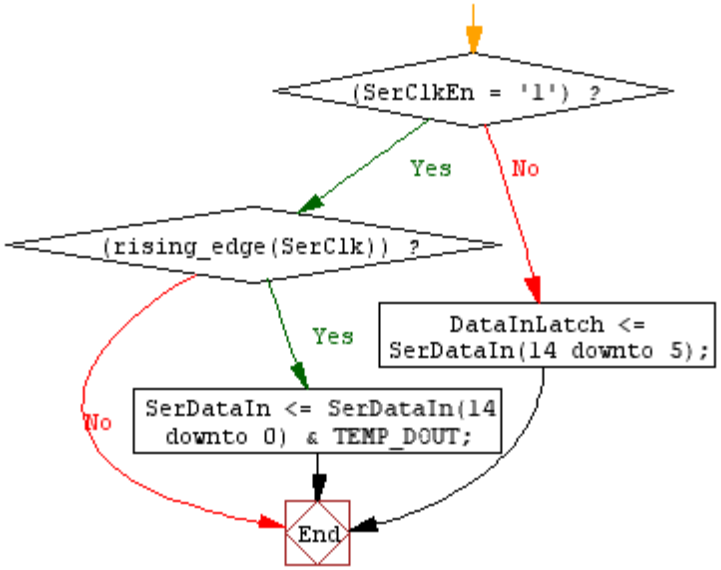
```
SerClkProc : process (SYSCLK)
```

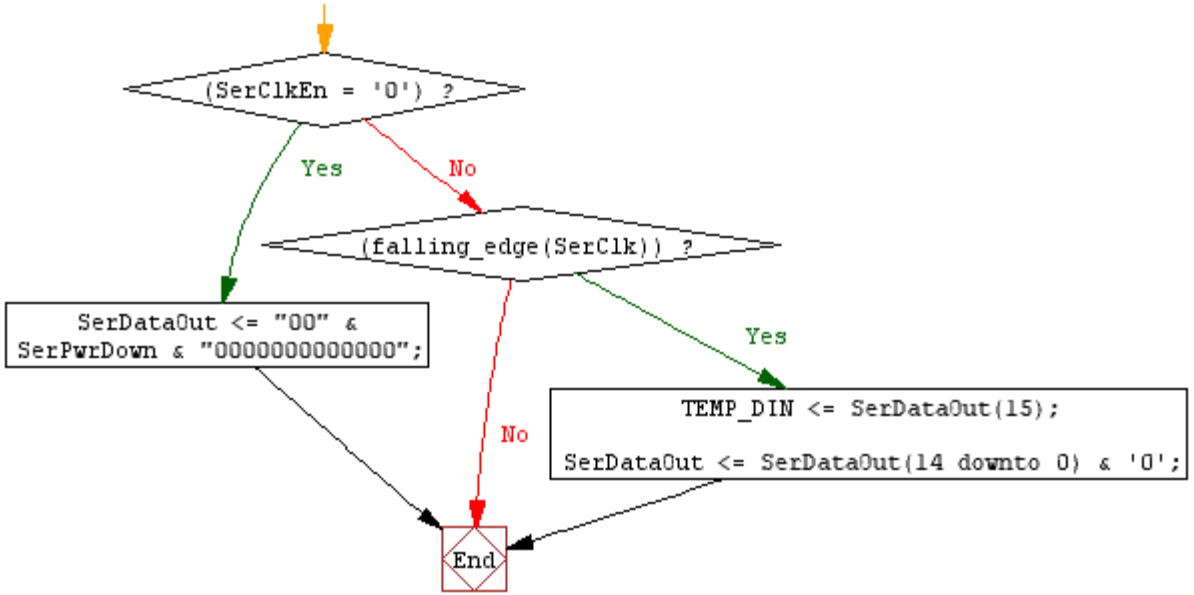



```
SerBitCntrProc : process(SerClk, SerClkEn)
```



```
SerReadProc : process(SerClk, SerClkEn)
```




```
SerWrtProc : process(SerClk, SerClkEn, SerPwrDown)
```