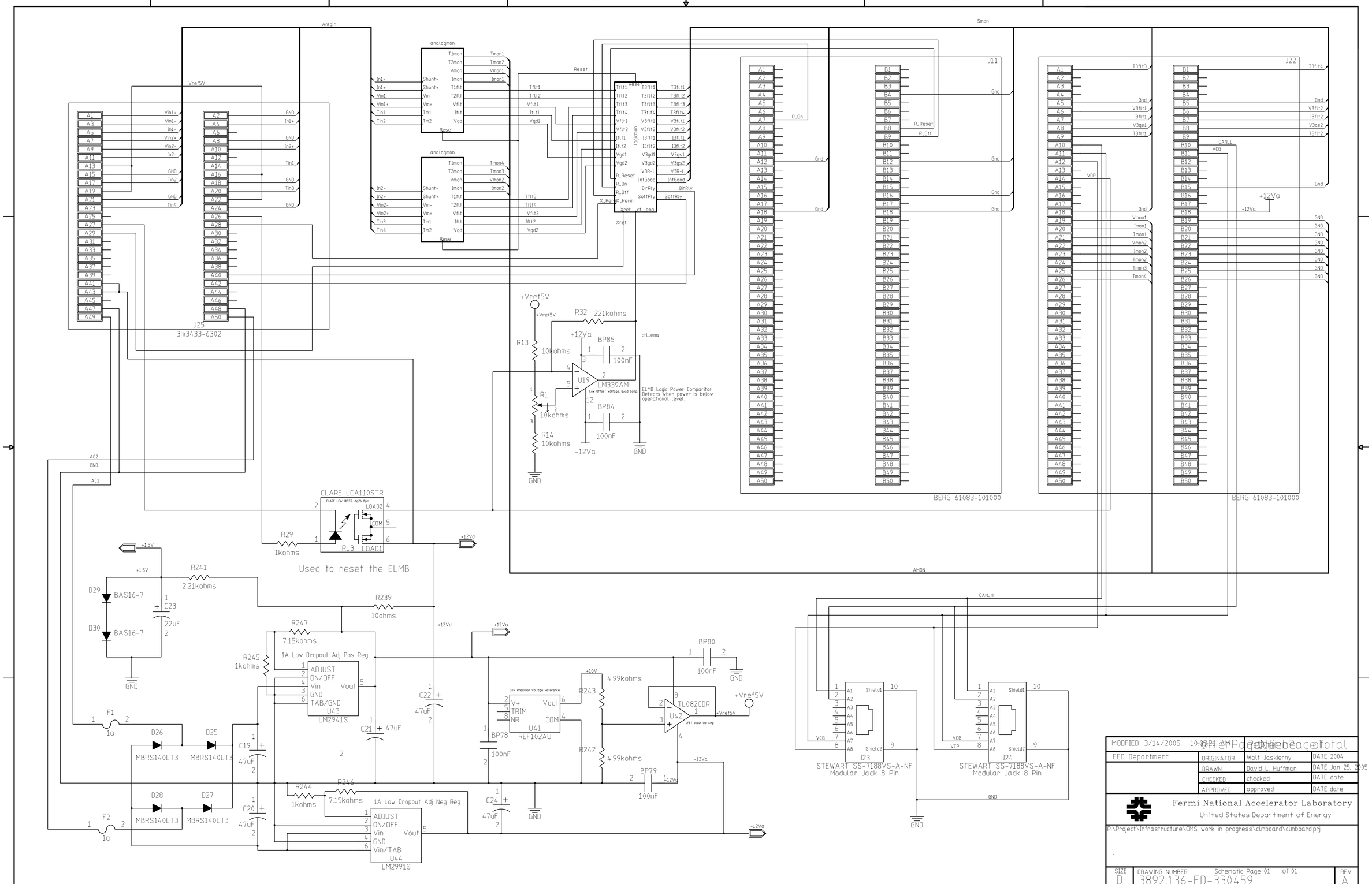

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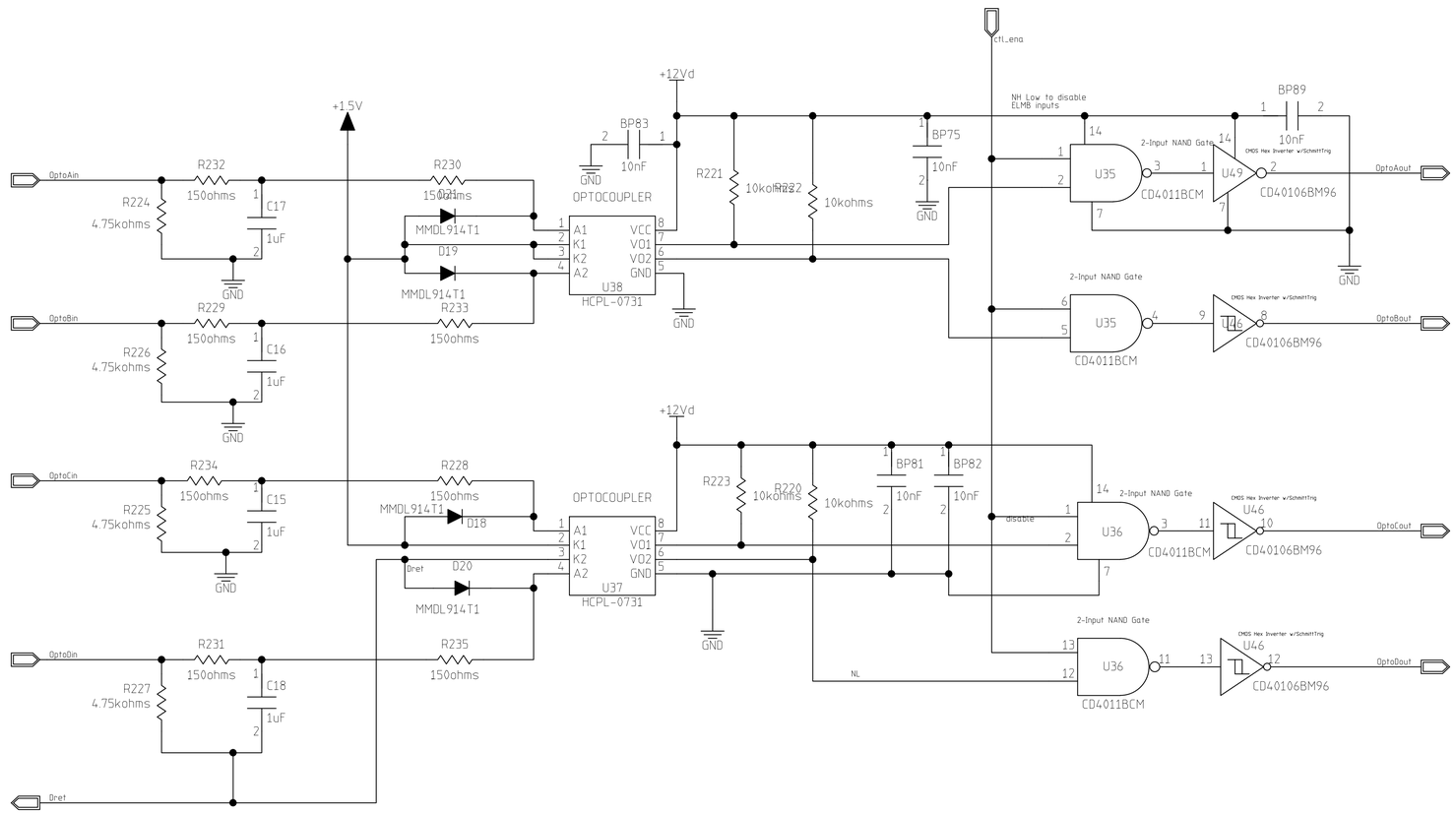

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	DRAWN	David L. Huffman	DATE Jan 25, 2005
	CHECKED	checked	DATE date
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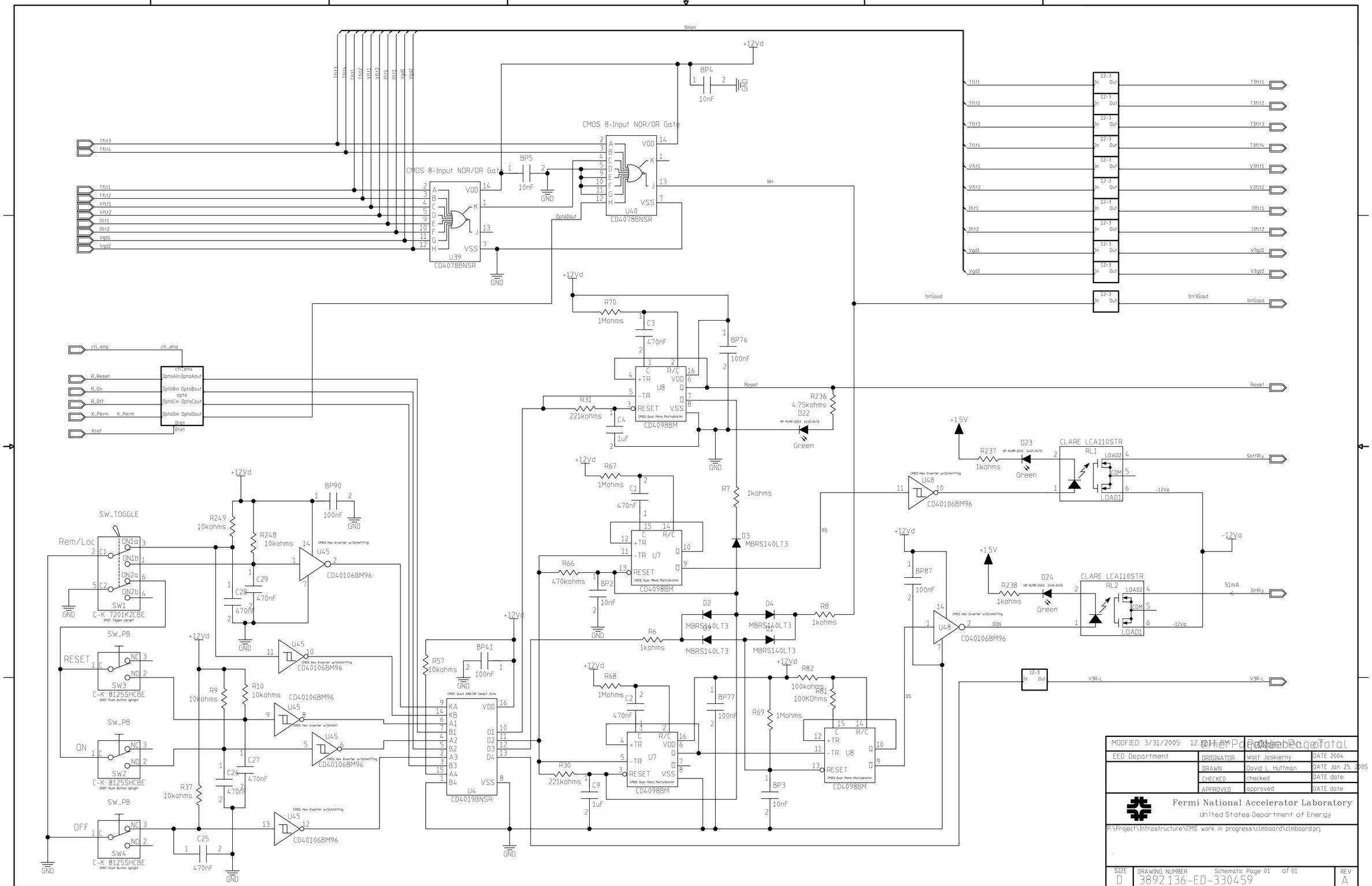
Dmon
+12Vd
BP4
10nF
GND
CMOS 8-Input NOR/OR Gate
U40
CD4078BNSR
U39
BP5
10nF
NH
OptoDout
Tflt3
Tflt4
Tflt1
Tflt2
Vflt1
Vflt2
Iflt1
Iflt2
Vgd1
Vgd2
T3flt1
T3flt2
T3flt3
T3flt4
V3flt1
V3flt2
I3flt1
I3flt2
V3gd1
V3gd2
IntGood
Int3Good
R70
1Mohms
C3
470nF
BP76
100nF
Reset
R236
4.75kohms
D22
Green
R31
221kohms
C4
1uF
CD4098BM
U8
R67
1Mohms
C1
470nF
U7
R7
1kohms
D3
MBRS140LT3
R66
470kohms
BP2
10nF
R6
1kohms
D2
D4
R8
1kohms
MBRS140LT3
R68
1Mohms
C2
470nF
R30
221kohms
C9
1uF
BP77
100nF
R82
100kohms
R81
100KOhms
R69
1Mohms
BP3
10nF
U48
CD40106BM96
R237
1kohms
D23
CLARE LCA110STR
RL1
LOAD2
COM
LOAD1
SoftRly
-12Va
R238
1kohms
D24
RL2
51mA
DirRly
BP87
100nF
DON
V3R-L
ctl_ena
R_Reset
R_On
R_Off
X_Perm
Xret
OptoAin OptoAout
OptoBin OptoBout
OptoCin OptoCout
OptoDin OptoDout
Dret
SW_TOGGLE
Rem/Loc
SW1
C-K 7201K2CBE
DPDT Toggle Upright
R249
10kohms
R248
10kohms
BP90
100nF
U45
CD40106BM96
C29
470nF
C28
470nF
SW_PB
RESET
SW3
C-K 8125SHCBE
SPDT Push Button Upright
R9
10kohms
R10
10kohms
ON
SW2
C27
470nF
C26
470nF
R37
10kohms
OFF
SW4
C25
470nF
R57
10kohms
BP41
100nF
CMOS Quad AND/OR Select Gate
U4
CD4019BNSR
+1.5V
MODIFIED 3/31/2005
EED Department
ORIGINATOR Walt Jaskierny
DRAWN David L. Huffman
CHECKED checked
APPROVED approved
DATE 2004
DATE Jan 25, 2005
DATE date
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Schematic Page 01 of 01
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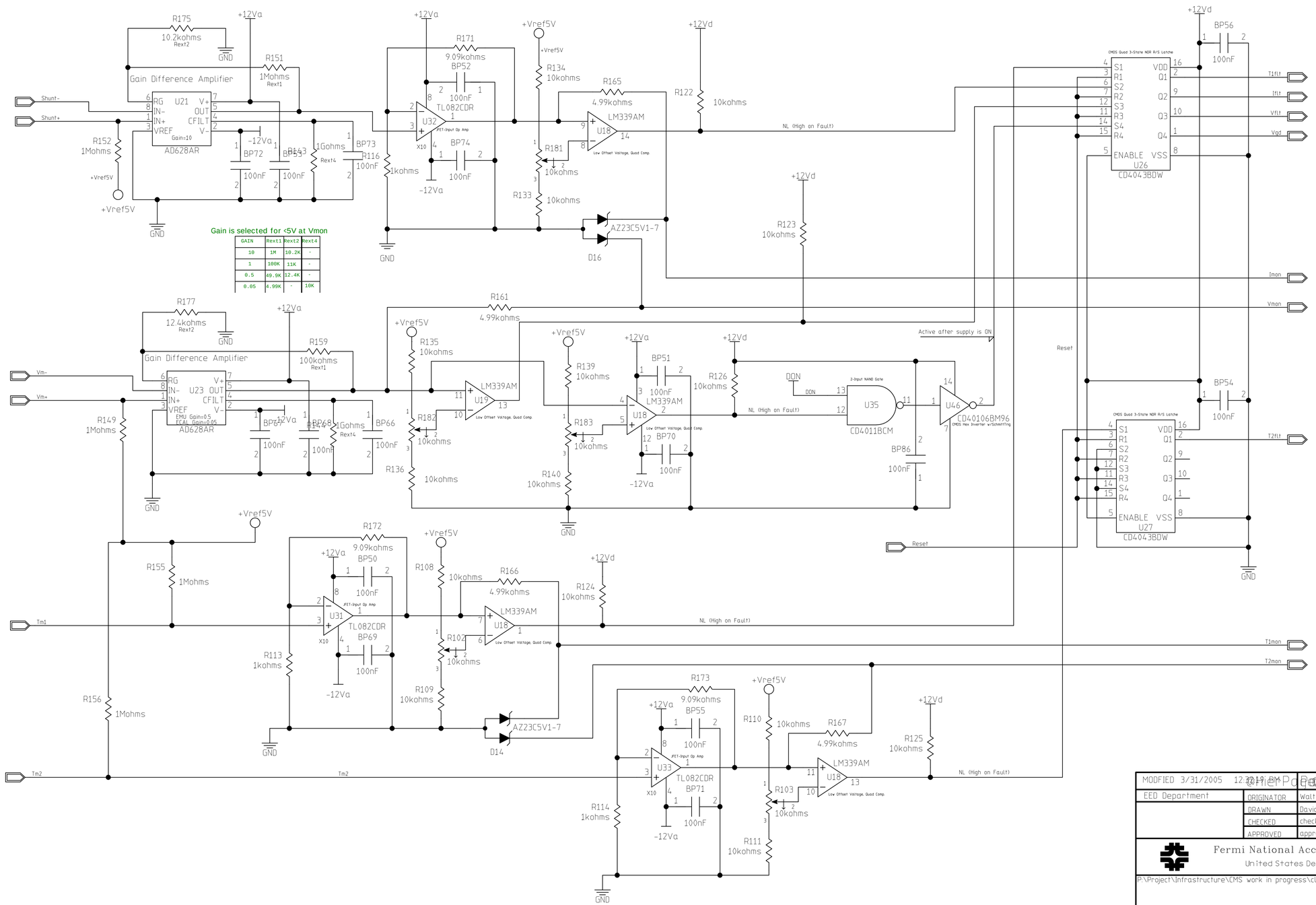

Gain is selected for <5V at Vmon

GAIN	Rext1	Rext2	Rext4
10	1M	10.2K	-
1	100K	11K	-
0.5	49.9K	12.4K	-
0.05	4.99K	-	10K

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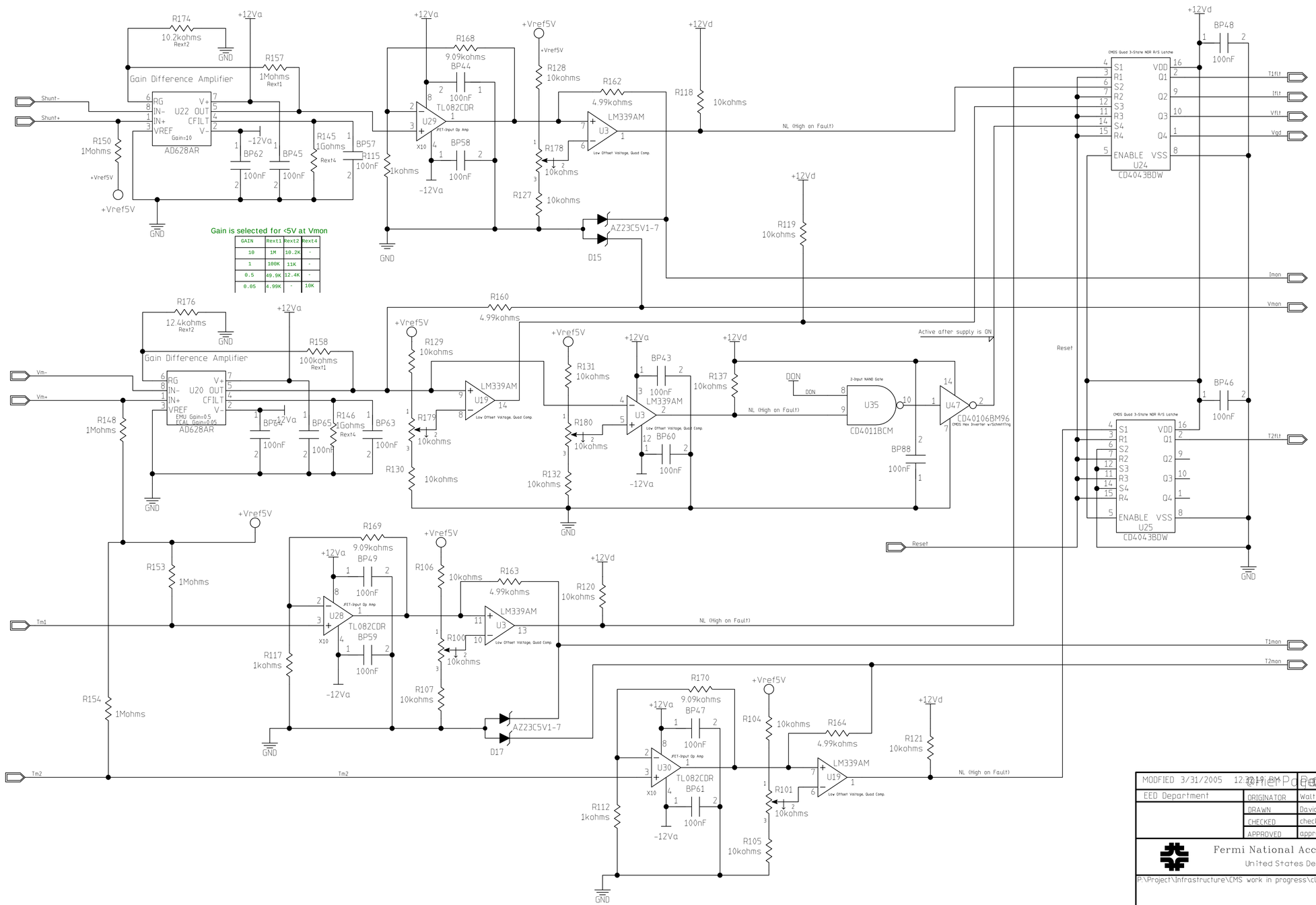

Gain is selected for <5V at Vmon

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0.05	4.99K	-	10K

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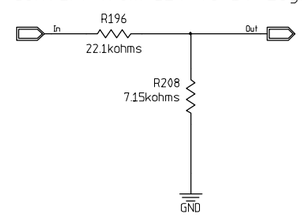
Convert from 12V to 3V Logic



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