# BRM Interlock Logic Proposal System Testing

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# Interlock Logic-Design Constraints

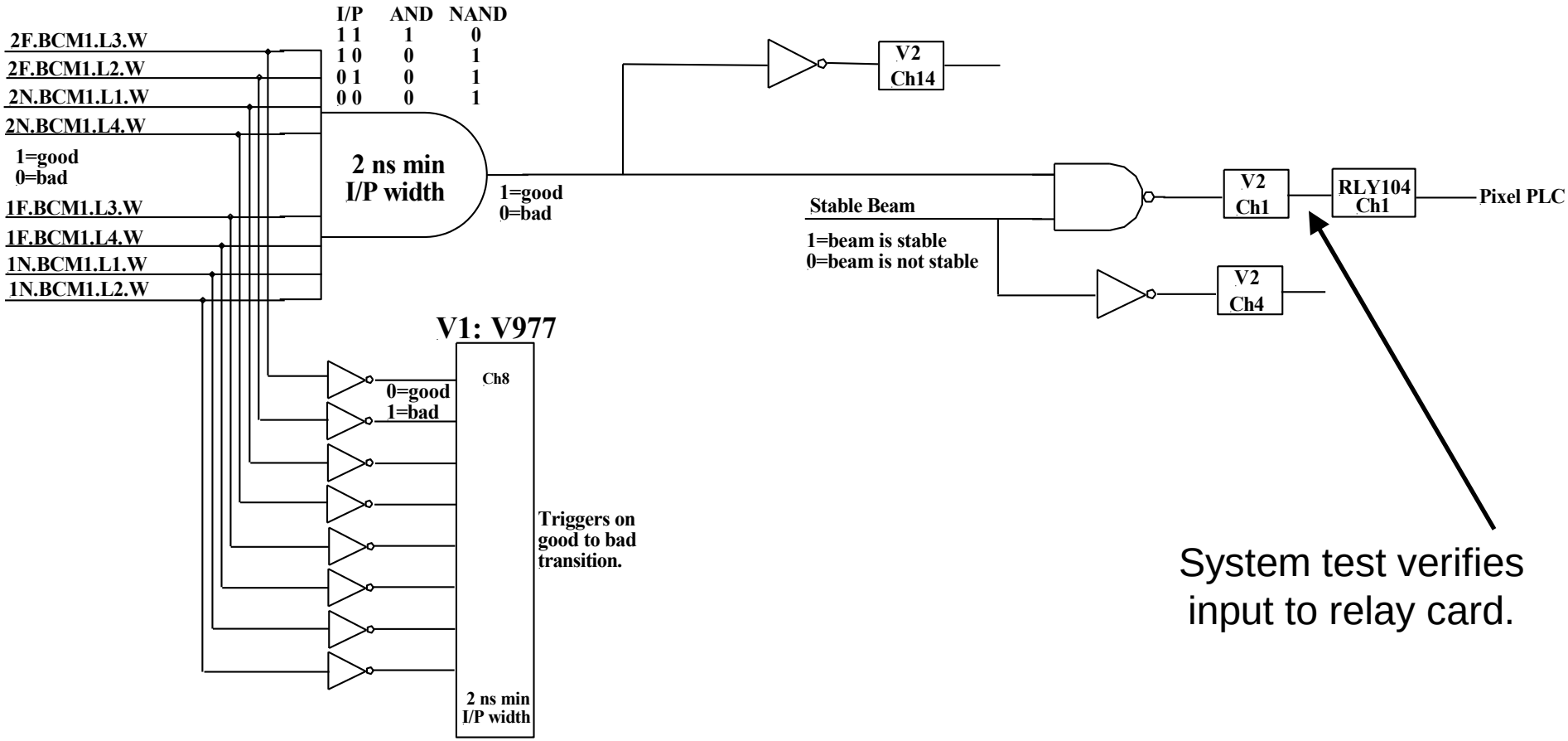
Input and Output signals must be fail-safe logic.

- 0=bad, 1=good

Inter-crate connections do not have to be fail-safe logic.

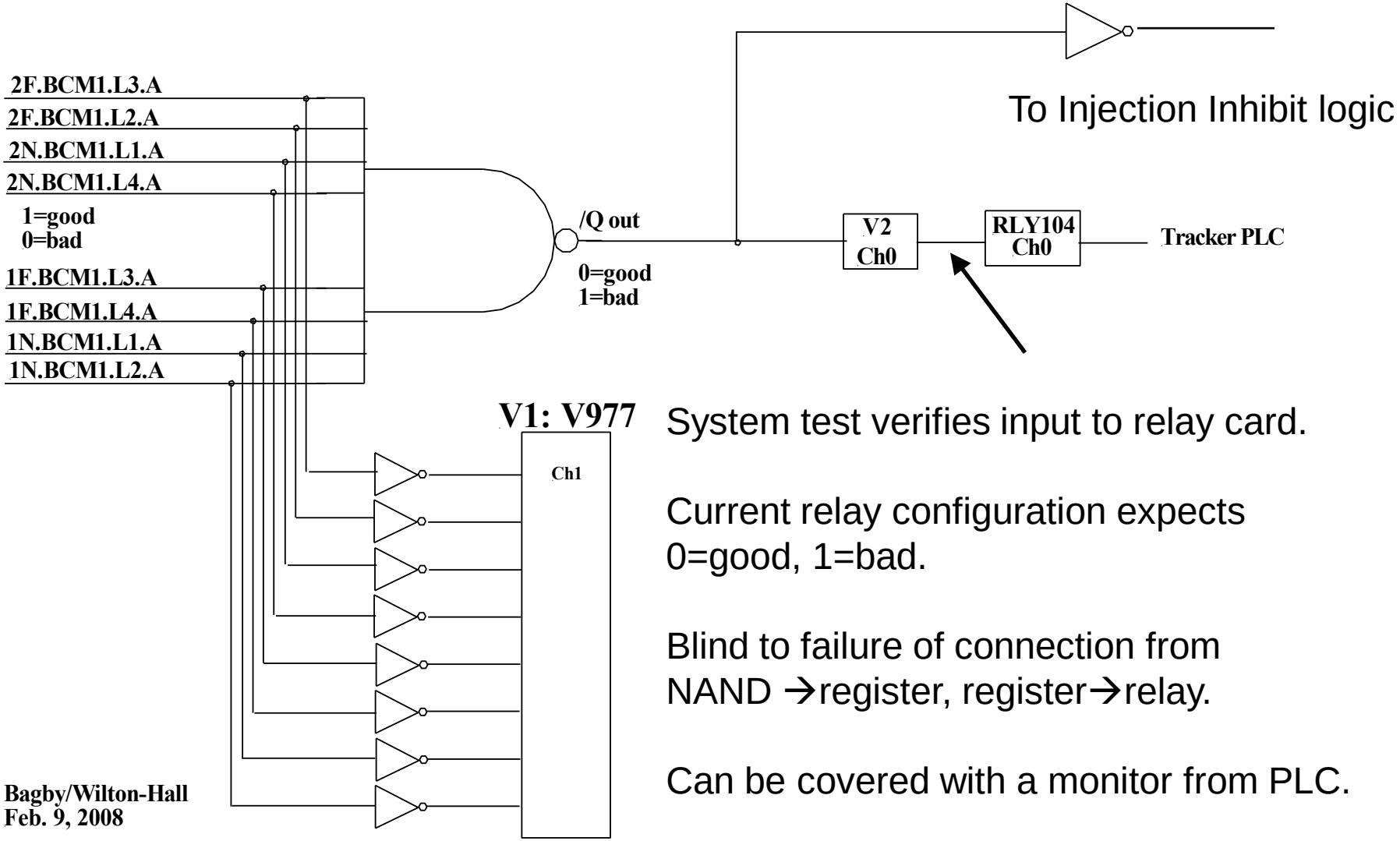
- Latched status of crate output more important than inter-crate fail-safe logic.
- Between run testing matrix insures inter-crate connections.

# Pixel PLC Logic




System test verifies input to relay card.

# Tracker PLC Logic



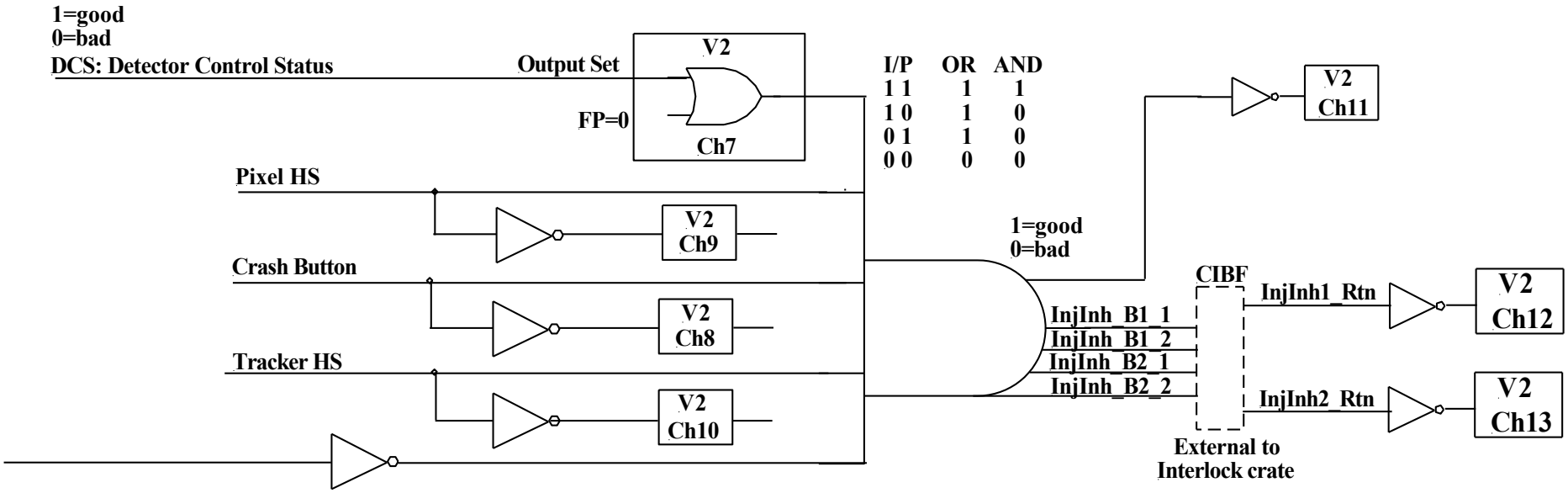

System test verifies input to relay card.

Current relay configuration expects 0=good, 1=bad.

Blind to failure of connection from NAND →register, register→relay.

Can be covered with a monitor from PLC.

# Injection Inhibit




Output of
Alarm NAND
0=good
1=bad

- DCS software input uses channel output set.
- Front Panel input should be terminated or FF output masked.
- InjInh_Rtn signal must be inverted for latching.
- Alarm input to Inj Inh NAND must be inverted.

# SF, DevMv, and PostMortem

Safe Beam 1 — V2 Ch2

1=Low Intesity
0=High Intesity

Safe Beam 2 — V2 Ch3

FF triggers on high to low intensity transition.

1=Devices not moving
0=Devices moving

Device Movement — V2 Ch5

FF triggers on moving to not-moving transition.

1=Postmortem state
0=no Postmortem

PostMortem — V2 Ch6

FF triggers on no Postmortem to Postmortem transition.

# System Test Issues

## Warnings and Alarms

- Registers can be tested either with a toggle from DAB64 (better) or by using the register input set feature.

## Pixel PLC

- Need to determine how to disable Stable Beam to see effect of Warning. Is it possible to get a toggle from the source?
- Register looks at input to Pixel relay.

## Tracker PLC

- Register looks at input to Tracker relay.

## Injection Inhibit

- Inclusive system test requires toggle from Pixel HS, CrashButton, and Tracker HS.
- DCS can be tested using output set.
- Output of CIBF (InjInh_Rtn) available for monitoring.

## Flag Monitors

- Safe Beam 1,2, Device Movement, PostMortem can either be tested with source toggle or input set.

# Register Test

## Establish communications with register modules.

- Read Serial Number, Firmware version, Dummy 16 register.
- Configure registers in ‘Test Mode’.
- Confirm all registers are clear.

## Test module functions.

- Input Mask, Output Mask, Input Set, Single Hit Read, Output Set

  Accomplished with x5555, xAAAA, and walking 1’s pattern.

# Communications Testing Sequence

V977: Register Test

| | | | 8 | 4 | 2 | 1 | 8 | 4 | 2 | 1 | 8 | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | x24 | Read SERIAL NUMBER of card | | | | | | | | | | | | | | | | |
| 2 | x26 | Read FIRMWARE REVISION | | | | | | | | | | | | | | | | |
| 3 | x2A | Read DUMMY 16 (x5555) | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 4 | x2E | SOFTWARE RESET (dummy write generates single shot reset) | | | | | | | | | | | | | | | | |
| | | Writes to the Control register (x28) default values | | | | | | | | | | | | | x | 0 | 1 | 0 |
| | | D0 Pattern Bit: 0=I/O register mode (Single-Hit) | | | | | | | | | | | | | | | | |
| | | D1 Gate Mask: 1=FP gate disabled (disables all FP inputs) | | | | | | | | | | | | | | | | |
| | | D2 OR/NOR Output: 0=enabled | | | | | | | | | | | | | | | | |
| 5 | x28 | Read CONTROL register (confirm mode) | | | | | | | | | | | | | x | 0 | 1 | 0 |
| 6 | x16 | SINGLEHIT READ-CLEAR (read clears all Qs) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | x00 | INPUT SET read (default state) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | If SUM>0, write INPUT SET 0000 | | | | | | | | | | | | | | | | |
| | | Read INPUT SET to confirm | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | x06 | SINGLEHIT READ (reads output) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

# System Test/Physics Mode

System test verifies logic gate connections are intact.

- Toggle Alarms and Warnings.
  - Monitor corresponding channels, PLC signals, and InjInh registers.
  - X5555, xAAAA, walking 1's test patterns.
- Toggle external inputs (DCS, Pixel/Tracker HS, CrashButton)

Configure registers in 'Physics Mode'.

- Enable Gate input.
- Set Single-Hit Mode.
- Mask unused registers.

# System Test

1 InjInh check

V2 SINGLEHIT READ x06 (0=good, no inhibit=$0000)

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

AFTER EACH TEST VARIABLE SINGLEHIT READ-CLEAR V2 to see InjInh change state

2 Walking 1's

V1 Chs 0-7 (ex. D4=tested Alarm channel)

V2 Ch 0,11,12,13 V1 chs 0-7 = Alarms

V1 Chs 8-15 (ex. D10=tested Warning channel)

Ch 1,14 V1 chs 8-15=Warnings

| | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | V1 readout | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Alarm trip | V2 readout | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | V1 readout | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Warn trip | V2 readout | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

V2 All other input testing

toggle 2-10 from source

monitor 2 for 2 11,12,13 for 7,8,9,10

3 for 3

1,4 for 4

5 for 5

6 for 6

3 $5555

V1 Even Chs

V2 Ch 0,11,12,13 for even V1 chs 0-7

Ch 1,4,14 for even V1 chs 8-15

4 $AAAA

V1 Odd Chs

V2 Ch 0,11,12,13 for odd V1 chs 0-7

Ch 1,4,14 for odd V1 chs 8-15

**Table 4.1: Address Map for the Mod. V977**

| ADDRESS | REGISTER/CONTENT | ADDR | DATA | R/W |
|---|---|---|---|---|
| Base + %0000 | INPUT SET | A24/A32 | D16 | read/write |
| Base + %0002 | INPUT MASK | A24/A32 | D16 | read/write |
| Base + %0004 | INPUT READ | A24/A32 | D16 | read only |
| Base + %0006 | SINGLEHIT READ | A24/A32 | D16 | read only |
| Base + %0008 | MULTIHIT READ | A24/A32 | D16 | read only |
| Base + %000A | OUTPUT SET | A24/A32 | D16 | read/write |
| Base + %000C | OUTPUT MASK | A24/A32 | D16 | read/write |
| Base + %000E | INTERRUPT MASK | A24/A32 | D16 | read/write |
| Base + %0010 | CLEAR OUTPUT | A24/A32 | D16 | write only |
| Base + %0012 | RESERVED | - | - | - |
| Base + %0014 | RESERVED | - | - | - |
| Base + %0016 | SINGLEHIT READ-CLEAR | A24/A32 | D16 | read only |
| Base + %0018 | MULTIHIT READ-CLEAR | A24/A32 | D16 | read only |
| Base + %001A | TEST CONTROL REGISTER | A24/A32 | D16 | read/write |
| Base + %001C | RESERVED | - | - | - |
| Base + %001E | RESERVED | - | - | - |
| Base + %0020 | INTERRUPT LEVEL | A24/A32 | D16 | read/write |
| Base + %0022 | INTERRUPT VECTOR | A24/A32 | D16 | read/write |
| Base + %0024 | SERIAL NUMBER | A24/A32 | D16 | read only |
| Base + %0026 | FIRMWARE REVISION | A24/A32 | D16 | read only |
| Base + %0028 | CONTROL REGISTER | A24/A32 | D16 | read/write |
| Base + %002A | DUMMY REGISTER | A24/A32 | D16 | read/write |
| Base + %002C | RESERVED | - | - | - |
| Base + %002E | SOFTWARE RESET | A24/A32 | D16 | write only |

# Documentation

Interlock documentation has been added to the web link

http://www-ppd.fnal.gov/EEDOffice-w/Projects/CMS/Silicon_TRacker/index.html

Item 2: Safety Interlock System Links

- Electronics manuals for V976 and V977
- Electronics schematic of logic.
- System test details.
- Text explaining test procedures.