Electronics Assemblies Checklist

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4/9/03 revised 06/28/12

1. System Design Elements

X/NA	List#	Checklist Function
	1.	Mating connectors on different assemblies checked for same pin-out
	2.	Cabling scheme insures that no return currents will flow back to remote sources through earth ground.
	3.	No signal cable is used to carry power to a remote device (remember the Wide Band fire..) without full and complete justification and paper trail
	4.	Maximal total power Dissipation of crate-full of boards calculated against cooling system capabilities; cooling system insures that, on average, no board runs hotter than 35˚C
	5.	Airflow of cooling system checked against area mechanics and local smoke detection systems to insure no blockage or restrictions.

2. Schematics – General Rules of Drafting

X/NA	List#	Checklist Function
	1.	All sheets same size (all B or all D)
	2.	All sheets have assigned drawing number on them
	3.	All sheets have drafter's name
	4.	All sheets have signed and dated check-off by designer
	5.	ANSI rules for title block, grid, etc. followed on all sheets
	6.	Design is fully hierarchical; no page to page connectors, no duplicate reference to same page
	7.	All components have unique visible reference designators and visible component values
	8.	All components have assigned PCB footprints
	9.	Schematic symbols are not re-used for different parts
	10.	All devices have visible and connected power and ground pins
	11.	All Schematic pages have top-to-bottom, left-to-right flow
	12.	Connectivity between signals is by wires and busses, not by signal names
	13.	Connection dots are evident and used
	14.	Power nets (e.g. VCC, VEE, GND) are global across entire design and not unique per sheet
	15.	Bill of materials included in review packet
	16.	Bill of Materials includes all mechanical, mounting and other non-electrical components in addition to all electrical components

3. Device Design Considerations

X/NA	List#	Checklist Function
	1.	all unused inputs terminated
	2.	race conditions checked
	3.	mating connectors on different assemblies checked for same pin-out
	4.	all outside world I/O lines filtered for RFI
	5.	all outside world I/O lines protected against static discharge
	6.	Analysis of filtering / bypass (bypass cap for each IC)
	7.	voltage ratings of components checked
	8.	each IC has predictable or controlled power-up state
	9.	minimum number of characters in values
	10.	character size for readability
	11.	schematics printed at a readable scale
	12.	special PCB or parts list information entered for each component, if required
	13.	polarized components checked (LEDs)
	14.	electrolytic and tantalum capacitors checked for no reverse voltage
	15.	ground made first and breaks last for hot plug ability
	16.	pull-ups on all open collector outputs
	17.	sufficient power rails for analog circuits
	18.	amplifiers checked for stability (capacitance load on op-amps)
	19.	oscillators checked for reliable startup
	20.	consider signal rate-of-rise and fall for noise radiation
	21.	check for input voltages applied with power off and CMOS latch up possibilities
	22.	reset circuit design reliable, both glitch-free and consistent; tested with slow power supply fall time
	23.	separate analog signals from noisy or digital signals
	24.	ability to disable watchdog timer for testing and diagnostics and emulation
	25.	sufficient capacitance on low dropout voltage regulators (Pdiss in regulator vs. package limits and ΔT rise
	26.	setup, hold, access times for data and address busses
	27.	check the data sheet fine print and app-notes for weird IC behaviors
	28.	Determine effect of losing each of multiple grounds on a connector. Connector pin rating does not presume any current to be carried by connector shells, screws or other non-pin contact
	29.	check maximum power dissipation at worst-case operating temperatures
	30.	check time delays and slew rates of op-amps used as comparators
	31.	check op-amp input over-drive response for unintended output inversion

	32.	check common mode input voltages on op-amps
	33.	check for voltage transients and high voltages on FET gates
	34.	check failure modes and effects of failed power semiconductors
	35.	Check jtag chain to insure proper wiring • ability to probe/break jtag chain to isolate failures of individual parts • filter capacitance provided on TMS, TCLK lines • Buffering of TMS. TCLK on boards so that external programmer never 'sees' more than a couple of loads • Provision to disable board-wide fast clocks during jtag to minimize programming errors
	36.	Power Supplies Fused
	37.	Speed of fuse response appropriate for load
	38.	Transient suppression on power supplies
	39.	Distribution of power supply capacitance across design- appropriate mix of C/L ratio, C values (C = [I * t] / (delta v)).
	40.	Correct speed grade/device family of all devices clearly marked
	41.	Check that at max fused load of all supplies, current through any pin of connector – including grounds – is less than fully derated pin current limit.
	42.	Physical distribution of pins in connection uses placement of grounds to advantage to shield sensitive signals from aggressor signals and from each other
	43.	Correct and proper isolation of analog ground from digital ground
	44.	System design provides one and only one point where analog ground, digital ground and earth ground tie to each other
	45.	Termination of differential signals provide return path for common-mode component of differential signal
	46.	Any connection between different logic families (e.g. CMOS driving TTL, TTL driving CMOS) insures sufficient drive current and voltage margin
	47.	Indicator LEDs are pulsed or sufficiently limited to insure minimal waste current
	48.	Fly-back diodes on relays and switched transformers
	49.	Pull-ups or pull-downs resistors on all unused inputs

4. Preferred Component Reference Designators

X/NA	Item#	Checklist Function
	1.	R - fixed resistor
	2.	RN - resistor network
	3.	RV-variable resistor
	4.	C - capacitor (network, fixed or variable)
	5.	L - inductor
	6.	Q - transistor, FET, SCR, TRIAC
	7.	D - diode, rectifier, zener, varicap, LED
	8.	DL - multi-segment display (any type)
	9.	VR, - voltage regulator
	10.	U, IC - integrated circuit
	11.	J - socket, jack (female)
	12.	P - plug (male)
	13.	JP - jumper (pins, trace, or wire)
	14.	X - crystal
	15.	M - modular subassembly, daughter board
	16.	S - mechanical switch
	17.	F - fuse
	18.	FL - filter
	19.	T - transformer
	20.	KB - keyboard
	21.	BT – battery
	22.	RC – resistor-capacitor network

5. Printed Circuit Board Design

X/NA	List #	Checklist Function
	1.	Hole diameters on drawing are finished sizes, after plating.
	2.	finished hole sizes are >=10 mils larger than lead
	3.	silkscreen legend text weight >=10 mils
	4.	pads >=10 mils larger than finished hole sizes
	5.	place thru-hole components on 50 mil grid
	6.	no silkscreen legend text over vias (if vias not solder masked) or holes
	7.	Soldermask does or does not cover vias (consistency tented or not)
	8.	all legend text reads in one or two directions
	9.	components labeled left-right, top-bottom
	10.	company logo in silkscreen legend or in the foil
	11.	Silkscreen lettering spaced away from contact areas, minimum 50 mil.
	12.	copyright notice on PCB
	13.	date code on PCB
	14.	PCB part number should be present on the silkscreen layer.
	15.	assembly part number on PCB
	16.	all polarized components point same way
	17.	components >=0.2” from edge of PCB
	18.	ground planes where possible
	19.	test pad or test via on every critical net to allow in circuit test
	20.	mounting holes electrically isolated or not
	21.	mounting holes shall be relieved from all copper (planes and > traces) a minimum of twice the trace/space rule applied to all board > copper or 20% of the drill diameter, whichever is larger
	22.	proper mounting hole clearance for hardware
	23.	all polarized components checked
	24.	no acute inside angles in foil (90 or 45 deg only)
	25.	Traces and Planes >= 20 mils from edge of PCB
	26.	PCB revision on silkscreen legend
	27.	assembly revision blank on silkscreen legend
	28.	serial number blank on silkscreen legend a filled rectangle provided for writing with a marker. (depending on how long the serial #’s will be and about 0.25” high.)
	29.	Soldermask swell checked, should not be too close to copper areas
	30.	thru hole drill tolerance noted
	31.	thru hole Soldermask tolerance noted
	32.	thru hole route tolerance noted
	33.	thru hole silkscreen legend tolerance noted

	34.	drill legend shows all symbols and sizes
	35.	mounting holes matched 1:1 with mating parts (get a part and check it)
	36.	automated netlist check
	37.	manual netlist check (compare to IPC356 netlist)
	38.	CAD design rule check
	39.	drill origin is a tooling hole
	40.	Check aspect ratio (board thickness to hole size) should be <= 10:1
	41.	NC drill and photo plot file language format noted
	42.	tools on drill plot and NC drill file cross checked
	43.	Soldermask over bare copper noted if needed (SMOBC)
	44.	PCB thickness, material, copper weight noted
	45.	trace and space geometry noted
	46.	printed drill report sent with check plots
	47.	Gerber 274-X files only, for build files
	48.	photo plot files checked in file viewer
	49.	test coupon on PCB containing minimum geometry features
	50.	Trace width sufficient for current carried Copper Foil Current capacity: 0.5oz/(sq/ft)--.67mil thick @ 5mil width -3.5amps 1.0oz/(sq/ft)--1.34mil thick @ 5mil width -7.0amps 2oz/(sq/ft)--2.68mil thick @ 5mil width - 28amps 3oz/(sq/ft)--4.02mil thick @ 5mil width - 42amps Copper ohm per foot calculation ((0.679*10-6)/(t-width*t-height)*length in inches)
	51.	minimum component body spacing (assembly drawing layer vs. actual part extents).
	52.	SMD pad shapes checked
	53.	Fiducials - visual references for automated assembly on the board and on components with high pin count and pitch < 20mil.
	54.	tooling holes for automated assembly
	55.	sufficient clearance for high voltage traces with FR4 10v/mil –external Layer 50-60v/mil – internal Layer 400v/mil layer to layer
	56.	Component and trace keep out areas observed
	57.	high frequency circuitry precautions observed
	58.	thermal relief's for internal power layers
	59.	solder paste mask openings are proper size
	60.	No blind or buried vias with justification and approval
	61.	PCB layout panelized correctly (typically supplied by vendor)
	62.	panelized PCB fits test and manufacturing equipment
	63.	sufficient clearance for socketed IC's

	64.	SMD component orientation arbitrary or consistent
	65.	insure pin 1 (different usually square) interpretation and orientation consistent among all connectors of a given type on the board
	66.	clearance for IC extraction tools
	67.	clearance for emulator adapter
	68.	clearance for sockets for ICs during proto phase
	69.	standoffs on power resistors
	70.	digital and analog signal commons joined at only one point.
	71.	EMI and RFI filtering as close as possible to exit and entry points in shielded areas
	72.	layout PCB so that any rework or repair of a component does not require removal of other components
	73.	Review component data sheets on all devices compare to manufacturers suggested layout

	74.	Must justify slots and scoring
	75.	Edge milling if necessary is on correct side of board
	76.	HASL finish only unless otherwise justified (BGA, COB, etc)
	77.	checking actual symbols in schematic against pin-out of device to make sure they match
	78.	Sufficient mechanical clearance between parts that have mechanical protuberance (e.g. regulators that fold down, with or without heat sinks).
	79.	Checking that BOM calls out right package relative to layout footprint (e.g. don't put a .150" SOIC on the board and order .300" parts)
	80	insure that the layout footprint has an assembly or silkscreen as big as the part will take up.
	81	Sufficient mechanical clearance between parts for pick-n-place

6. PCB Assemblies

X/NA	List#	Checklist Function
	1.	miscellaneous parts on bill of materials and assembly notes for same: hardware, heat sinks, heat sink compound or composite insulators, IC sockets, consumables
	2.	assembly notes for all special operations
	3.	conformal coating should be noted
	4.	special static handling precautions required during assembly and test
	5.	BOM and packing list parts must agree with parts delivered

7. Wired Assemblies

X/NA	List#	Checklist Function
	1.	wire gauge checked for compatibility with each termination
	2.	cable ties or lacing cord shown where needed
	3.	length & color of each wire indicated
	4.	Overall shield should be tied at one end or both to ground
	5.	notes about application of wire terminations (technique, heat shrink tubing, amount of solder, crimp force, tools, etc.)

8. Parts List

X/NA	List#	Checklist Function
	1.	each component has quantity, reference designator and description
	2.	list qualified part numbers for special devices
	3.	suggested and alternate manufacturer(s) listed
	4.	object/binary code and method/programmer specified for each programmable device
	5.	Delivery schedule of parts consistent with board delivery
	6.	price and availability checked for each component

9. Testability

X/NA	List#	Checklist Function
	1.	test points on PCBs for critical circuits
	2.	test pads for in-circuit or bed-of-nails functional testing
	3.	test pads on a regular grid
	4.	test procedure written for each test phase
	5.	Software written prior to proto delivery
	6.	special test arrangements and connectors for testing

10. Maintainability

X/NA	List#	Checklist Function
	1.	easy disassembly and reassembly
	2.	fuses accessible and labeled
	3.	self test mode
	4.	spare parts available
	5.	status LEDs on PCB
	6.	event logging of exceptional conditions

	7.	vibration tolerance of entire assembly and individual modules
	8.	surge current magnitude through semiconductors within rating
	9.	thermal cycling excursions internal to components and assemblies within acceptable limits
	10.	capacitors mounted below or away from heat-dissipating devices such as transformers
	11.	resistance and tolerance of entire product to static discharge via any path

11. Mechanical Drawings

X/NA	Item#	Checklist Function
	1.	standard title block and border used
	2.	no dimensions on the material
	3.	every feature must have X and Y dimension, along with radius, diameter, etc.
	4.	every hole must be checked for alignment with mating hole(s) in other parts
	5.	check every hole diameter
	6.	tolerance for sheet metal feature position noted
	7.	tolerance for sheet metal hole size noted
	8.	specify material
	9.	specify finish
	10.	specify units
	11.	specify debur or brush
	12.	details for special operations
	13.	file name on each sheet
	14.	CAD layers shown on drawing
	15.	all hardware specified and listed on parts list
	16.	screw lengths checked; extra thread required for fasteners (nut, lock washer, washer)
	17.	hole diameters checked for each screw
	18.	tapped hole thread details indicated

11. Safety

X/NA	List#	Checklist Function
	1.	fuse and circuit breaker size and characteristics
	2.	fuse sizes marked near fuse holder
	3.	room to remove fuse without damaging other components
	4.	spare fuse storage
	5.	shock hazards
	6.	radiated energy warnings and shields
	7.	applicable standards checked
	8.	protection against liquids and foreign objects

12. Documentation

X/NA	List#	Checklist Function
	1.	end-user instructions: unpacking, how to use, warranty, service, troubleshooting
	2.	service manual: troubleshooting procedures, parts lists, help line info
	3.	design notes: why were significant design decisions made the way they were and other info that may be lost if designers depart the organization
	4.	PLD Firmware archive, Download files unique per position, database of load sets for different segments

Notes:
Checklist user should review all functions and check off all items as valid and checked (X) or as not applicable (NA).