Nevis MicroBooNE Readout

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Our Tasks

- Digitize and record TPC pulse height information: 8256 channels.
- Digitize and record PMT pulse height information: 30 pmt's.
- For both neutrino beam events and for potential Supernova events.

Environment

- TPC Full drift time: 1.6msec.
- To include ALL track information from random events that could give some ionization reaching wires within 1.6 msec of the t_0 of an event we save all samples within -1.6msec to +3.2 msec of the t_0 of the event: 4.8 msec.

- Digitize at 2 MHz

- Booster Neutrino Beam: **15Hz**.
- Beam neutrino event rate only: **1/600 secs.**
- **To avoid recording unnecessary “empty spill data” the photodetectors will provide a trigger for neutrino beam events.**

- **Supernova events are spread over ~ 20 secs and are low energy.**
- **Impossible to trigger on amidst radioactivity and cosmic rays background.**
- **Must rely on “external alert” from the supernova alert watch: ~ 1 hour.**
- **→ The last hour of SN data must be always available → Continuous data recording.**

Boundary conditions

Digitizing Boards: Full event Data volume.

- 16 bits/sample **x** 2 MHz **x** 4.8 ms **x** 8256 wires = **160 MB/event**

↓

Data reduction and Compression

- Neutrino Beam events: No data loss.

  Only lossless data reduction or compression allowed.

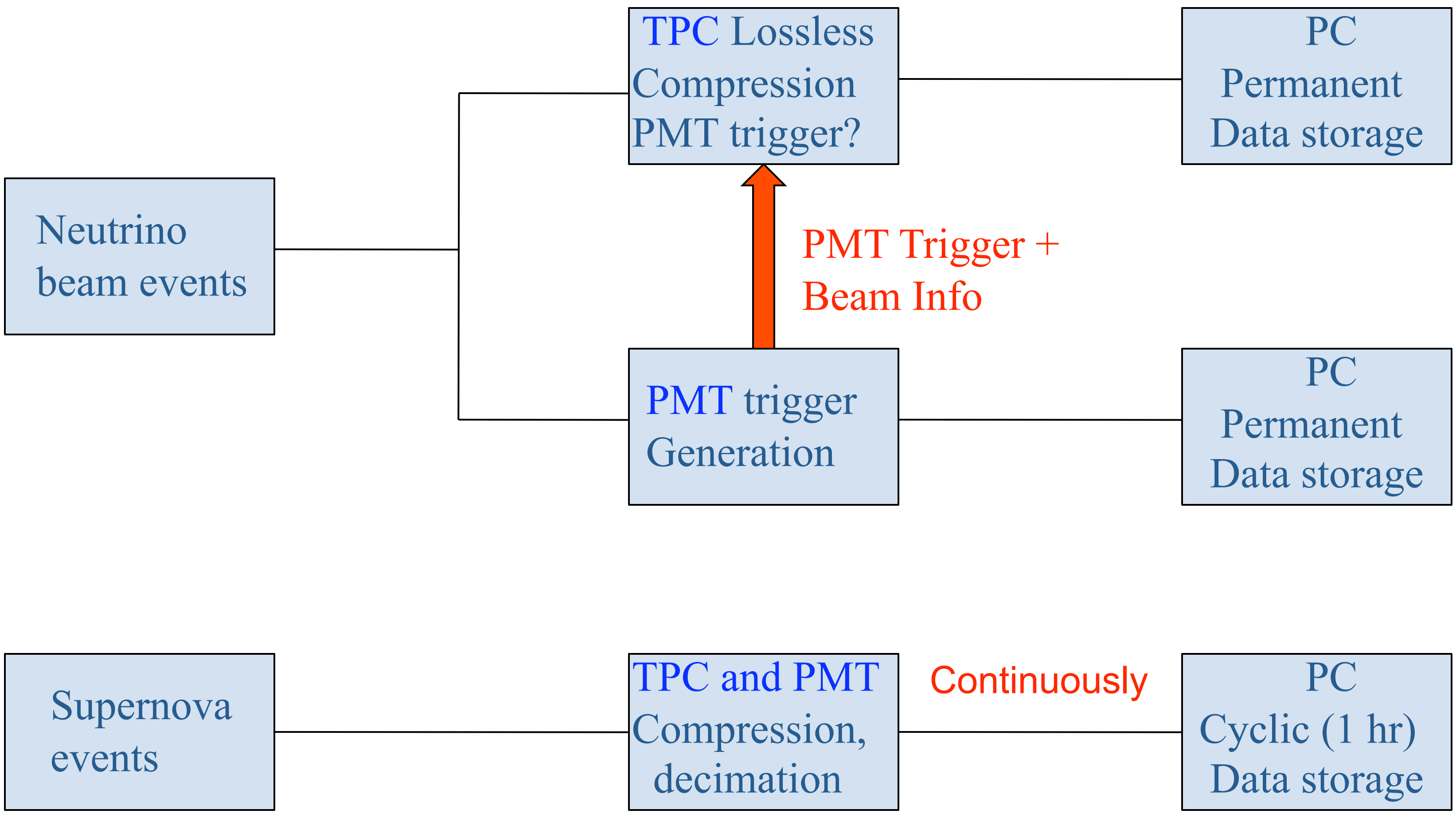
  Example: Huffman coding. Reduction: ~8-10.

- Supernova data: Some data loss allowed.

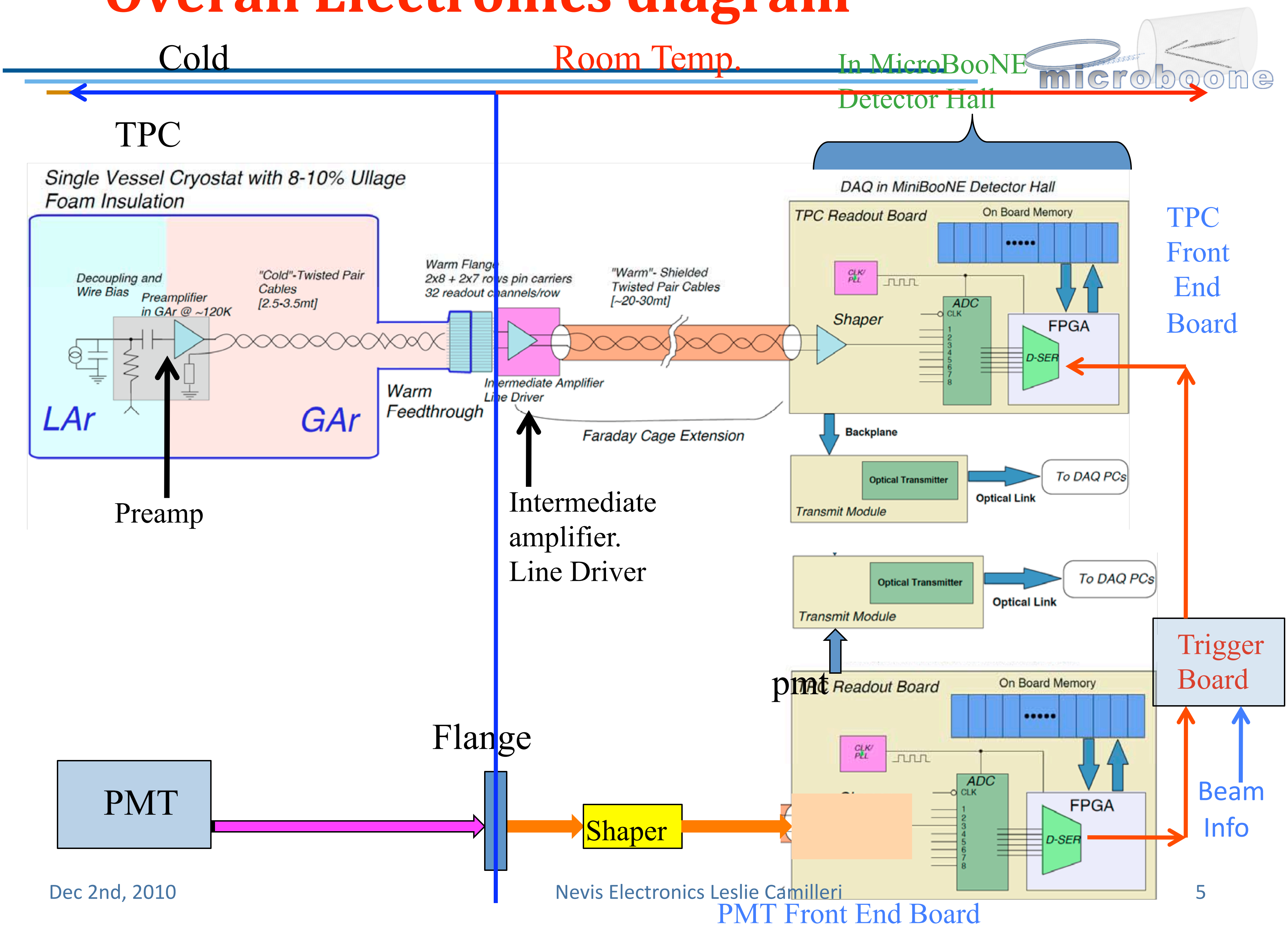
  Example:

  Decimation (Average of 10 samples) + Huffman coding → Reduction: ~80.

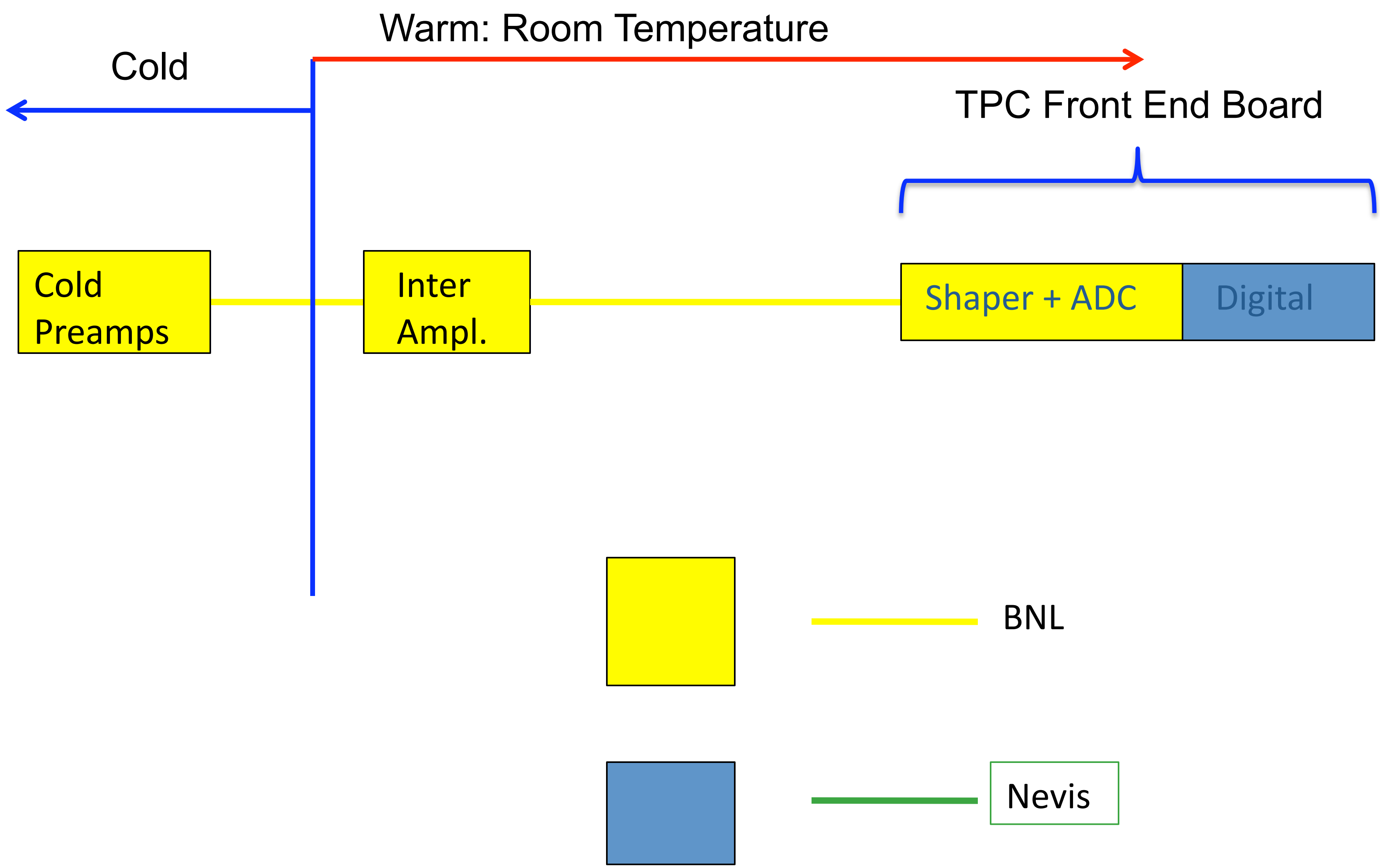
System Conceptual design



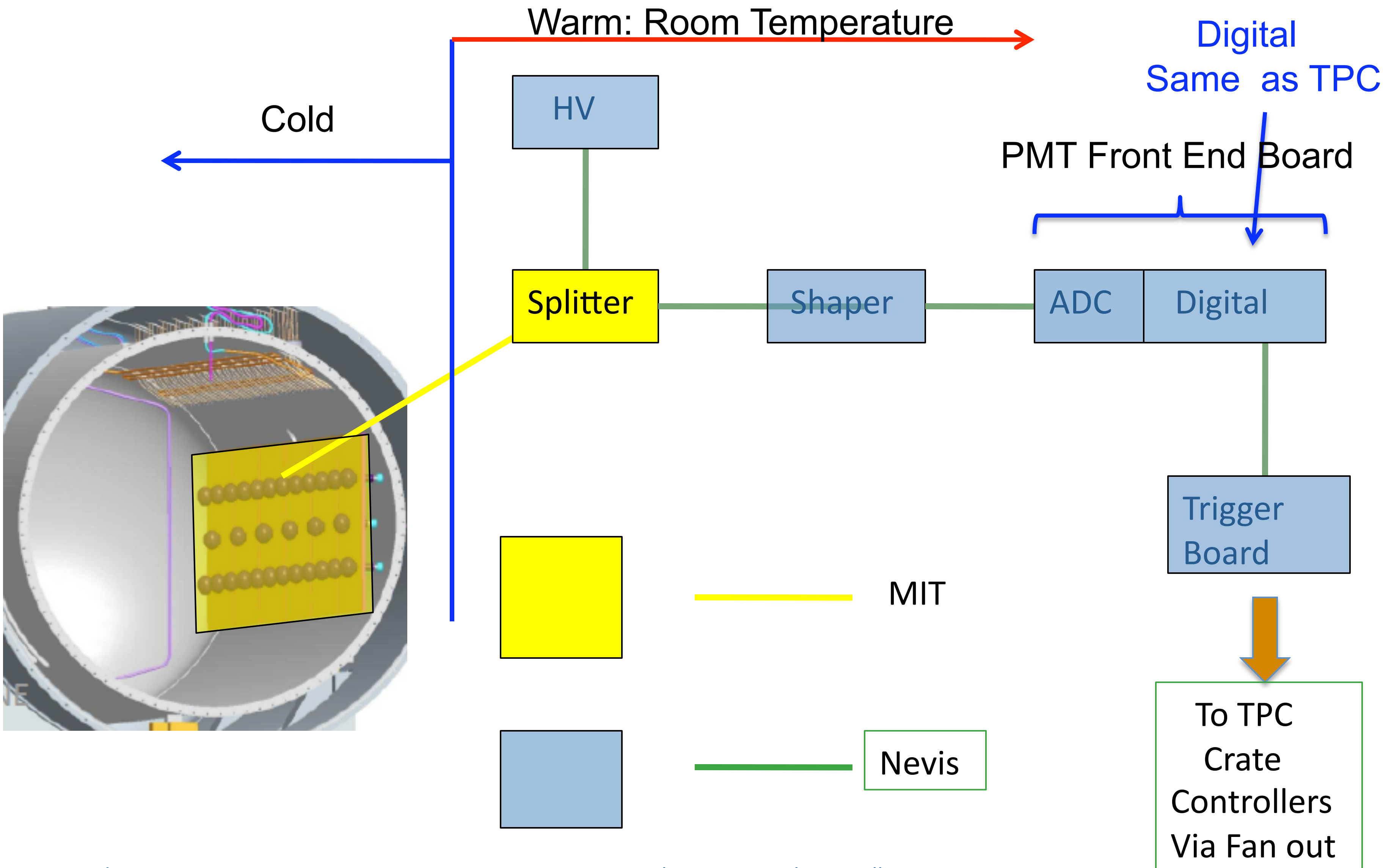
Overall Electronics diagram



TPC Readout Structure and Responsibilities



Photodetector Readout Structure and Responsibilities



TPC Digitization components .

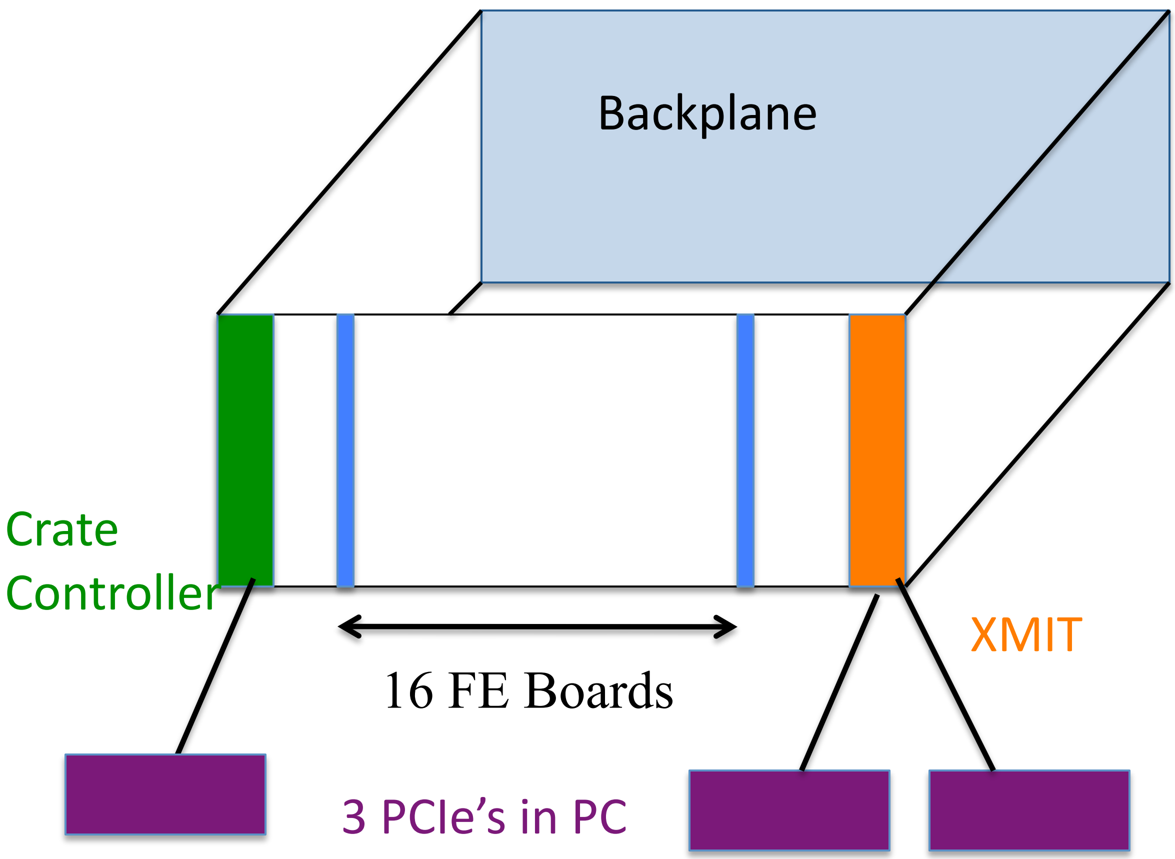
Split the TPC digitizing into 5 components

All boards are custom designed at Nevis

- Crate (16 FEB): mechanics and Backplane
- Front End Board
- Transmit (XMIT) Module
- Crate Controller
- 3 PCI express modules in PC.

One PC per crate

10 crates
(9 TPC + 1 PMT)

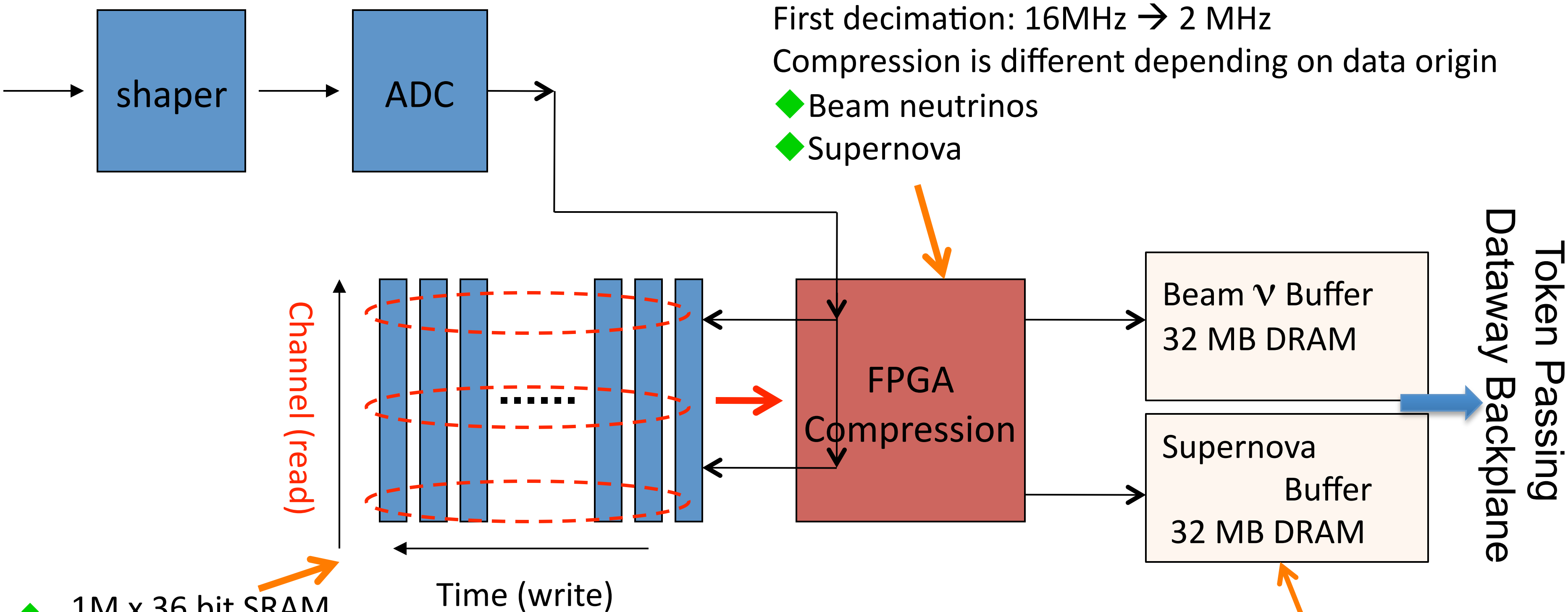


Each crate and PC
Cover ~1/9 of the detector
Along beam direction

Digitizing Boards: Hardware and Tasks

Continuous Data rate per card: 64 wires x 2 MHz = 128 MHz 12 bit ADC words.

STRATIX III FPGA
First decimation: 16MHz → 2 MHz
Compression is different depending on data origin
- Beam neutrinos
- Supernova



- 1M x 36 bit SRAM
- Speed 128 MHz
- **Data is recorded in Time order**
- **2 ADC/36 bit word → 64 MHz**

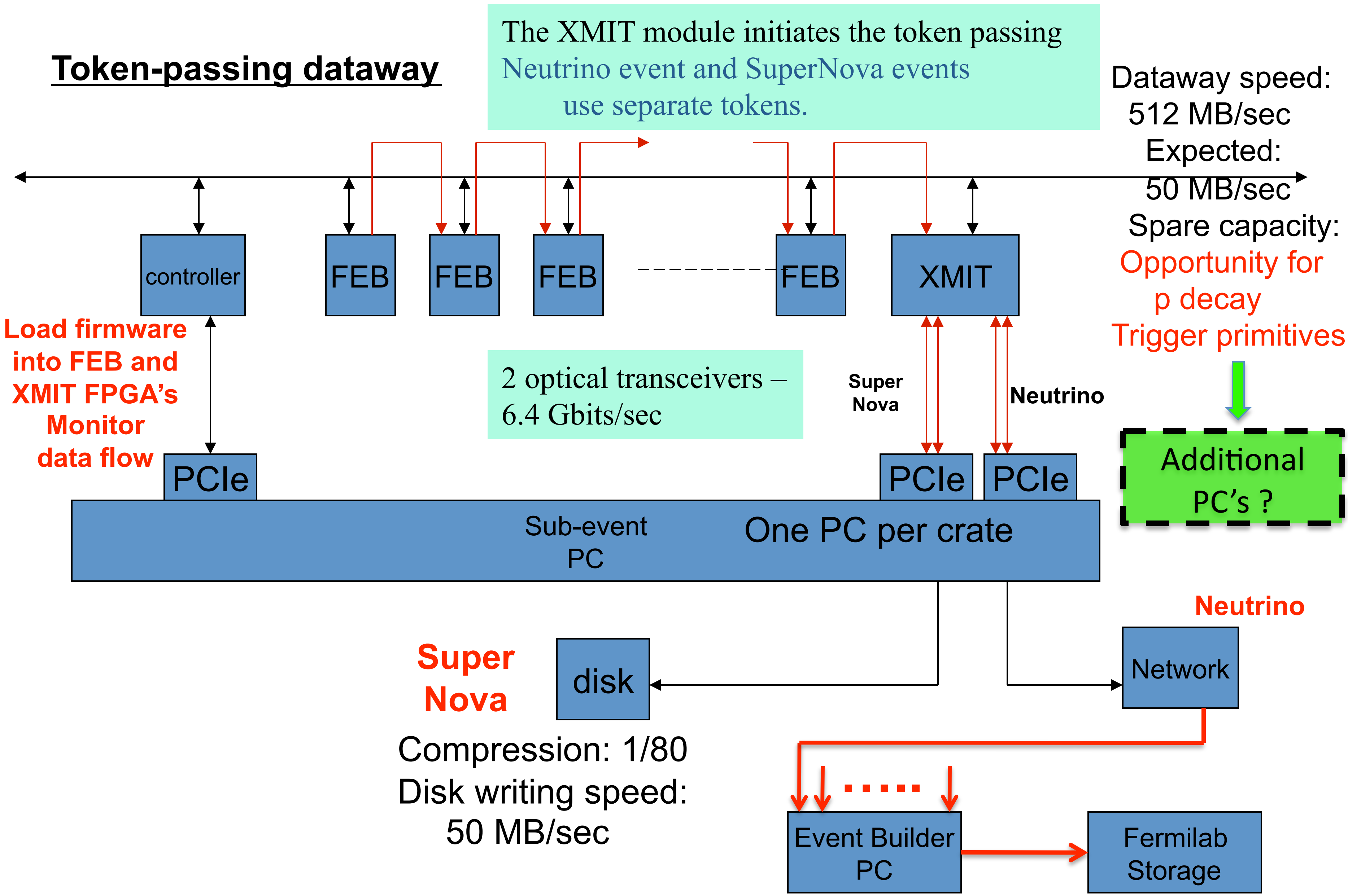
- **Read out in Channel order for compression**

  in alternate cycles: 64 MHz

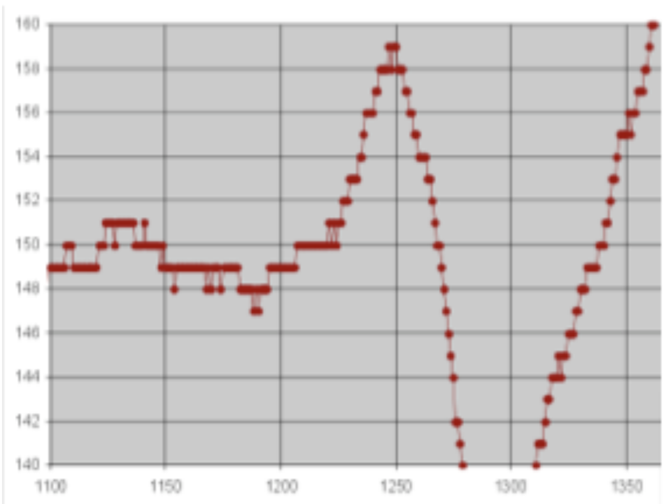
  Matches speed specs

Each buffer can accommodate 26 uncompressed (1.2 MB) events.

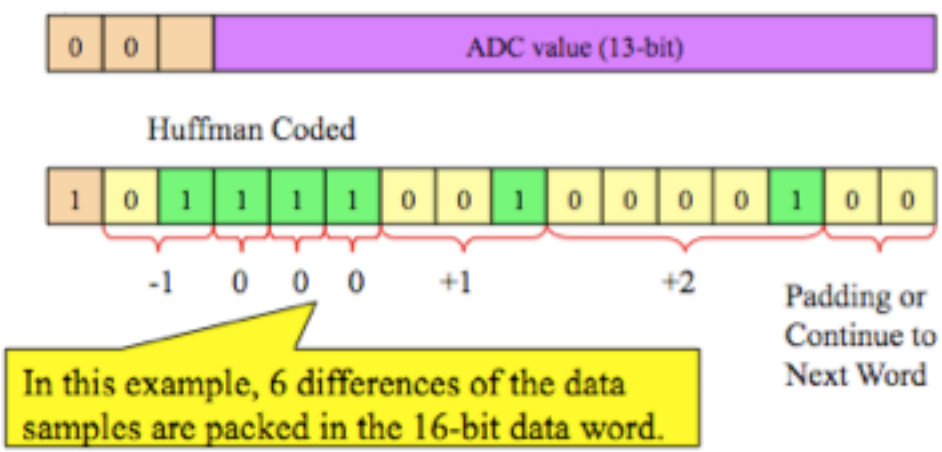
FEB Crate Level View



Data compression using Huffman coding



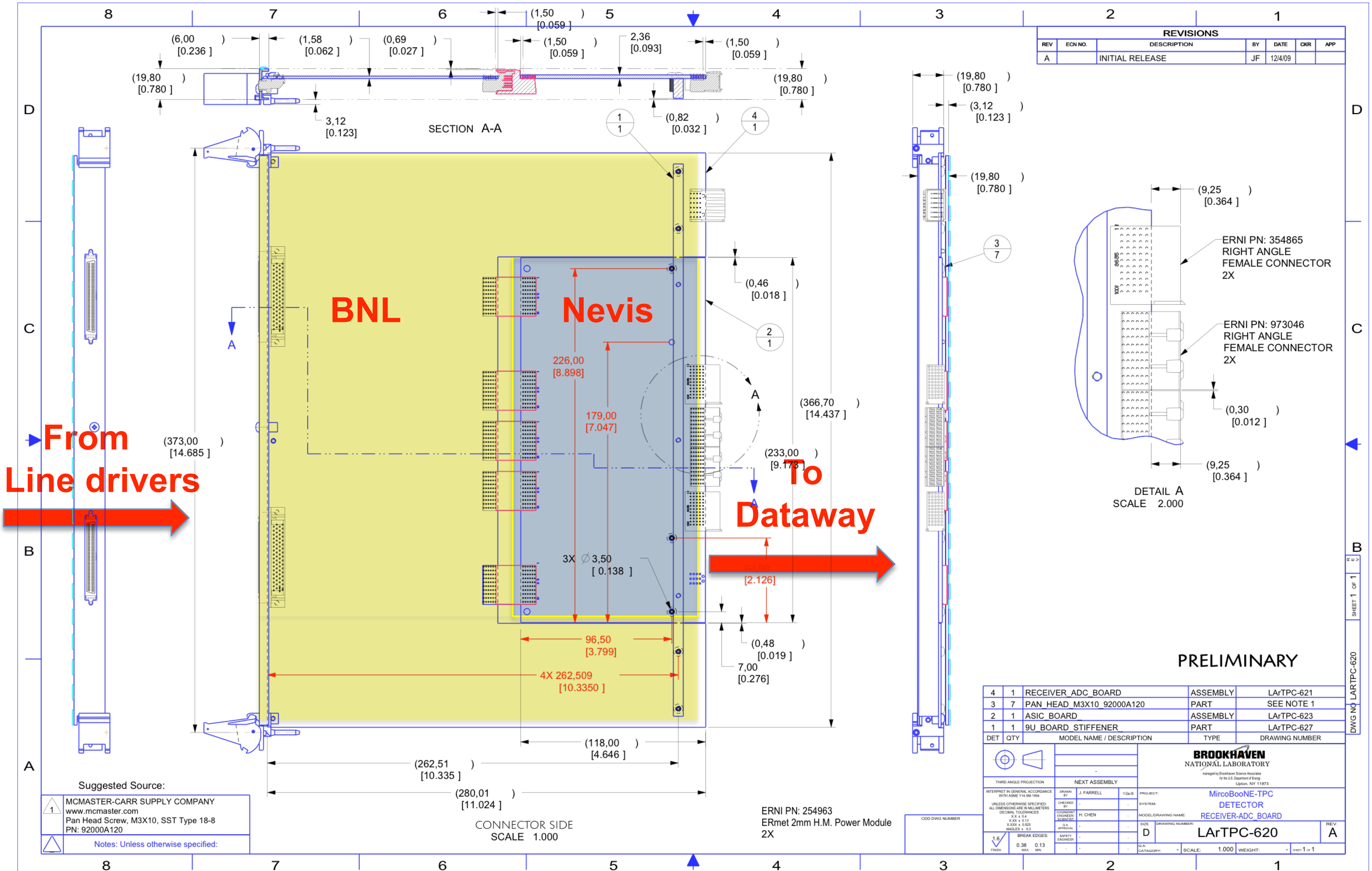
- **Slow variation of data**
- **Record Differences between samples**
- >99% of successive sample pulse heights differences are **-1, 0, +1**
- The most frequent differences are assigned the shortest codes.



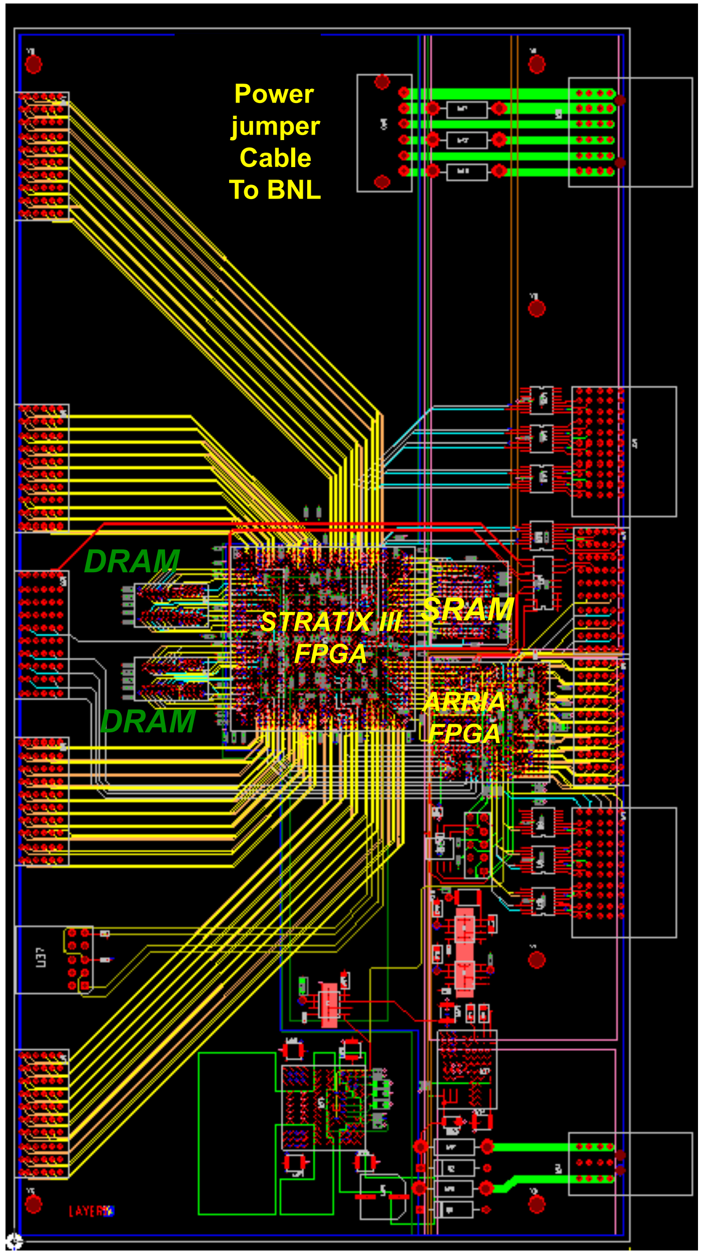
1st sample entered with no coding
In first word

Next samples: Differences coded and packed in successive words

TPC Readout Board (FEB) .



Nevis FEB PCB (Ready for Prototyping)



Analog power
+3V, -5V, +5V

Slow readout of data Through Crate Contr. → Readback path

Synch, trigs
Clock, run

Standard readout of data through XMIT → Token Passing Dataway

FPGA firmware → Download path

Digital power
+12V
(4.5V – 24V)

Serial
ADC
Clock
Data
in

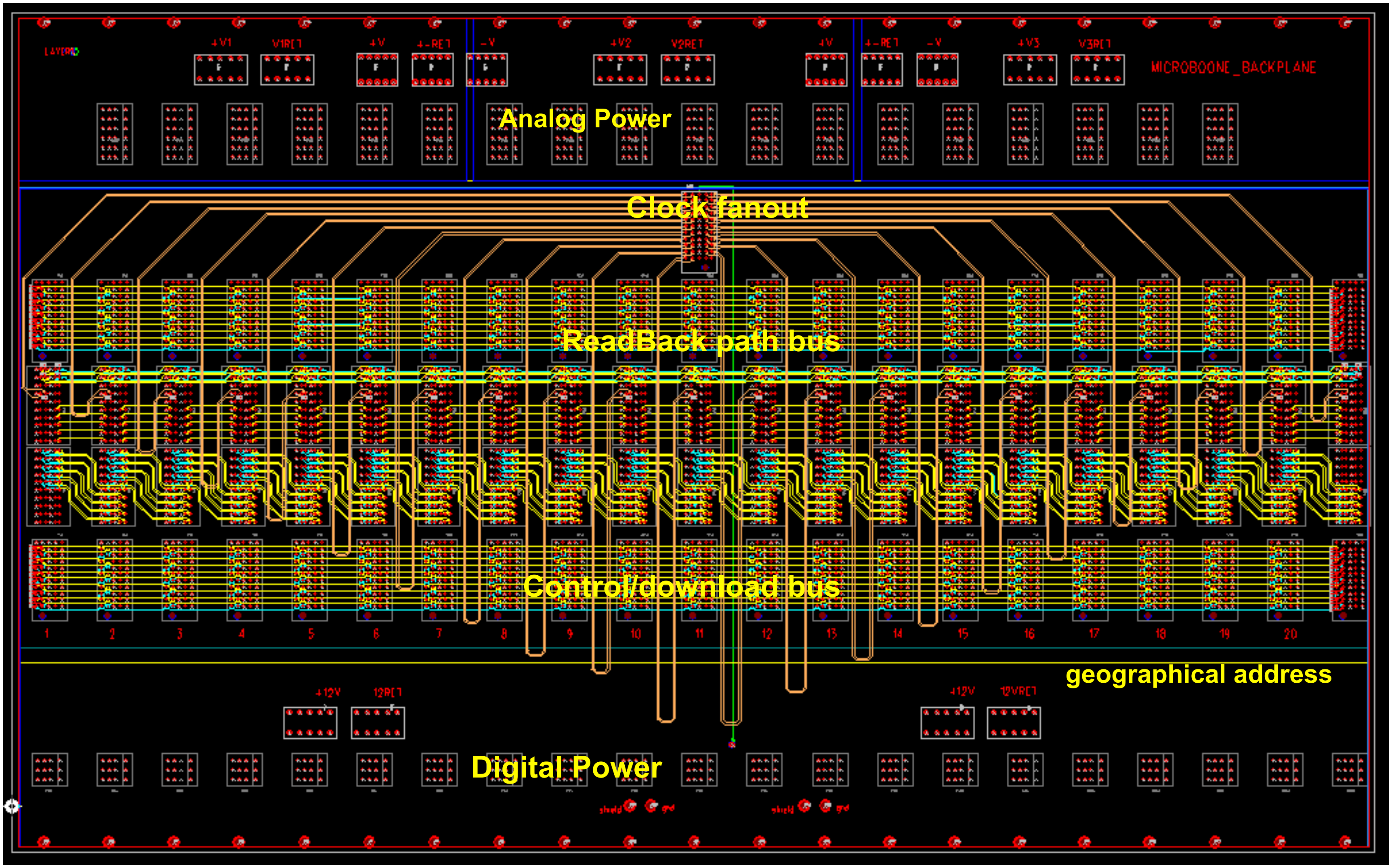
Clock
Trigger out
ADC serial

Stratix III
JTAG

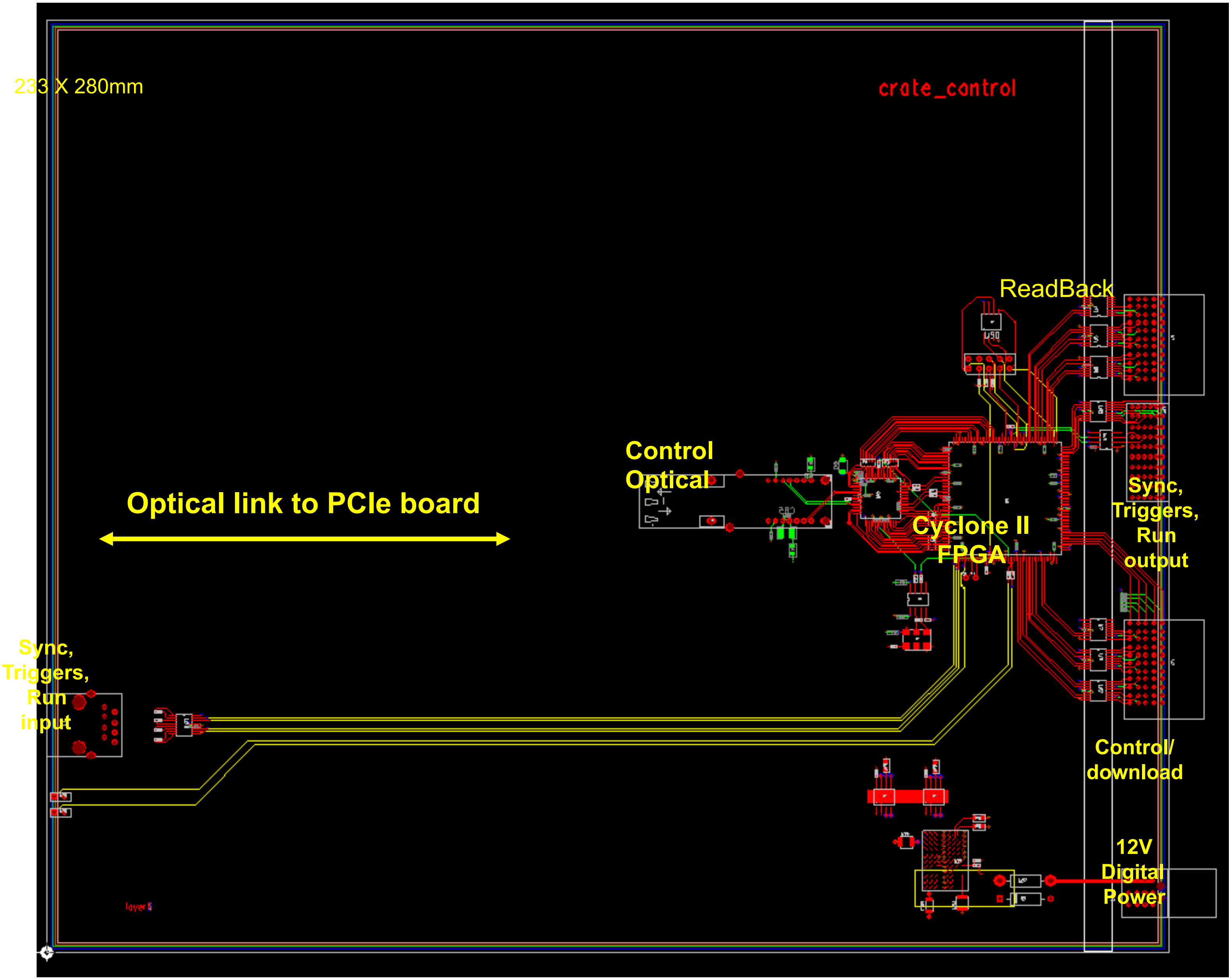
14 Layers
233 X 118 mm
High speed trace buried

Data flow

FEB Crate Backplane (Ready for prototyping)

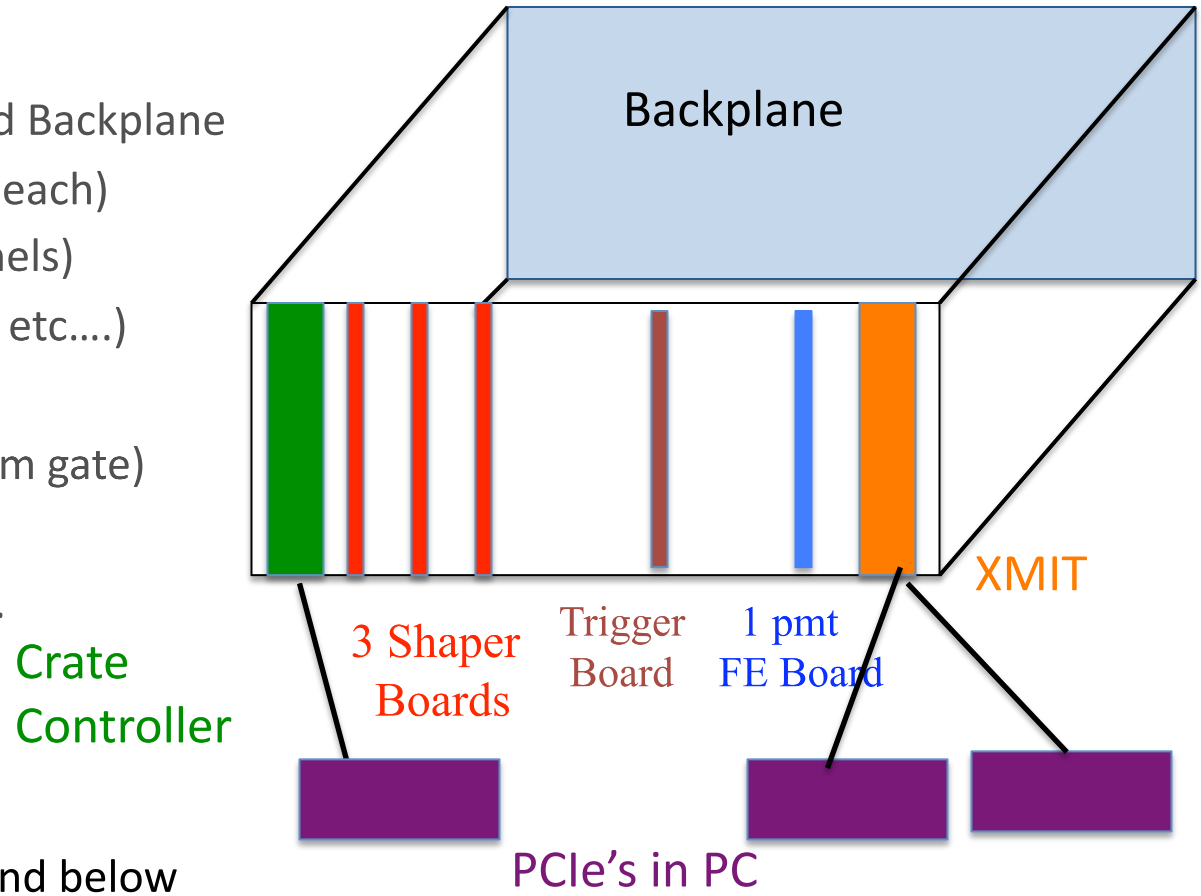


Controller PCB (Ready for prototyping)



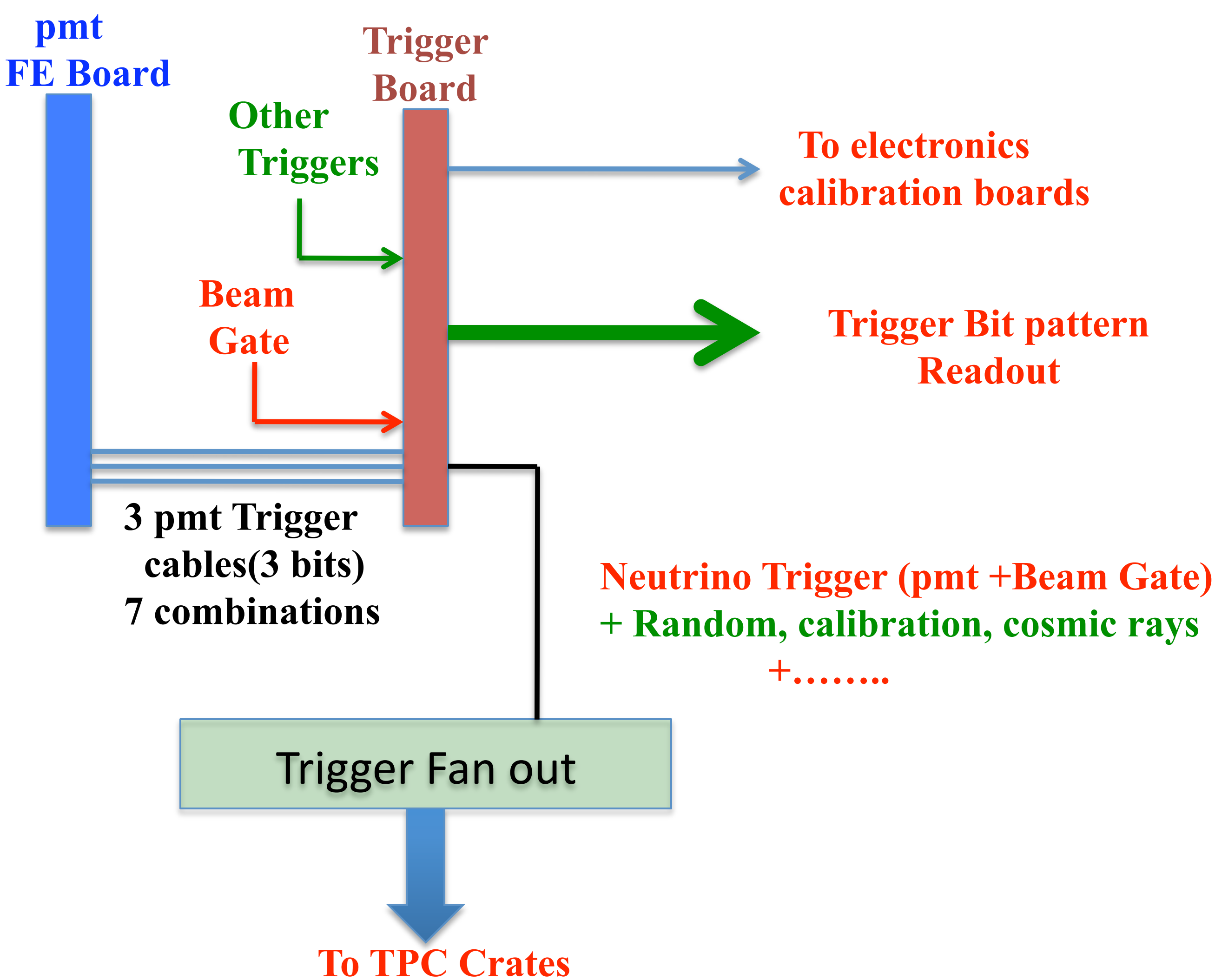
PMT and Trigger crate occupancy .

- Crate (1 FEB): mechanics and Backplane
- 3 shaper cards (16 channels each)
- 1 Front End Board (48 channels)
  ADC + Digital (FPGA, buffers etc….)
- Transmit (XMIT) Module
- 1 Trigger board (Trigger, Beam gate)
- Crate Controller
- 3 PCI express modules in PC.
- One PC.



- Cables from splitters
  Enter patch panels above and below PMT readout crate.
- Patch panels to shapers
- Shapers to ADC

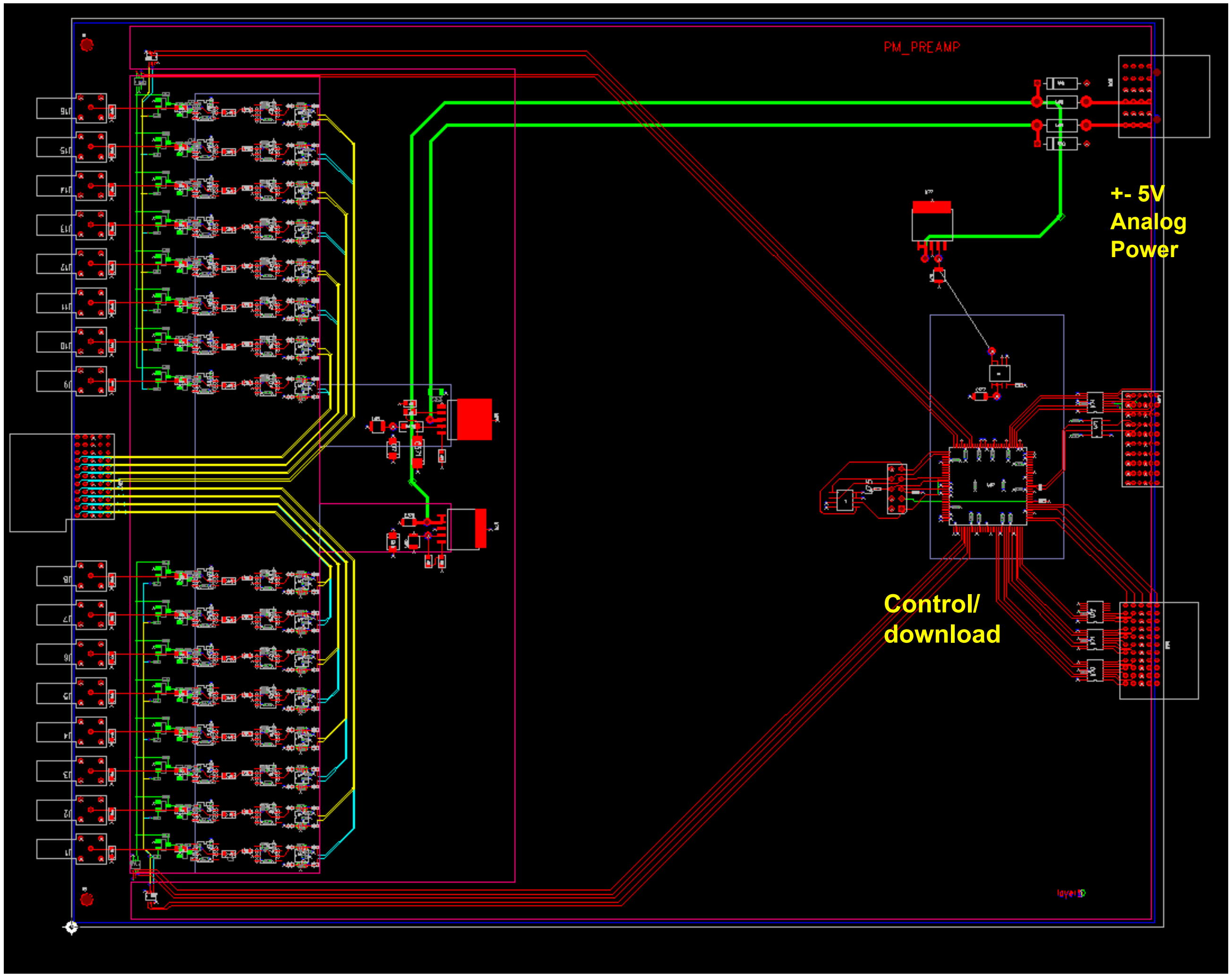
Trigger.


pmt
FE Board
Trigger
Board
Other
Triggers
Beam
Gate
To electronics
calibration boards
Trigger Bit pattern
Readout
3 pmt Trigger
cables(3 bits)
7 combinations
Neutrino Trigger (pmt +Beam Gate)
+ Random, calibration, cosmic rays
+……..
Trigger Fan out
To TPC Crates

PMT Shaper Board (Ready for prototyping)

PMT
In

Shaper
out



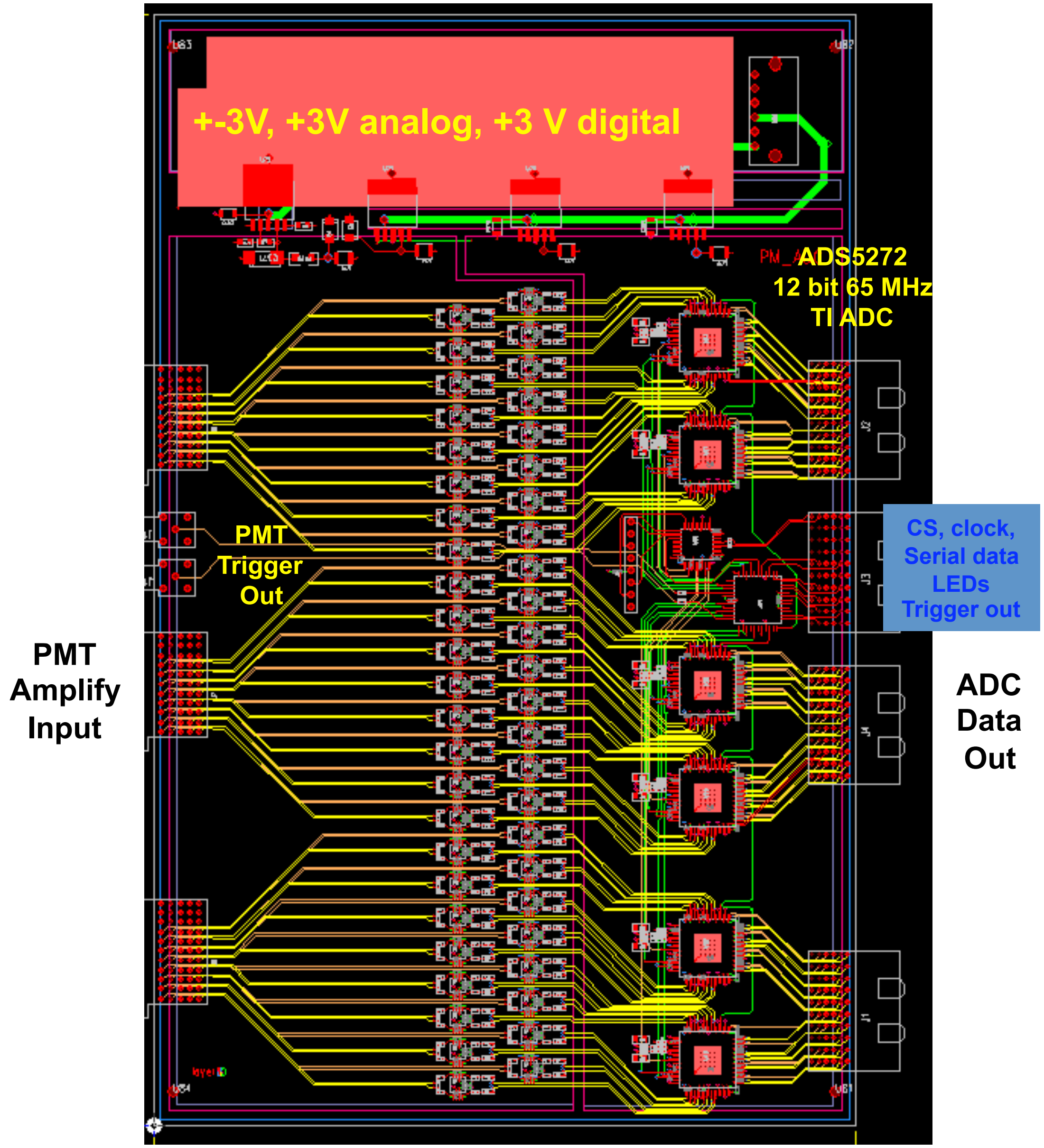
16 channel per board
233X280mm
Lemo connector for input
(patch panels above/below the PMT crate)
2mm HM cable output
2 DAC for even/odd
channel test pulse

Dec 2nd, 2010

PMT ADC board (Ready for prototyping)

233mm X 147mm
10 layers PCB

48 channel per board



Hardware Fabrication summary

10% spares + 3% Failure rate

Item	Needed	Spares	Total
FEB	129	18	147
Crates	10	2	12
Crates Backplanes	10	2	12
XMIT	10	2	12
Controllers	10	2	12
PCIe	10	2	12

Item	Needed	Spares	Total
Shaper boards	3	2	5
ADC board	1	2	3
Trigger Board	1	2	3

Proto 1, Proto 2, Fabrication sequence

Single Board Test

Internal Nevis
Proto 1
Testing
2/8/11→ 3/28/11

Joint Nevis/BNL
Proto 1
Testing
3/28/11→4/22/11

Full Crate SystemTest

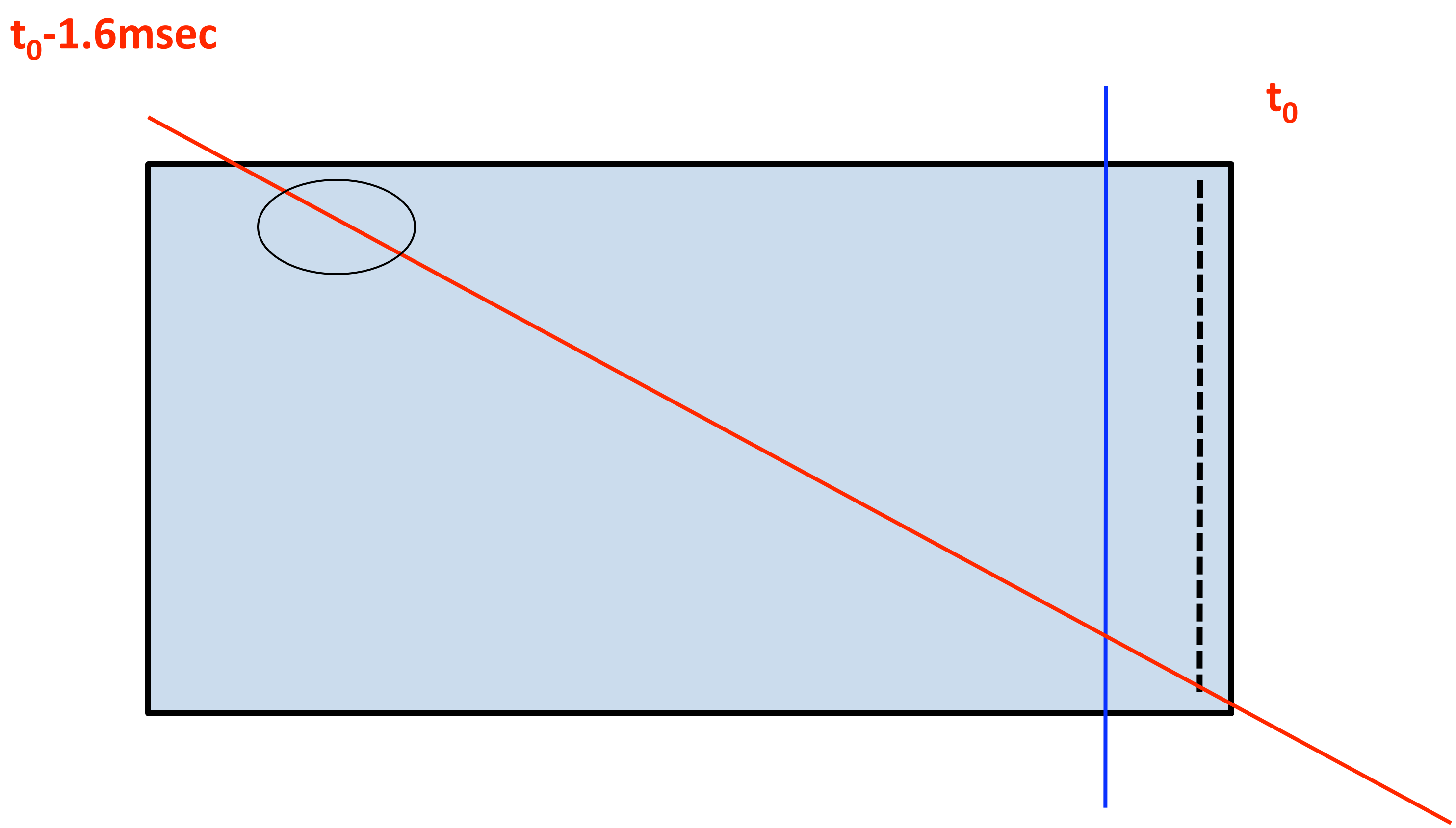
Internal Nevis
Proto 2
Testing
7/21/11 →8/9/11

Joint Nevis/BNL
Proto 2
Testing
9/21/11→ 12/15/11

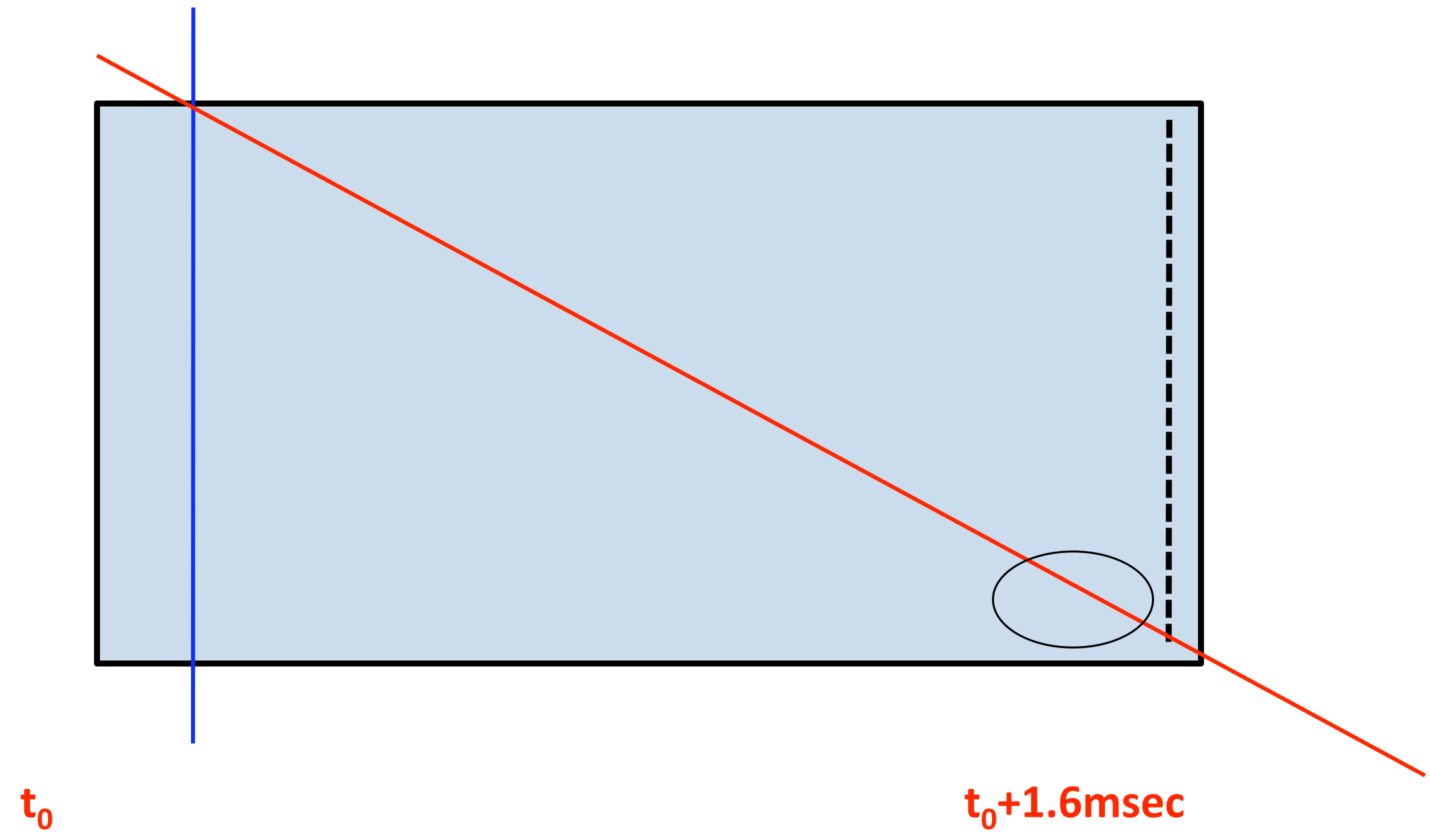
Production and Testing 12/16/11→9/28/12

Back up slides

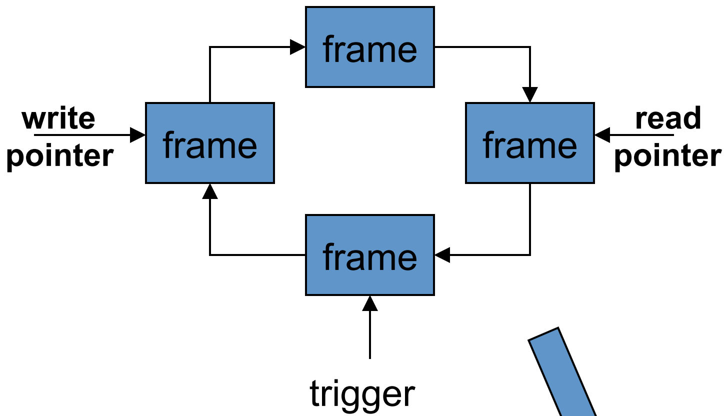
Scenario: 2 tracks: The good one at t0 (blue)and another one at t0 – 1.6 msec (red)
The red track ionization in the black circle will arrive at the wires at ~ the same time as the good track.
If we only read from t0 on, we will not know of the existence of the remaining red ionization and will therefore associate the circled ionization to the good track
If we read from -1.6 msec on we will see the whole early track and separate the two tracks.



Scenario: 2 tracks: The good one at t0 (blue)and another one at t0 + 1.6 msec (red)
The red track ionization in the black circle will arrive at the wires at ~ the same time as the good track.
If we only read up to t0 + 1.6 msec on, we will not know of the existence of the remaining red ionization and will therefore associate the circled ionization to the good track
If we read up to t0 + 3.2 msec we will see the whole late track and separate the two tracks.



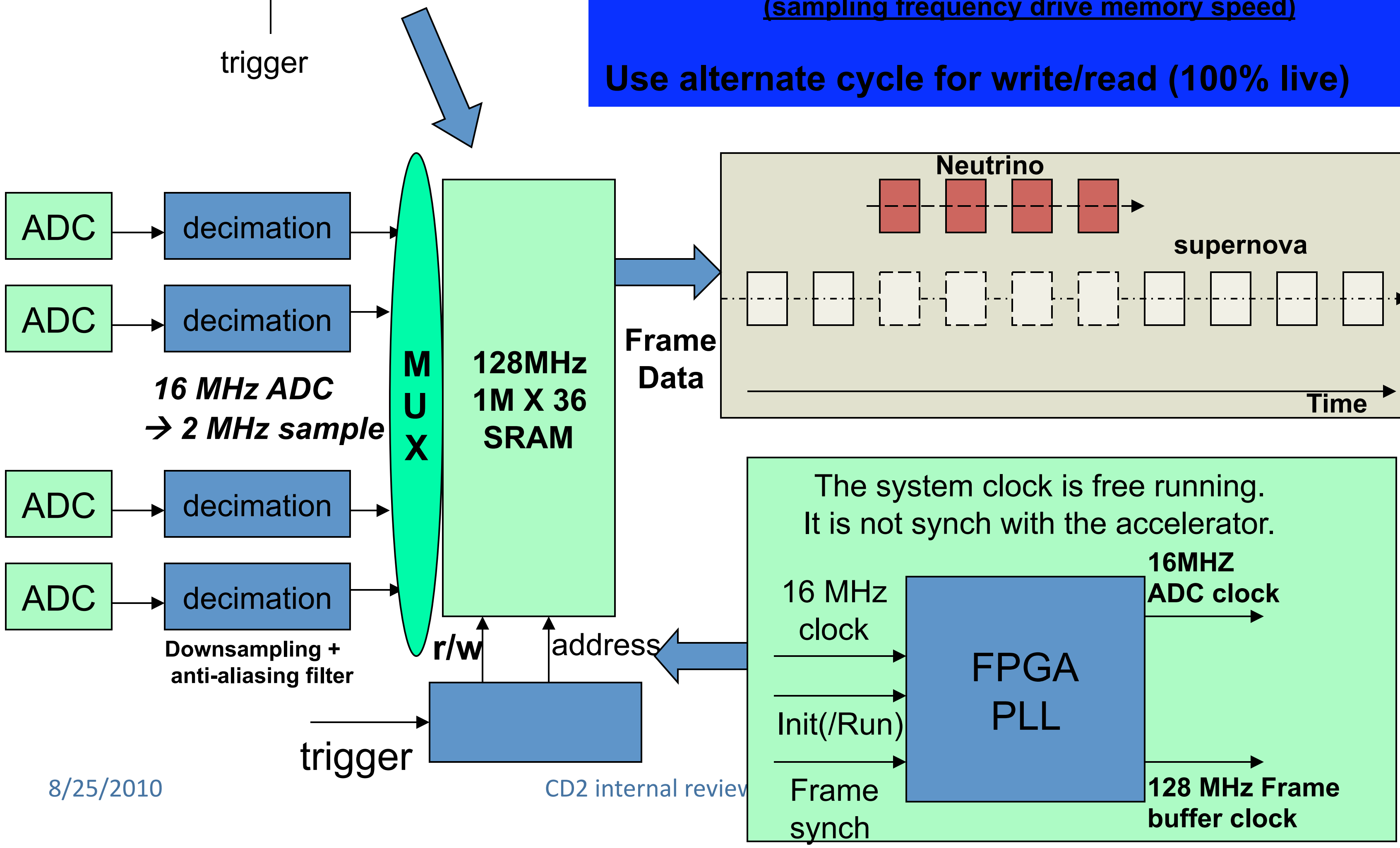
Data Sample memory



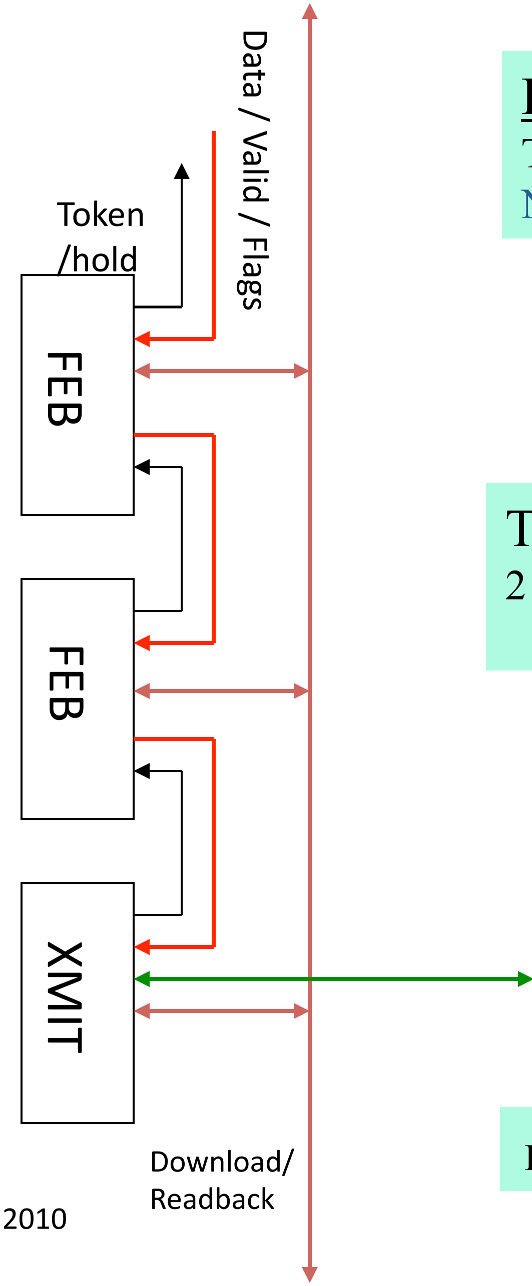
Arrange the sample memory into 4 frames
Each frame can store up 2ms of data
(currently set at 1.6ms)

Sampling speed set a 2MHz maximum
→ 2MHz* 64 channel =128MHz 16 bits word
→ 64 MHz 32 bits word (2 ADC's / word)
(sampling frequency drive memory speed)

Use alternate cycle for write/read (100% live)



❑ Digitizing Boards: Data Mover



16 FEB
1~2 XMIT
Per crate

Dataway: Token passing.

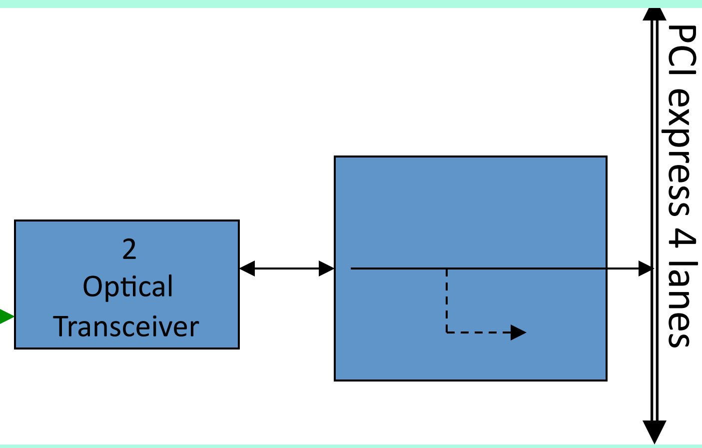
The XMIT module initiates the token passing

Neutrino event and SuperNova events use separate tokens.

The PCI express interface:

2 optical transceivers – 6.4 Gbits/sec

each PCI express lane can have 2.5 Gbit/sec speed



One PC
per
Crate

Hard Drive
For SN data

Route traffic differently depending on the header info (ν or SN)