SNAP Data Recorder 2

- Update of talk I gave last December
- Overview
- Scope of FNAL involvement in FY03
  - Feasibility of FLASH memories
    - Power advantage (1/10th) over DRAMs
    - Open issues with read/write speed, read/write cycles, architecture, fault tolerance, error detection and correction
    - Open issues (any dense technology) with radiation susceptibility in a space environment
- Next steps

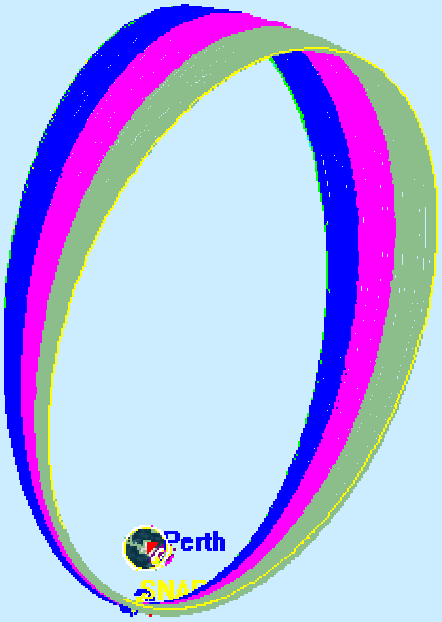
SNAP Baseline

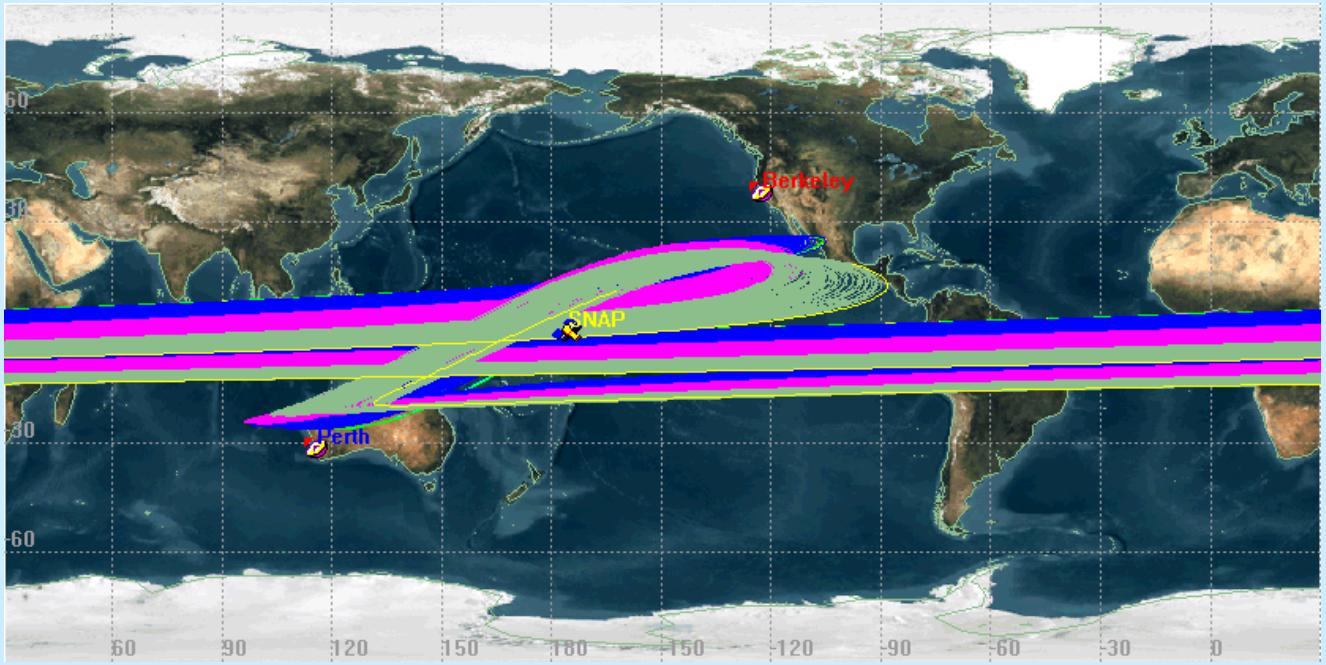
- "A solid state recorder – a shoebox"
  - No moving (rotating) parts
  - Lots of memory
  - Radiation / space qualified
  - Low power

- SNAP plans to transmit data in Kα band @ 300 Mbs with 6W transmitter.
- 350 Gbyte storage requirement (after compression). 675 GB transmittable at 300 Mbs for 5 days

Data requirements

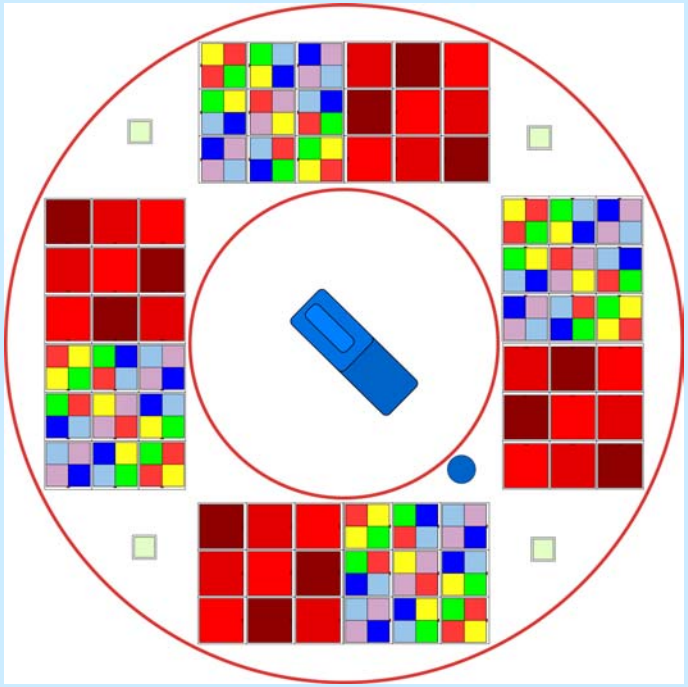
- 3 day elliptical orbit: 2.5 Re x 25 Re
  - 62 hours of data taking
  - 11.2 hours in radiation belts (16%)
  - 5.2 hours over Berkeley





SNAP data volume

- CCDs: 36 sensors(4 filters per)
  - 3.5K x 3.5K: 10.5 μm pixel
  - 350-1000 nm λ's
- Near-IR: 36 sensors HgCdTe
  - 2048 x 2048: 18 um pixel
  - 0.9 – 1.7 um λ's
  - 2 averages of 4 reads?
- 16 bit dynamic range
- Single exposure: 9.5 Gbits



SNAP data volume (cont)

- 300 sec exposure + 20 sec read
- 218000 seconds per 3 day orbit
- Total: 6.5 Tbits (811 GBytes)
- Compression factor of ~2.3 gives 350 GB
  - -> estimates from Rhodes report of 1000 sq deg survey. In the mix of photometry and spectroscopy, data storage requirement are about 50% less.
  - Bottom line is that several 1000's of Gb-size memory chips are needed

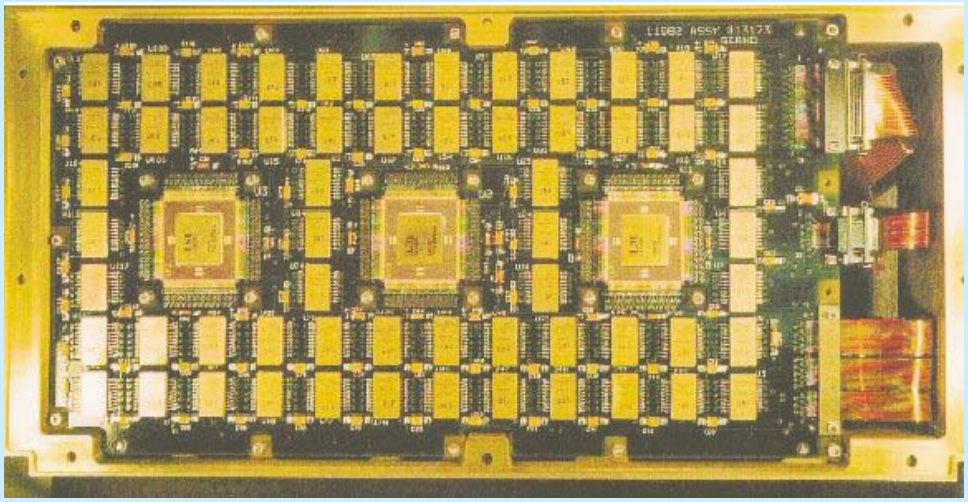
Memory technologies

- Memories
  - Dynamic RAM
    - Parasitic capacitance needs power to refresh
  - Static RAM
    - 2 transistors + 4 resistors FLIP-FLOP
  - FLASH memories
    - Floating gate with tunneling processes
  - FeRAM
    - Ferromagnetic crystal storage
  - Holographic and other technologies
- Tape and disk recorders are candidates

Some current missions

- Cassini

  - Two SSRs each of 2.5 Gbit
  - 640 4Mbit DRAMs
  - Early 90's technology => '97 launch
  - Multiple-bit upsets observed despite testing (architecture flaw)



-3 control ASICs
-120 DRAM/board
-Error detection and correction circuitry

Some current missions

- Hubble Space Telescope
  - Reel-to-reel tape replaced by SSR
    - 1.2 Gb -> 12 Gb
    - 1440 16 Mbit DRAM
    - Two stacks of 10 (+2 spare) for 320 Mb packages (still 12500 chips for 500 GB)

  - Single event upsets observed
    - EDAC (Reed-Solomon scheme)
    - Two events where memory corrected but damaged

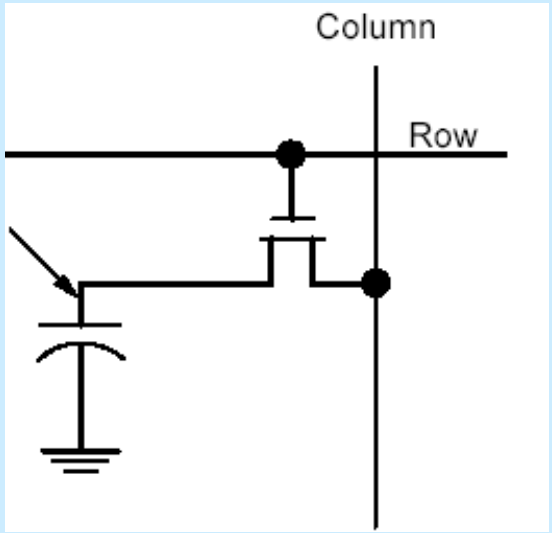
Challenges for SNAP

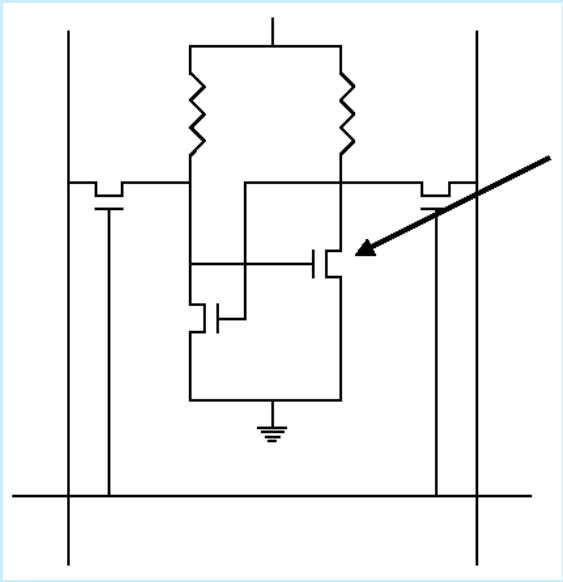
- Amount of memory
  - No examples of large (>>1 GB) SSRs found
  - Moore's Law growth. Need ~4000 x 1 Gbit
- Mass budget
  - Boards with 1000's of chips is several 10's lbs
- Power budget
  - Meeting at LBNL emphasized this over mass
- Radiation tolerance
- Space qualification

Radiation Tolerance

- Ionizing radiation small (<50 Krad)
- SEE (Single Event Effects) include many failure mechanisms
- SEU (Single Event Upset) can change state of a bit

DRAM Sensitive area

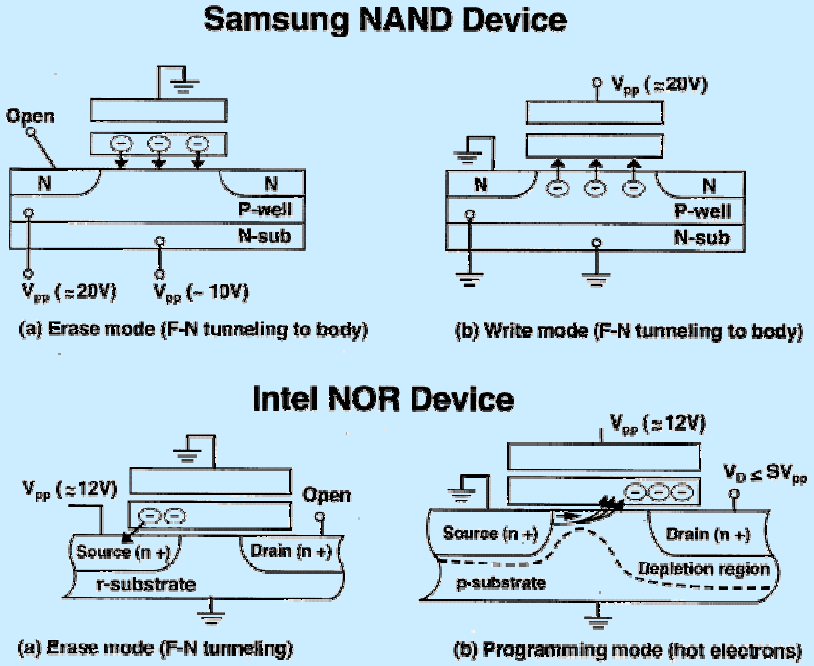


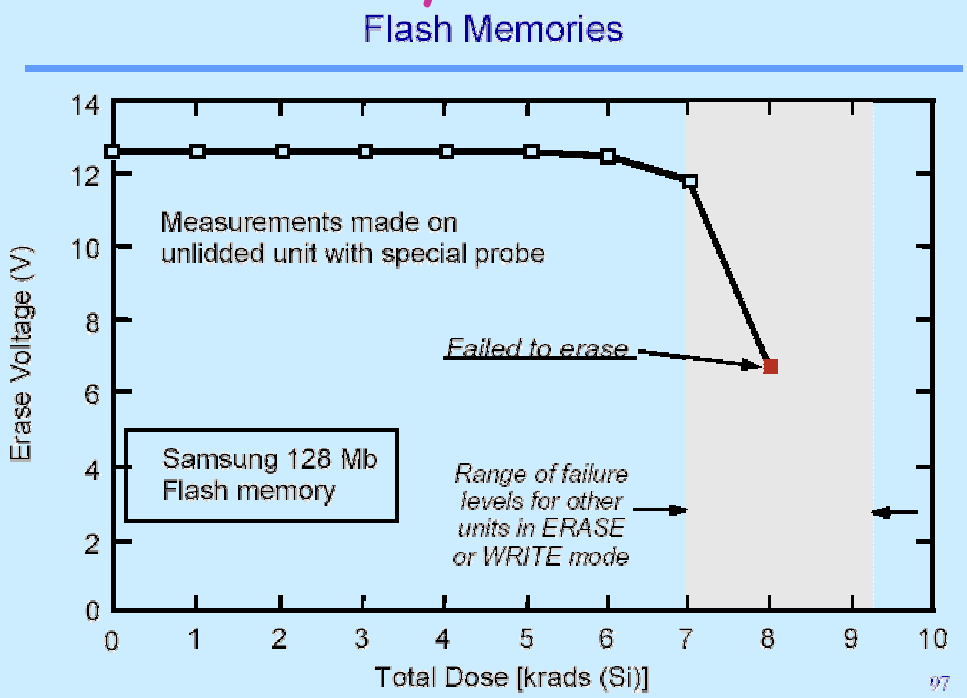


SRAM Sensitive area

Radiation Tolerance

- FLASH memories
  - Very thin oxides make FLASH susceptible
  - Charge pump is the suspect for many failures
  - Limited number of read/write cycles





Space qualification

HST HOST Mission

- Thermal-Vac
  - Vacuum and Temperature extremes (-40 to +90 degC)
- Vibration facility
  - Hard shake
- More Thermal-Vac and vibration testing after mount
  - Room filled with engine noise simulation

Space qualification

GSFC-S-480-89

PERFORMANCE ASSURANCE
REQUIREMENTS (PAR)
FOR THE
SOLID STATE
RECORDER

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

National Aeronautics and
Space Administration

CONTENTS

Space qualification

CONTENTS (Continued)

Para.

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Space qualification

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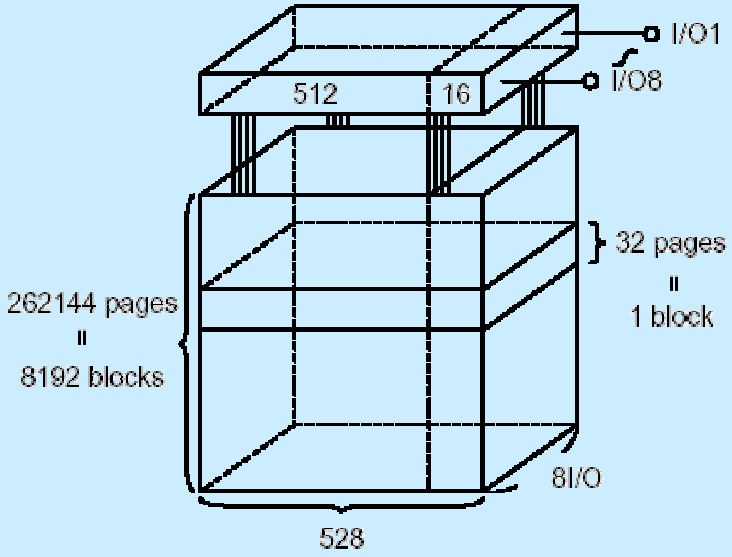
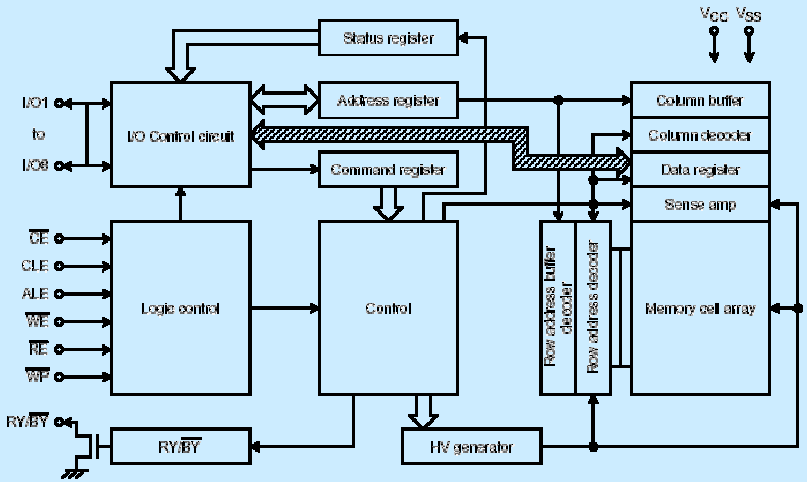
FNAL FY03 Plans

- Address the question "Is FLASH memory a viable technology for the SNAP SSR?"
- Plans
  - Design and build a test board to operate and evaluate a dense FLASH memory chip
  - Continue literature search
  - Talk with SSR vendors
  - Talk with JPL radiation testing group
  - Design (and do?) radiation exposure of the evaluation board

Evaluation Board

- Design and produce board ($1K, June 1)
- Procure FLASH chips ($500, April 1)
- Interface to PC with simple programming protocols (i.e. BASIC or FORTRAN) and get board working (July 1)
- Evaluate board and design radiation exposure measurement (Aug 1)





Other next steps

- Literature search
  - Space experience and IEEE articles
  - Characterization of radiation environment
- Talk with SSR vendors
  - Initial email exchange started with SEKR
    - Told SNAP DRAMs OK, told me FLASH OK
    - Also estimated they could take care of it with 1.5 to 3 years and $3M - $15M
- Talk with JPL radiation testing group
  - For money, they will space qualify parts
  - Maintain a list of space qualified parts