

# An FPGA TDC for Time-of-Flight Applications

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## Abstract:

An 18-channel time-of-flight (TOF) grade time-to-digit converter (TDC) has been implemented in a low cost FPGA device. The TDC has the following unique features. (1) The time recording structures of the TDC is based on the “wave union TDC” we developed in our previous work. A leading edge of the input hit launches a bit pattern, or wave union into the delay chain-register array structure which yields two usable measurements. The two measurements effectively sub-divide timing bins for each other especially the “ultra-wide bins” caused by the FPGA logic array block (LAB) structure and improves measurement precision both in terms of maximum bin width and RMS resolution. A coarser measurement on input signal trailing edge is also provided for time-over-threshold (TOT) applications. (2) The TDC supports advanced timing reference distribution schemes that are superior to conventional common start/stop schemes. The TDC has 16 regular measurement channels plus two channels for timing reference. The timing reference is established with multiple measurements rather than single shot common start/stop. An advanced scheme, the mean-timing approach even eliminates needs of high quality timing distribution media. (3) The ASIC-like encapsulation of the FPGA TDC significantly shorten the learning curve for potential users while maintain certain flexibility for various applications. Necessary digital post-processing functions including semi-continuous automatic calibration, data buffer, data link jam prevention logic etc. are integrated into the firmware to provide a turn-key solution for users.

## Summary:

Carry chain structure can be used to implemented TDC in FPGA. However, the logic elements in the FPGA are organized in logic array blocks (LAB) and at the crossing of the LAB boundaries, extra delay are added into the delay chain resulting in periodic “ultra-wide bins”. In our previous work, a logic scheme called “Wave Union Launcher” is designed to sub-divide ultra-wide bins in the raw TDC measurements. A wave union launcher creates a pulse train or “wave union” with several 0-to-1 or 1-to-0 logic edges for each input edge and feed the wave union into the TDC delay chain/register structure, making multiple measurements as shown in Fig. 1.

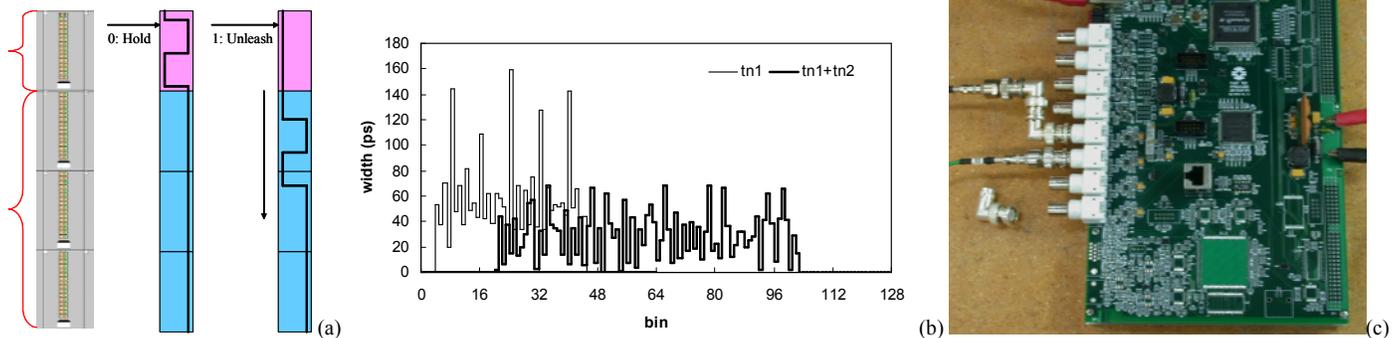


Fig. 1. The wave union TDC: (a) the wave union launcher and time recording array (b) bin widths plot (c) the TDC module

When the input is low, a bit pattern is formed in the wave union launcher, implemented in one LAB containing 16 logic elements as shown in Fig. 1(a). Once the TDC input is high, the bit pattern or wave union is unleashed and it propagates down in the carry chain/register array structure. At the leading edge of the system clock (400MHz), the bit pattern is recorded in the register array and its relative position represents the arrival time of the TDC input. The two 1-to-0 edges are encoded to extract the input arrival time. Note that in regular TDC without wave union launcher, the input is directly connected to the delay chain and only one transition edge is recorded and encoded for input time. In Fig. 2(b) the sum of the encoded positions of the two edges marked as “ $tn1+tn2$ ” is compared with the output of the regular single-edge TDC. It can be seen that the ultra-wide bins are now sub-divided and the maximum bin width is about 65ps comparing with 165ps in regular TDC. Since the bins now have various widths, bin-by-bin calibration is necessary. Based on our previous work, after the bin-by-bin calibration, an RMS resolution of about 25ps can be achieved. The trailing edge time is measured in the clock cycle when the wave union recovers which is a single measurement with a coarser resolution but is sufficient for most of time-over-threshold (TOT) applications. Fig. 3(c) shows the test module with FPGA TDC.

There are additional challenges beyond implementing the time measurement array when multiple channels are packed in an FPGA and multiple FPGA TDC devices are used for a large time-of-flight (TOF) system. A major task for such systems is to distribute the common timing reference. Two extra TDC channels are implemented in addition to the 16 regular channels for establishing time reference. The two timing reference channels are assigned to two input banks with 8 regular channels in each bank. Temperature variation between the reference channels and regular channels is expected to be mainly cancelled given that they have identical time measurement structure as the regular channels.

The primary motivation of using timing reference channels is to support advance timing distribution schemes. In conventional common start/common stop schemes, the common timing signal is distributed in a single shot, suffering circuit jitter and binning errors in TDC. In our design as shown in Fig. 2(a), the reference time inside FPGA is an average of multiple (e.g. 8) measurements. The timing distribution system produces a common timing burst of 8 pulses and the times of the leading edges are digitized relative to the local PLL clock inside the FPGA and then averaged as the timing reference.

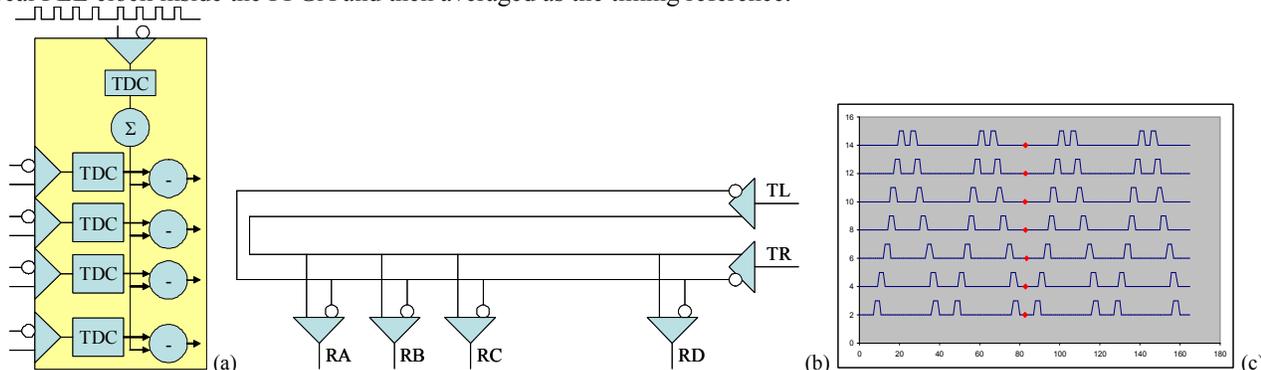


Fig. 2. Timing Reference: (a) The Timing Reference Channel (b) Distribution Network for Mean Time Scheme (c) Waveforms at Receiving Points  
 A very attractive timing distribution method is the mean timing scheme. The timing distribution system drives a multi-drop copper twist pair cable from both ends as shown in Fig. 2(b). The differential signals are received in each TDC module/FPGA and the arrival times are digitized. The mean timing burst has 8 pulses as shown in Fig. 2(c). The left and right end drivers are alternatively enabled and drive pulses to travel from left or right end. The receivers on each TDC FPGA receive the burst with 4 pulses delayed from left path and 4 from right path. The arrival times at different TDC modules are different, but the mean times of the 8 pulses as indicated with the red dots in Fig. 2(c) are the same.

The only required condition in this scheme is that the cable segments have the same propagation delays for left-going and right-going pulses. There is no requirement on actual values of the delays and temperature variations and therefore, no requirement of using high quality media. Any moderate grade media like Cat-5 twist pair cables or even ribbon cables can serve this purpose. The TDC supports either common burst mode or mean time mode without any changes in the firmware. The distribution network shown above is DC coupled. In our full paper, mean time scheme with AC coupled network will be discussed.

A feature of this design is the ASIC-like encapsulation. It is known that FPGA TDC is ultra-flexible and suitable for different user projects. However, the FPGA TDC design requires certain carefulness in various aspects beyond typical FPGA digital design practice and it may become a long learning curve for potential users. Our firmware is designed as if the FPGA is used as an ASIC TDC that provides a turn-key solution for users in wide range of applications.

An auto calibration functional block is provided for bin-by-bin calibration. The calibration process is semi-continues during the normal operation of TDC. The random input hits are booked into a DNL histogram implemented with FPGA internal RAM. Each time after 16K hits are booked, the contents of the histogram are integrated and used to update the lookup table. The TDC measurements are checked through the lookup table and the center time values in picoseconds of the input bins are output. The lookup table automatically keeps track of the net effect of the temperature and the power supply voltage during the past 16K hits.

The following table shows performance parameters of the TDC. Given the high double hit rate supported, an average rate limiting logic for each channel and the output data jam prevention logic become unavoidable. The detail will be discussed in our full paper.

Minimum pulse width	5 ns after previous leading edge.	
Maximum double hit rate	5 ns after previous trailing edge.	
Maximum average hit rate before losing hits in a channel	8 hits/2.56 us/CH	
Maximum average hit rate before losing hits for 16 channels (Free running mode)	1 LVDS output pair	24 hits/2.56us
	2 LVDS output pairs	48 hits/2.56us
	3 LVDS output pairs	96 hits/2.56us
	4 LVDS output pairs	144 hits/2.56us

Flexibilities are designed into the firmware to fit users' demands with minimum efforts. For example, the users are allowed to use the TDC in non-trigger free running mode with 1, 2, 3 or 4 differential LVDS outputs even without having to set a register bit. Also, as mentioned earlier, the timing reference can be in either common burst mode or mean time mode without any changes.

To pack 18 channels into the FPGA, silicon resource usage is carefully planned. An internal RAM (M4K) with 4608 bits serves one channel for both leading edge and trailing edge calibration tables and temporary FIFO. The resource usage reported by the Altera Quartus II compiler is shown in the following table:

Device: EP2C8T144C6, Price: \$28 (April 2009), Operating Frequency: 400MHz, Total Logic Elements: 8256, Total M4K blocks: 36		
	Logic Element Usage	Memory Usage
18 CH TDC and output data path	6423	22 M4K blocks
Supporting circuits		9 M4K blocks
Whole chip	7139 (86%)	136192 bits, 31 M4K blocks