An aerial photograph of the Fermilab facility. The image shows a large, circular track or road that winds through a green, wooded area. In the background, there are several large, modern buildings, including a prominent one with a curved facade. The surrounding landscape is a mix of green fields and brown, cleared areas. The sky is clear and blue.

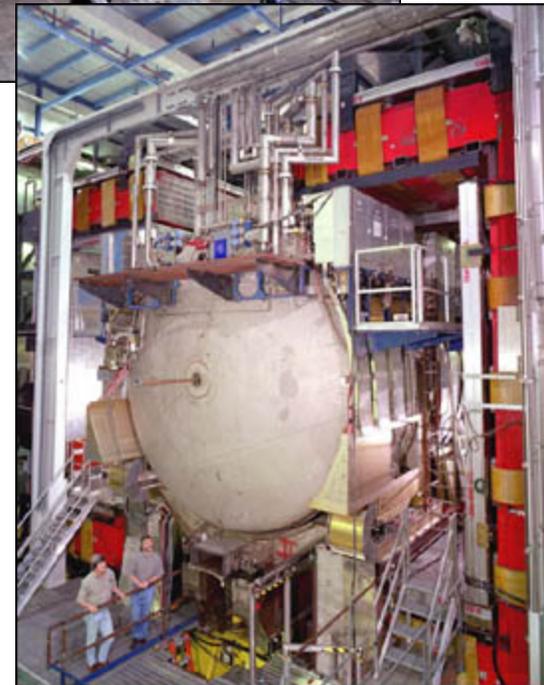
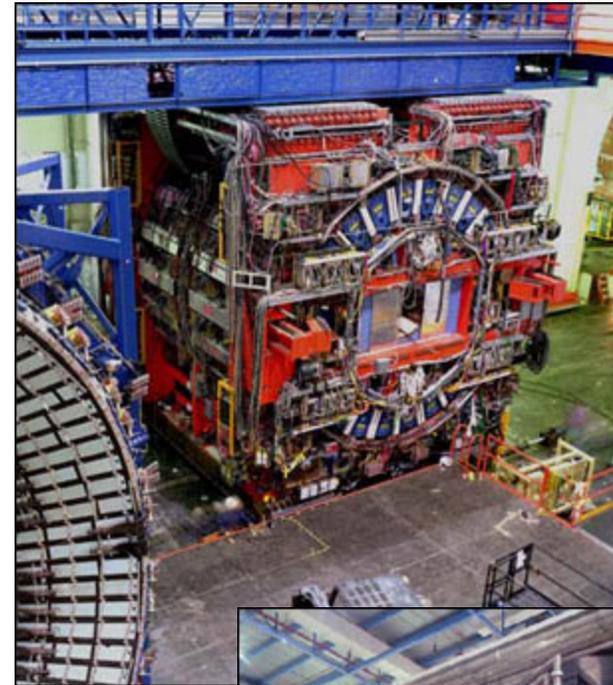
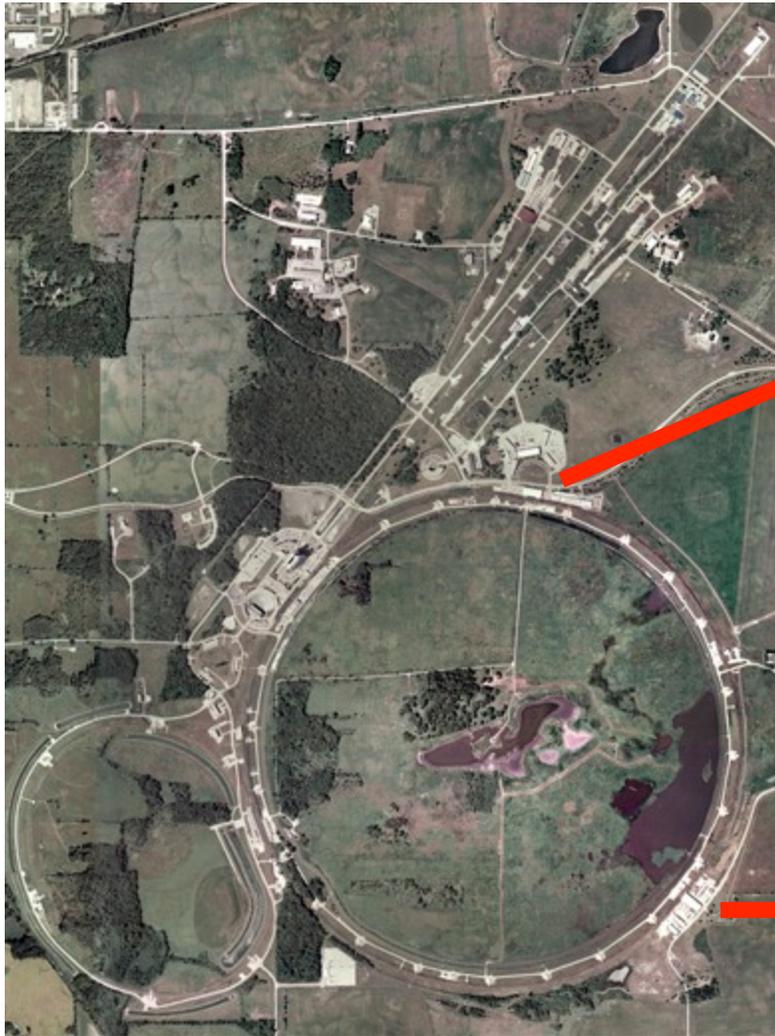
PET Fundamentals: Electronics (1)

Wu, Jinyuan
Fermilab
Apr. 2011

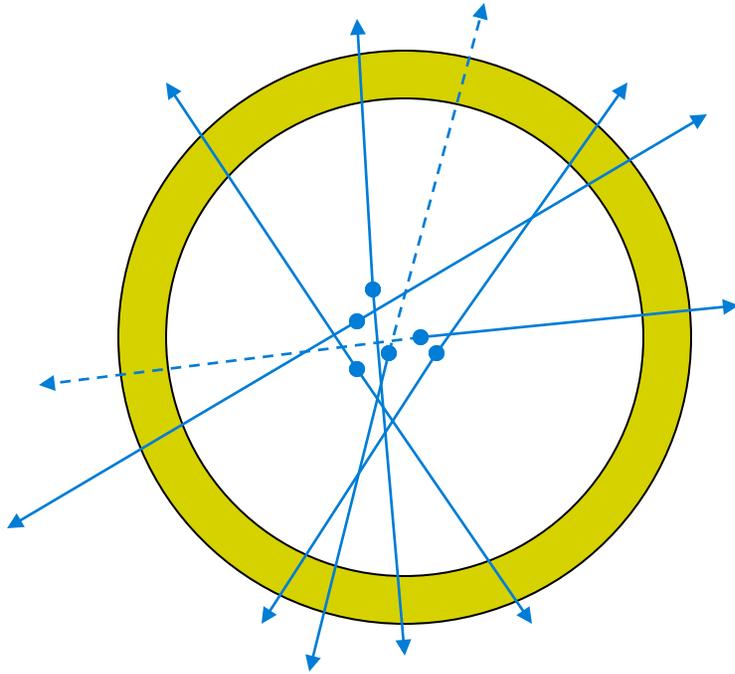
Fermi National Accelerator Laboratory



Colliding Experiments



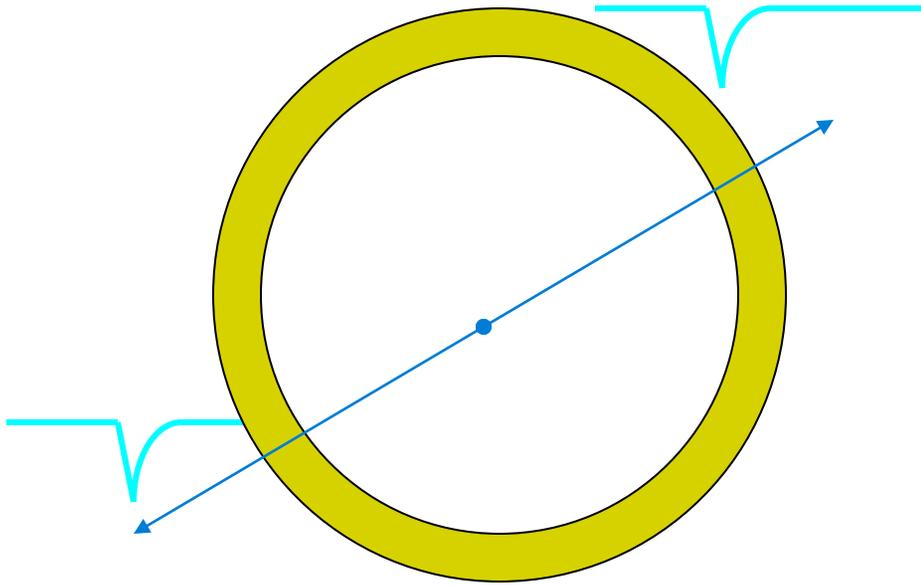
Questions



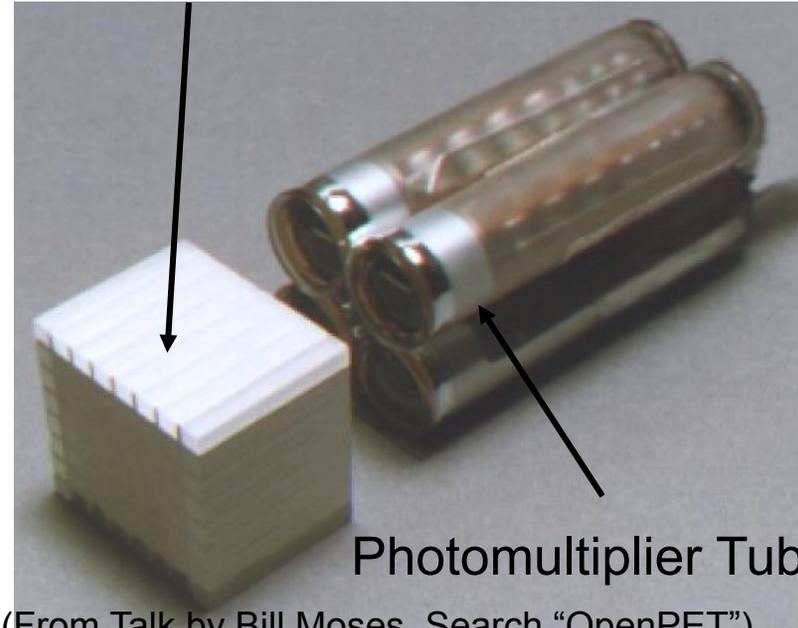
- PET?
- 511 keV?
- Back to Back?
- Speed of Light?
- ADC?
- TDC?
- FPGA?

PET Electronics Overview

Things to Measure



Array of Scintillator Crystals

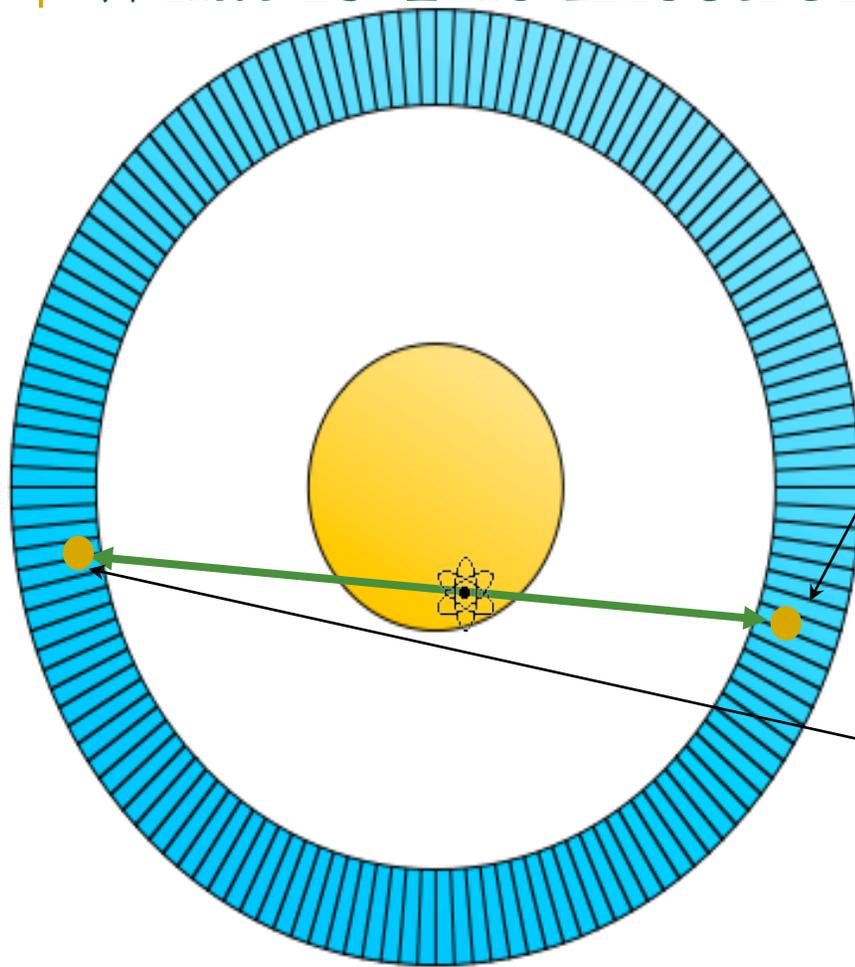


Photomultiplier Tubes

(From Talk by Bill Moses, Search "OpenPET")

- Total Charge:
 - Charge is measured to calculate the photon energy.
- Hit Time:
 - To pair up two hits, timing resolution about 1 ns is needed.
 - To improve imaging quality, time-of-flight (TOF) measurement good to ~50 ps is needed.
- Hit Position:
 - The positions crystals being hit are end points of the chord line.

What Is The Electronics Concept?



“Singles Event”

- Position (crystal of interaction)
- Time Stamp (arrival time)
- Energy Validation (=511 keV?)

Δt

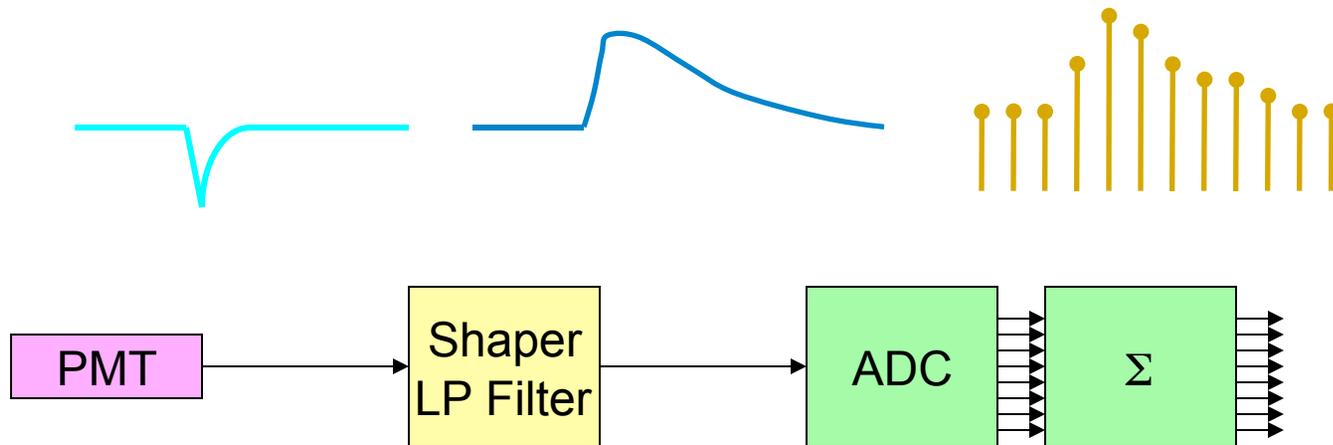
“Singles Event”

- Position (crystal of interaction)
- Time Stamp (arrival time)
- Energy Validation (=511 keV?)

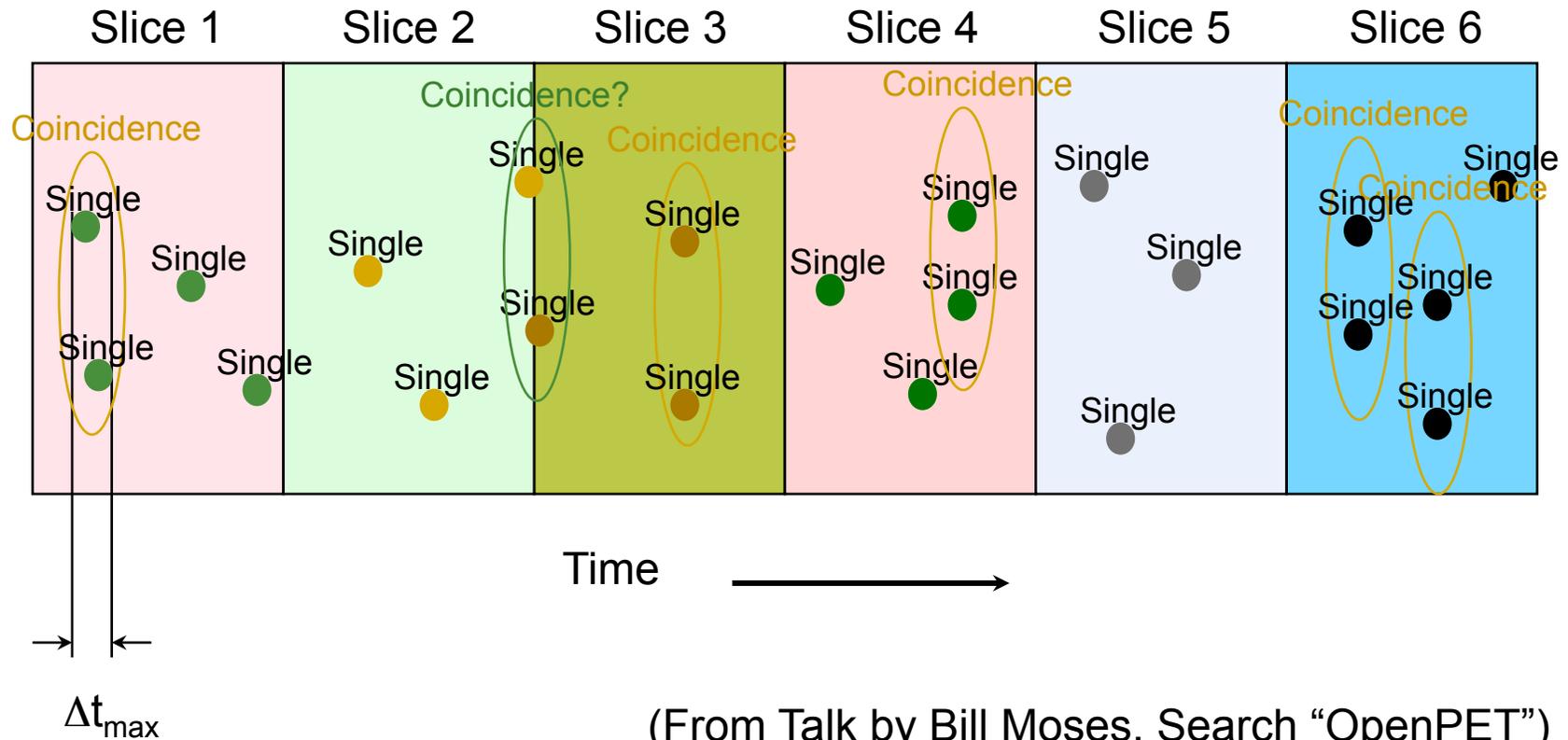
(From Talk by Bill Moses, Search “OpenPET”)

- Identify “Singles Events”
- Find Time Coincidences Between Singles Events w/ Δt
- “Coincident Event” = Pair of Singles Events

Energy Validation



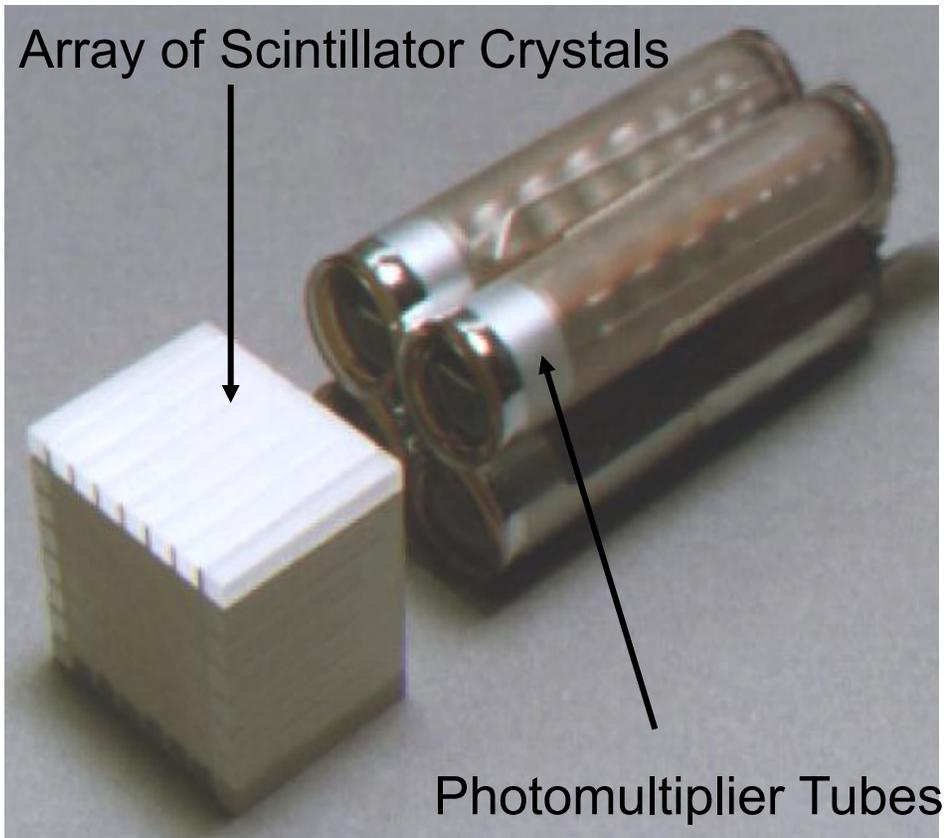
Identifying Time Coincidences



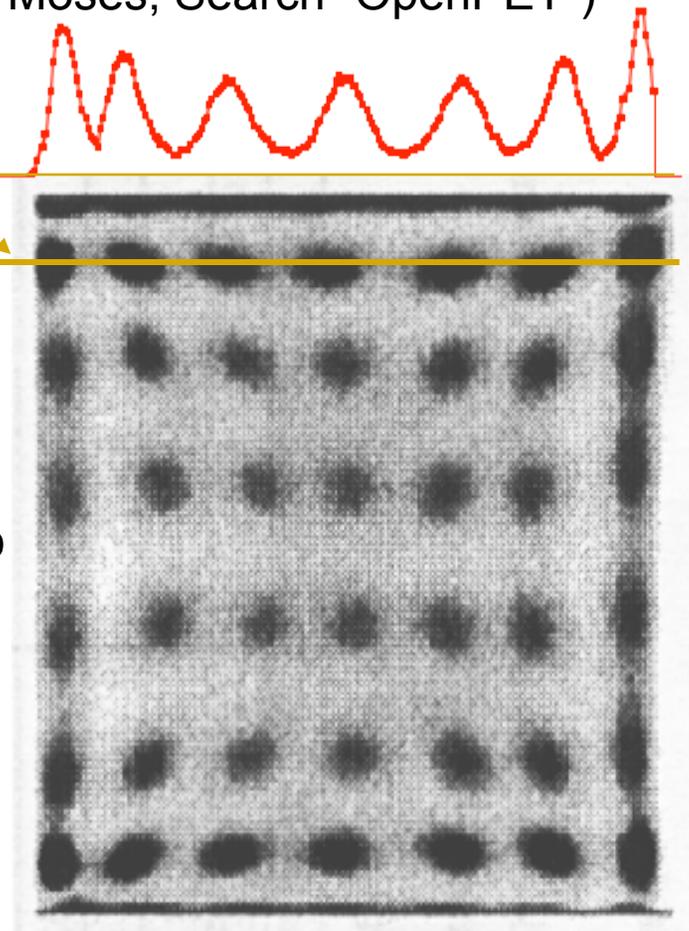
- Break Time Into Slices (100–250 ns / slice)
- Search for Singles Within Δt_{\max} (4–12 ns) in Each Slice

PET Detector Module

(From Talk by Bill Moses, Search "OpenPET")



Profile
through
Row 2

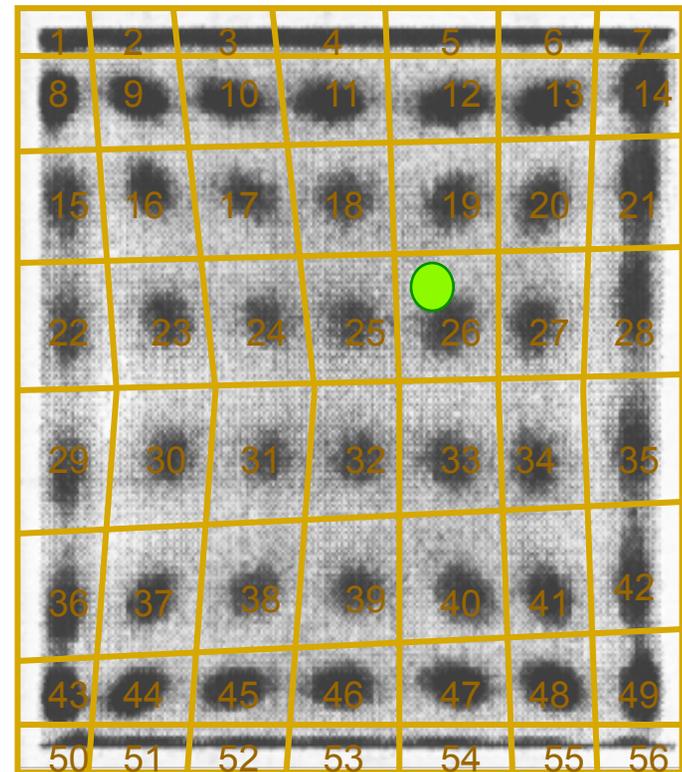


Decode Crystals Using Anger Logic (Light Sharing)

Position Identification

(From Talk by Bill Moses, Search "OpenPET")

1	2	3	4	5	6	7	
8	A		11	1	B		14
15	A		13	1	B		21
22	23	24	25	26	27	28	
29	30	31	32	33	34	35	
36	C		30	4	D		41
43	C		45	4	D		49
50	51	52	53	54	55	56	



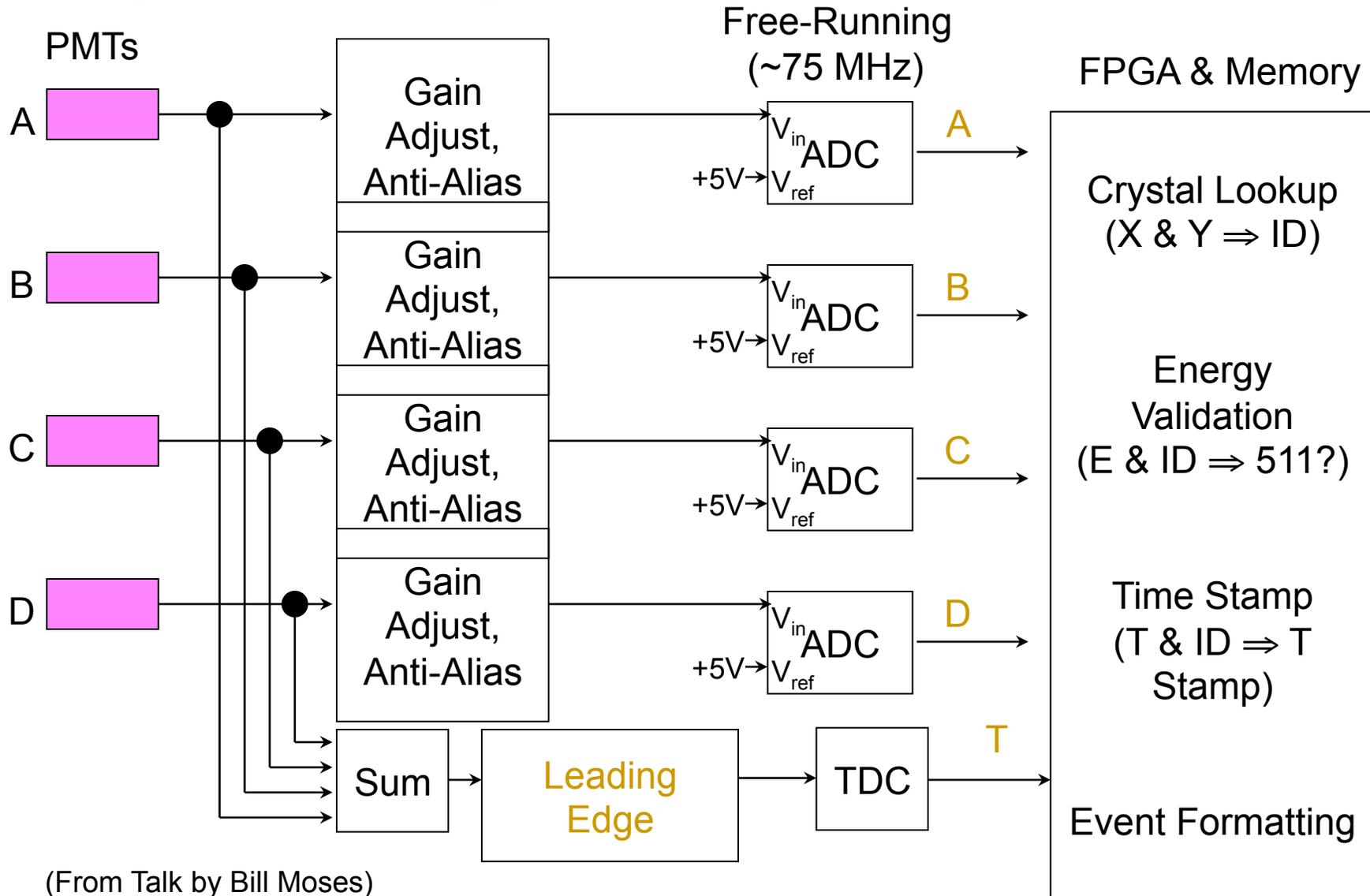
$$E=A+B+C+D$$

$$Y=(A+B)/E$$

$$X=(B+D)/E$$

- Identify Crystal of Interaction Using Lookup Table
- Position Given by Crystal ID

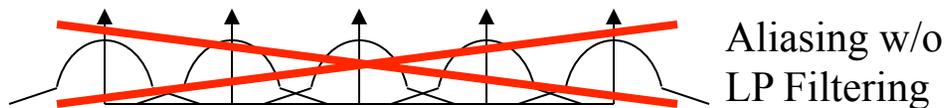
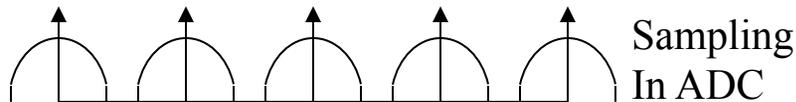
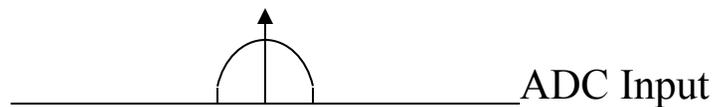
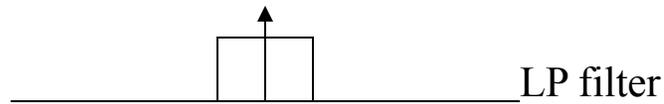
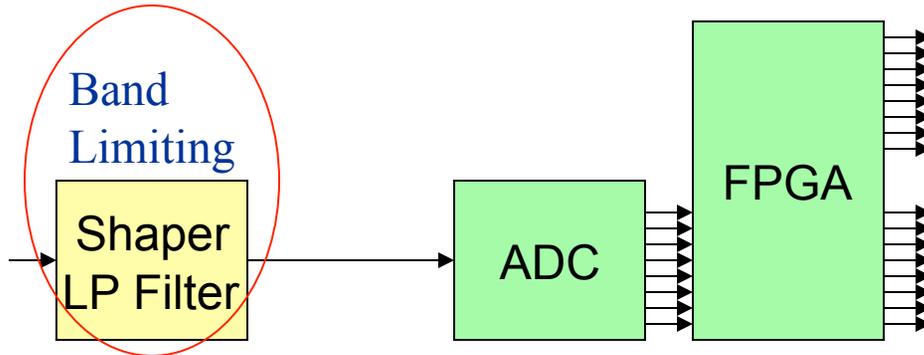
OpenPET Implementation (~2010)



(From Talk by Bill Moses)

Before ADC

Cares Must Be Taken **Outside** FPGA (1)

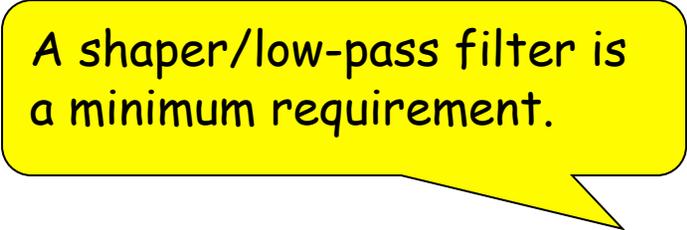


Nyquist Frequency < (1/2) Sampling Frequency

The “Trend” vs. The Sampling Theorem



There will be no hardware analog processing.
Everything is done digitally in software.



A shaper/low-pass filter is a minimum requirement.

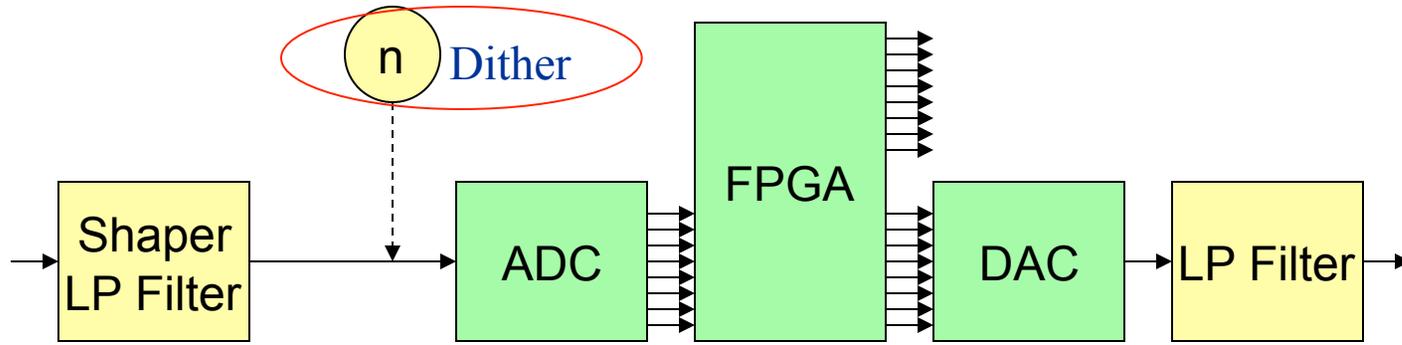


It sounds very stylish 😊

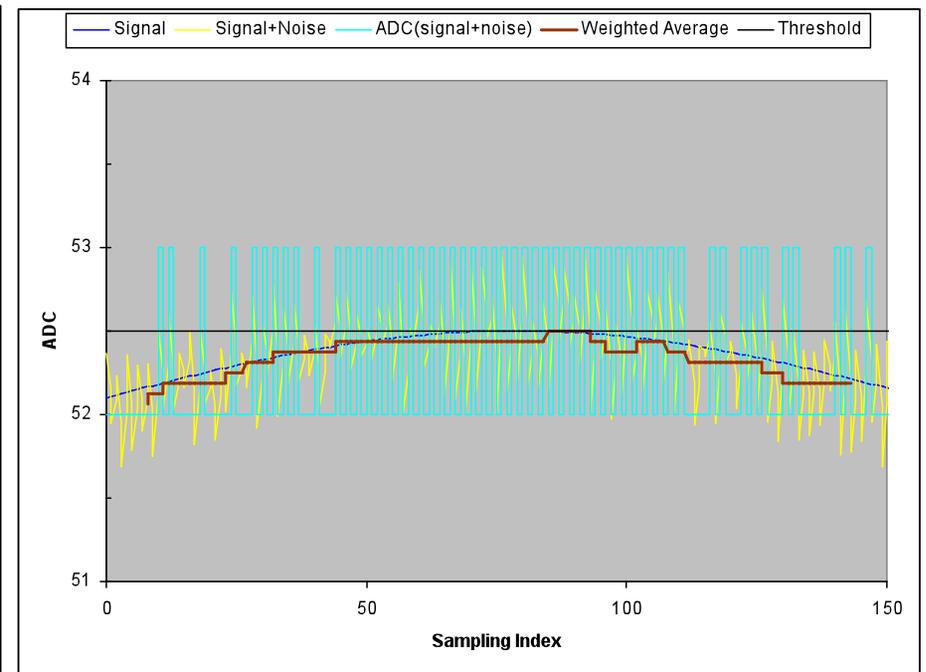
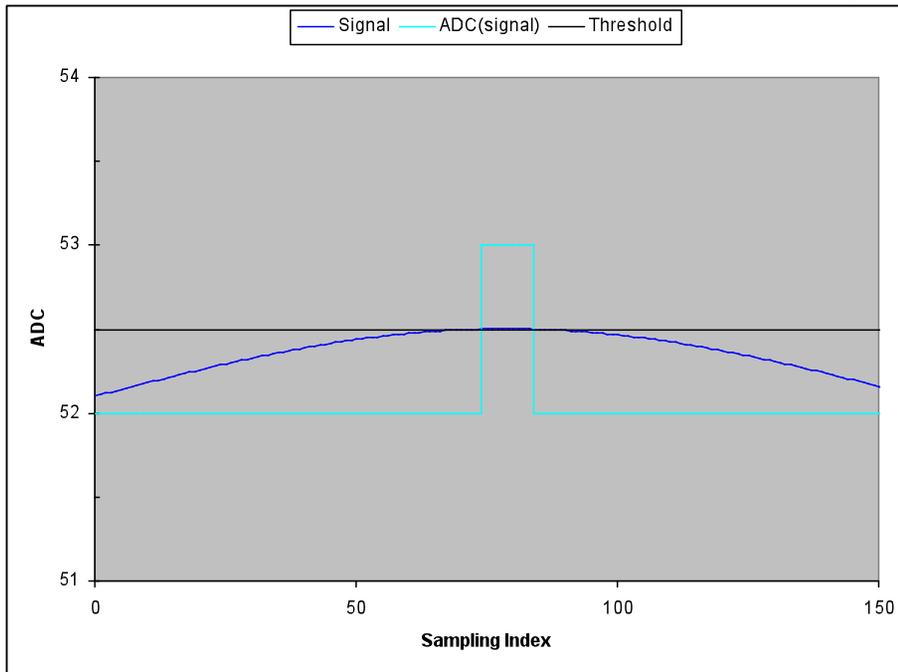
Sampling Theorem!

- 采样定律！
- Sampling Theorem!
- Teorema De Amostragem!
- Abtast Theorem!
- Theorie d'Echantillonnage!
- Samplings Teorem!
- ...
- Follow the sampling theorem strictly!

Cares Must Be Taken Outside FPGA (2)



Resolution finer than the ADC LSB can be achieved by adding noise at ADC input and digital filtering.



Adding Noise for Finer Resolution



Photo Credit: www.telegraph.co.uk, trinities.org

- Mechanical pressure gauges usually do not track small pressure changes well.
- The gauge readers may lightly tap the gauges to get more accurate reading.
- The idea of dithering at ADC input is similar.

Why Band Limiting & Dithering are Ignored?

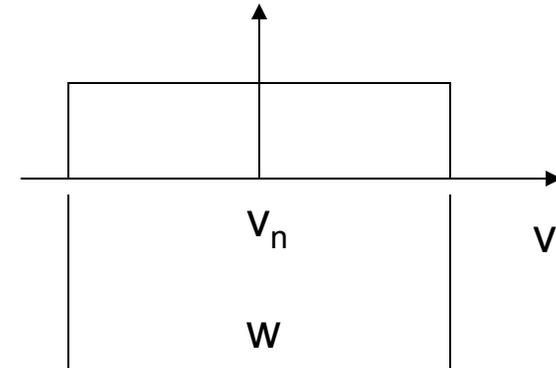
- Pre-amplifiers usually have a naturally limited bandwidth and an intrinsic noise larger than the LSB of the ADC.
- So a lot of time, band limiting and dithering can be “safely” ignored since they are satisfied automatically.
- High bandwidth, low noise devices now become easily accessible. 😊 A design can be too fast and too quiet. 😞
- **Do not forget to review the band limiting and dithering requirements for each design.**

Descriptions of Resolution

Bin Width

$$\sigma = \frac{1}{\sqrt{12}} w$$

(If the distribution within the bin is uniform)

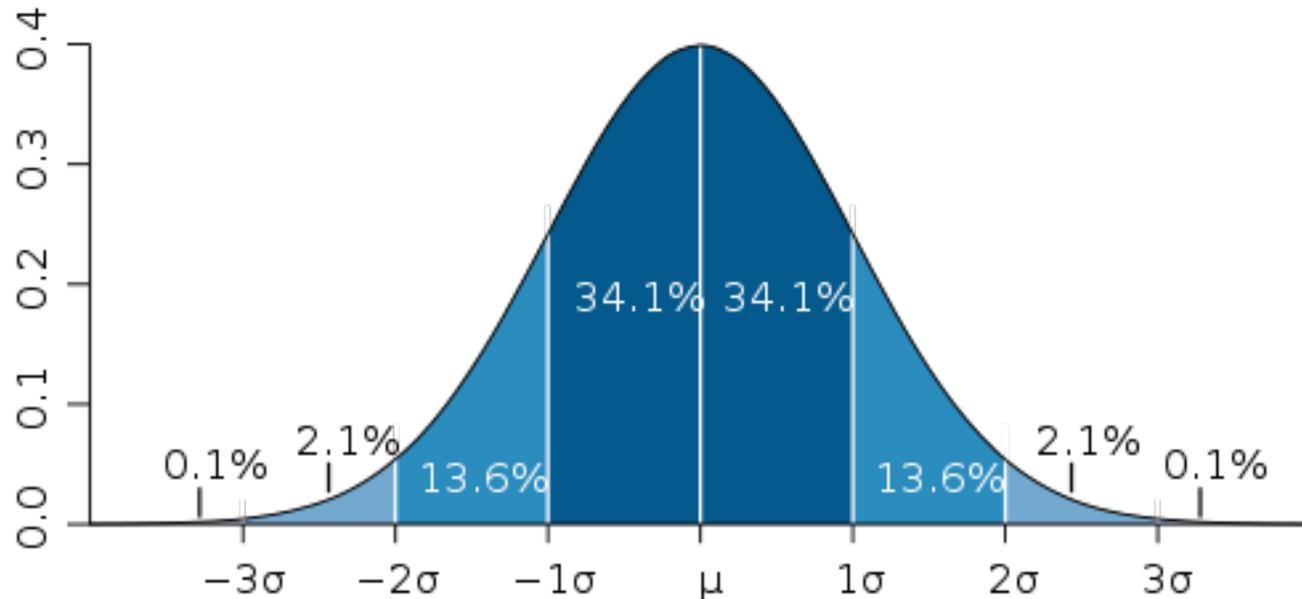


- When the input signal value v to an ADC is within $(v_n - w/2, v_n + w/2)$, the ADC outputs an integer n , representing that the input value is approximately v_n .
- The bin width is a description of measurement errors, or measurement resolution.
- The bin width = (full range)/2^(number of bits):
 - 8 bits: $w = (\text{full range})/256$.
 - 9 bits: $w = (\text{full range})/512$.
 - 10 bits: $w = (\text{full range})/1024$.

Standard Deviation

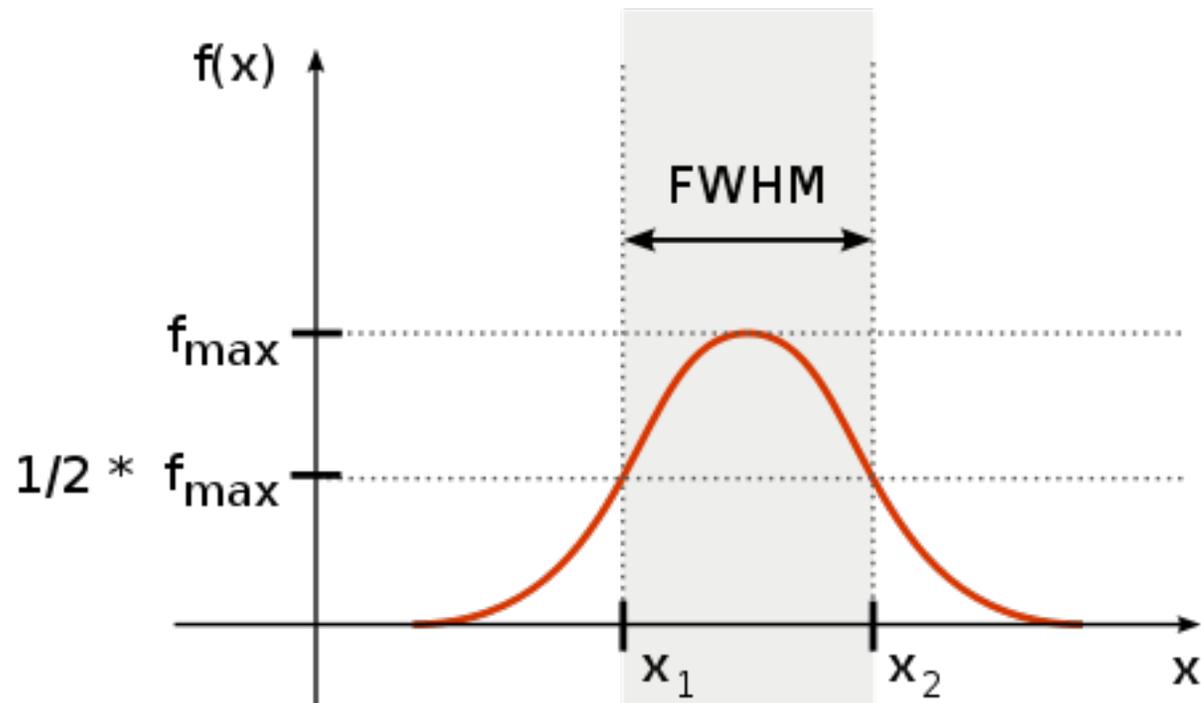
$$\sigma = \sqrt{\frac{1}{N} \sum_{i=1}^N (x_i - \mu)^2} \quad \mu = \frac{1}{N} \sum_{i=1}^N x_i$$

$$f(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}$$



Ref: <http://en.wikipedia.org/>

Full Width at Half Maximum (FWHM)



$$\text{FWHM} = 2.35482\sigma$$

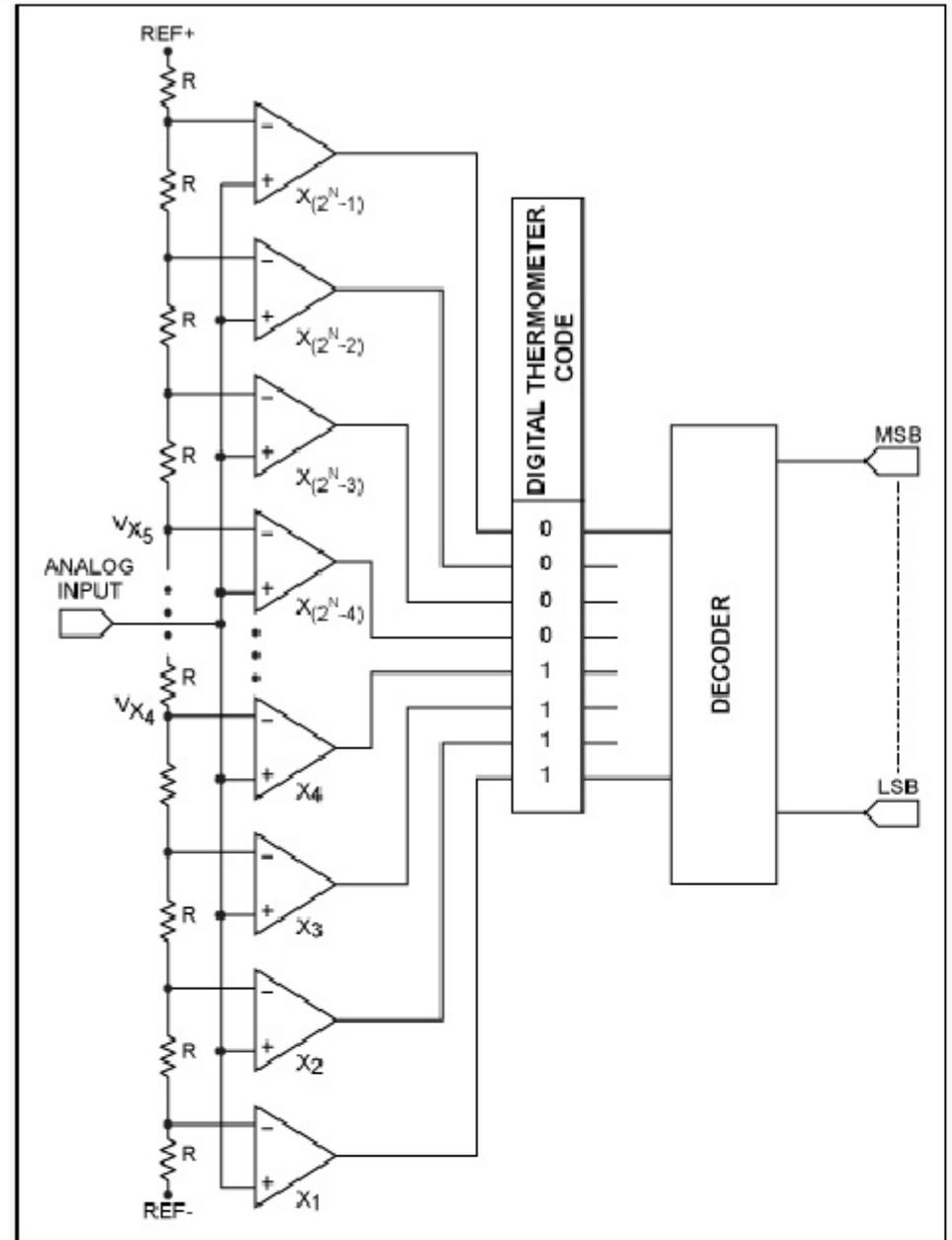
(For Gaussian distribution)

Commercial ADC

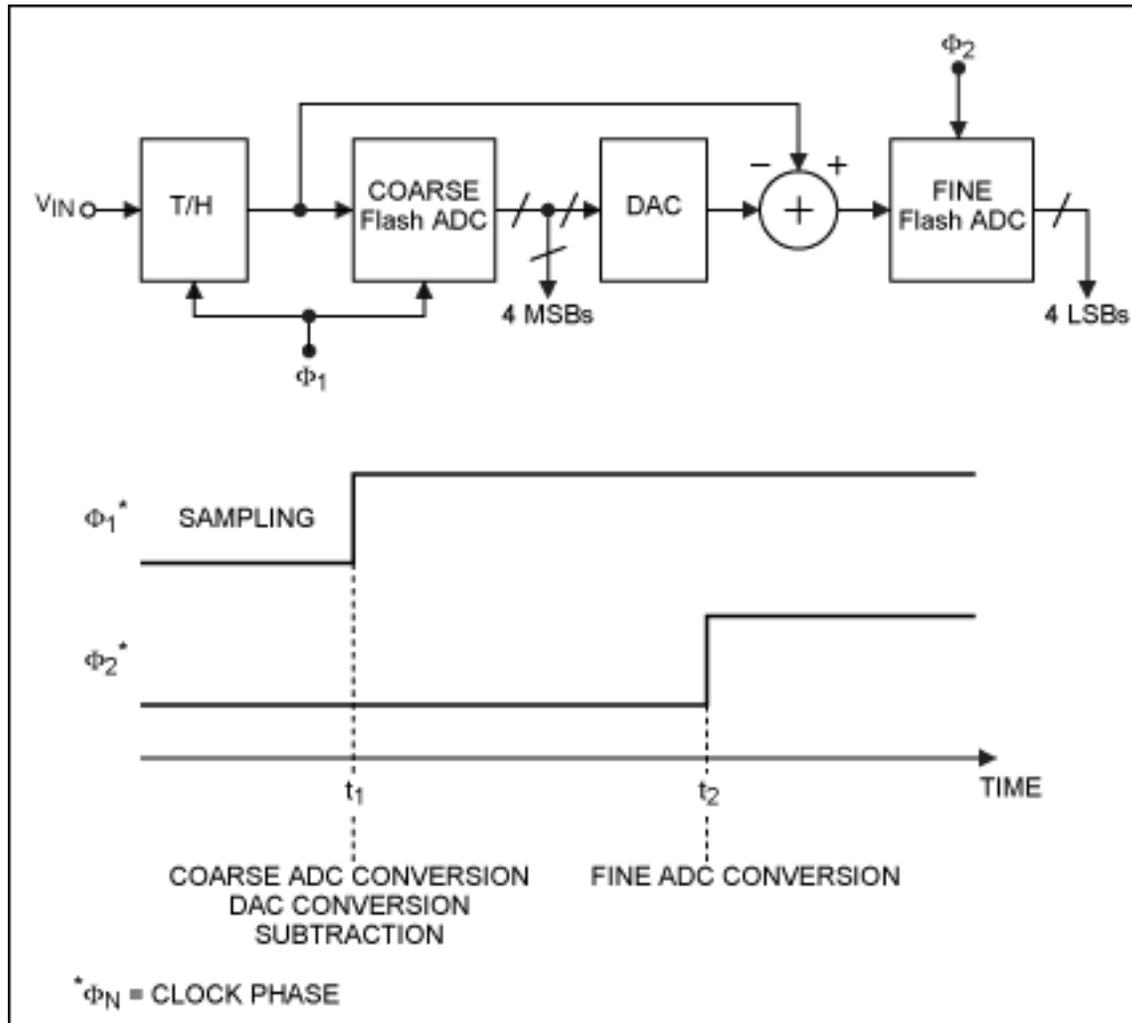
The Flash ADC

8 bits: 256 Comparators
9 bits: 512 Comparators
10 bits: 1024 Comparators
...

Ref: <http://www.scribd.com/doc/50291058/Flash-ADC-tutorial>



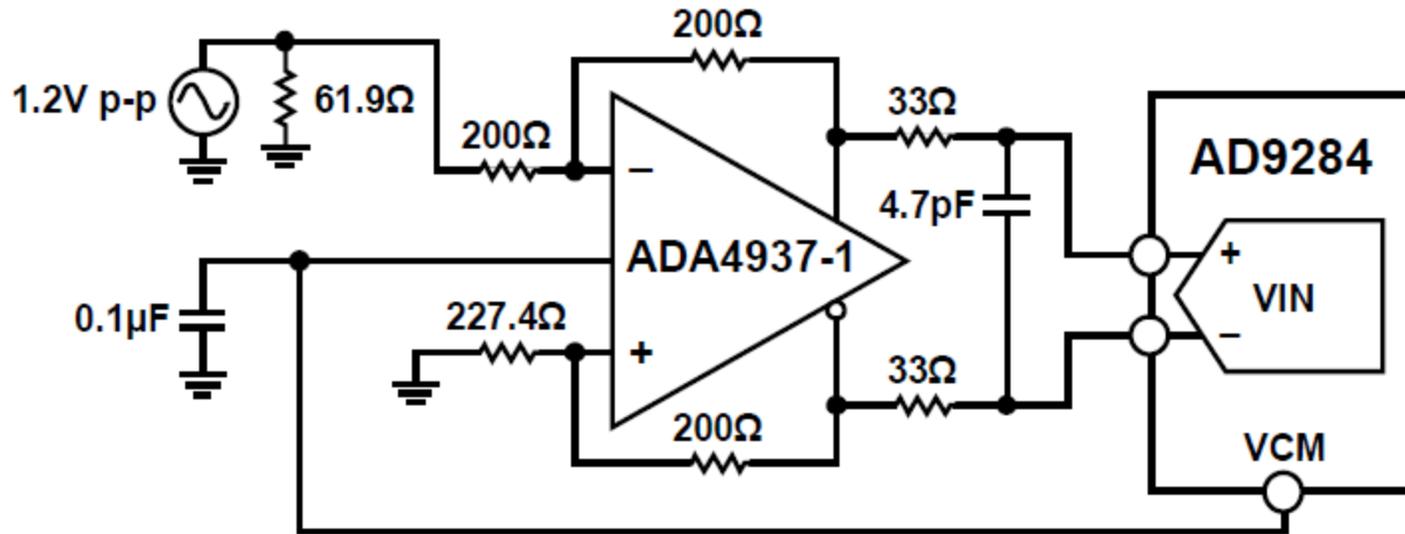
The Pipeline ADC



8 bits = 4 bits + 4 bits
16 + 16 comparators

Ref: <http://www.maxim-ic.com/app-notes/index.mvp/id/810>

Typical Circuit of ADC Applications



Ref: <http://www.analog.com/>

TDC Implemented in ASIC

Traditional TDC Implemented in ASIC

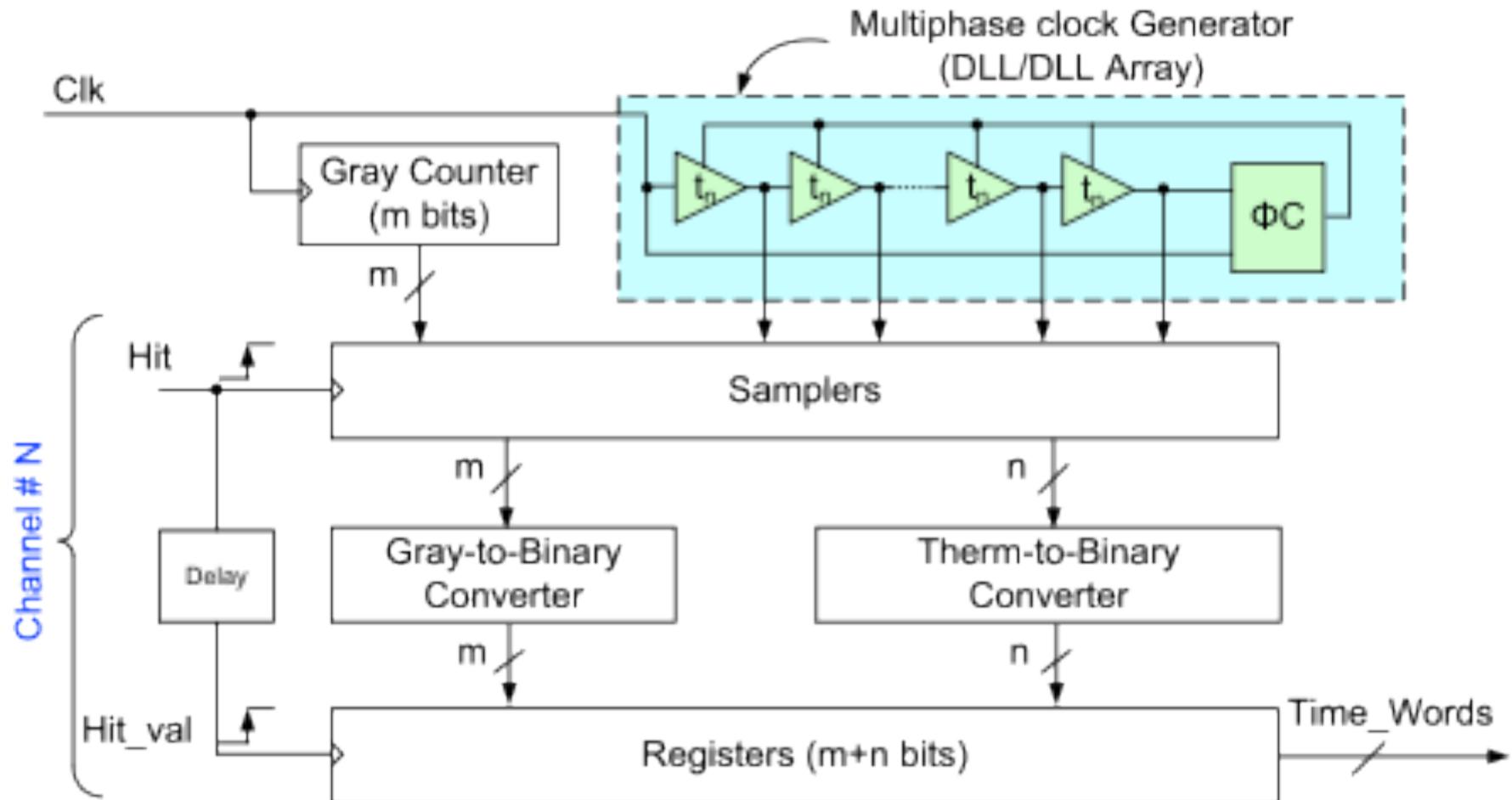
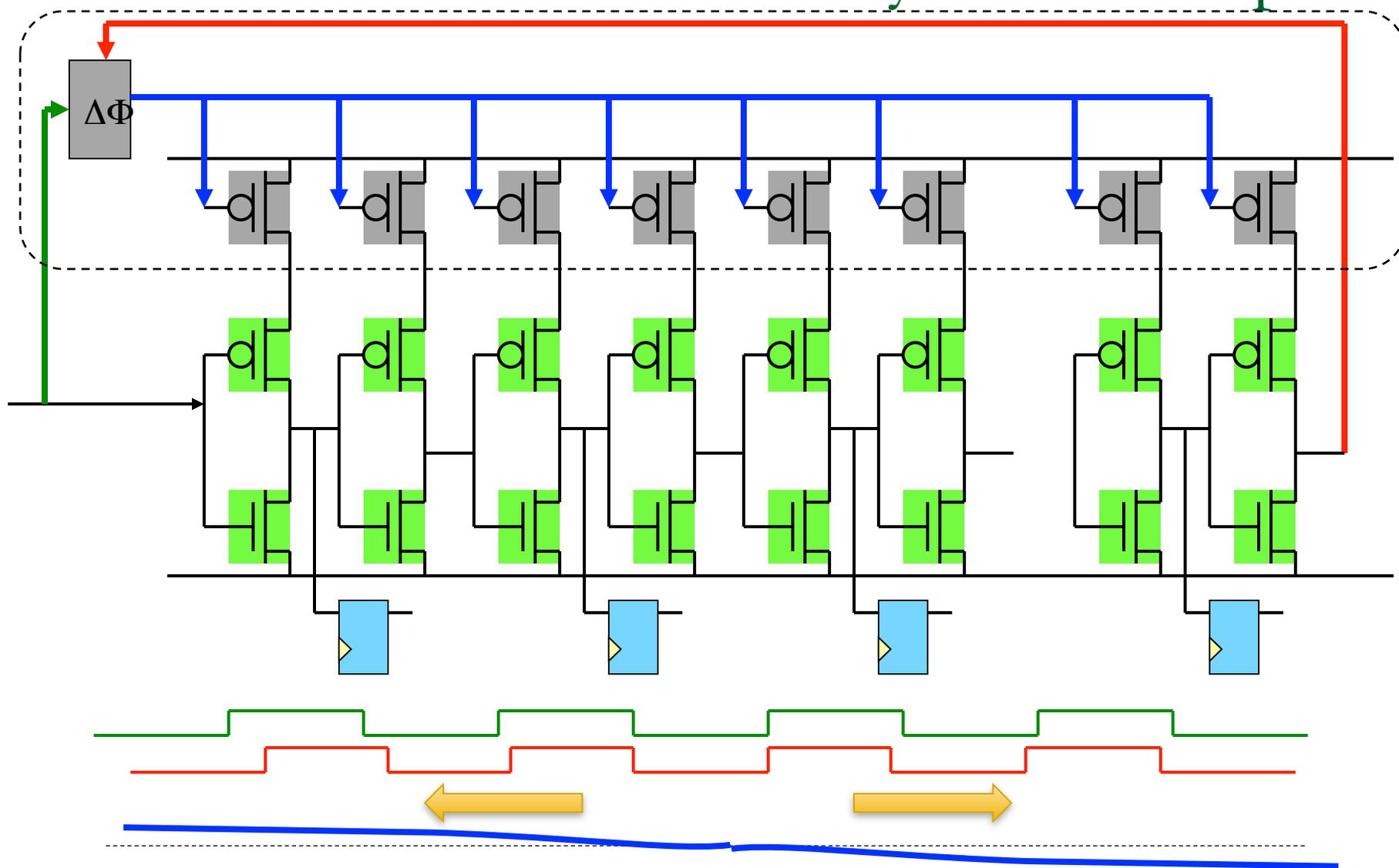


Figure 1: Traditional architecture of a flash TDC.

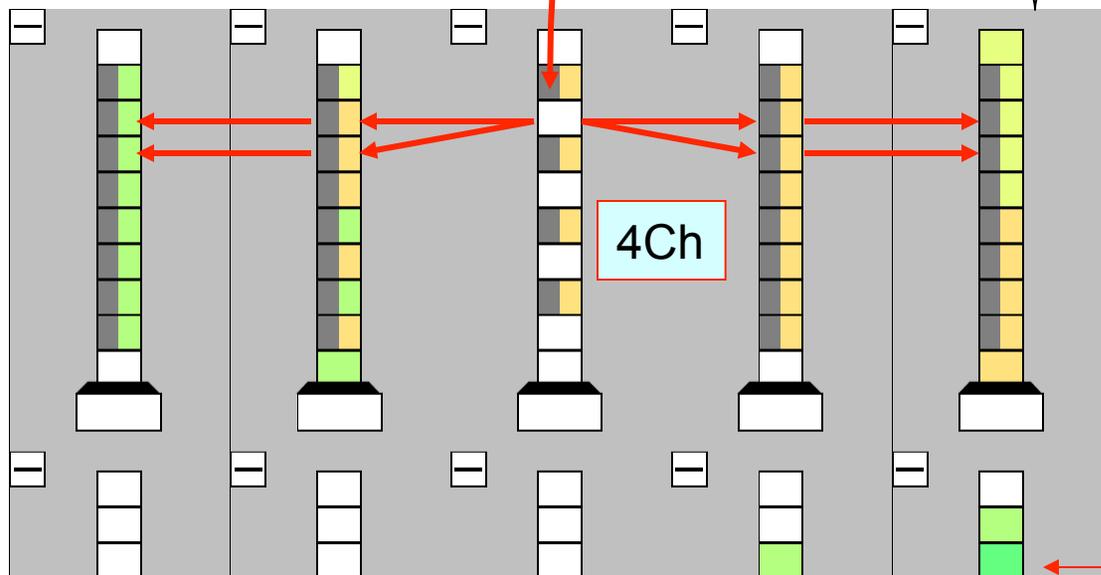
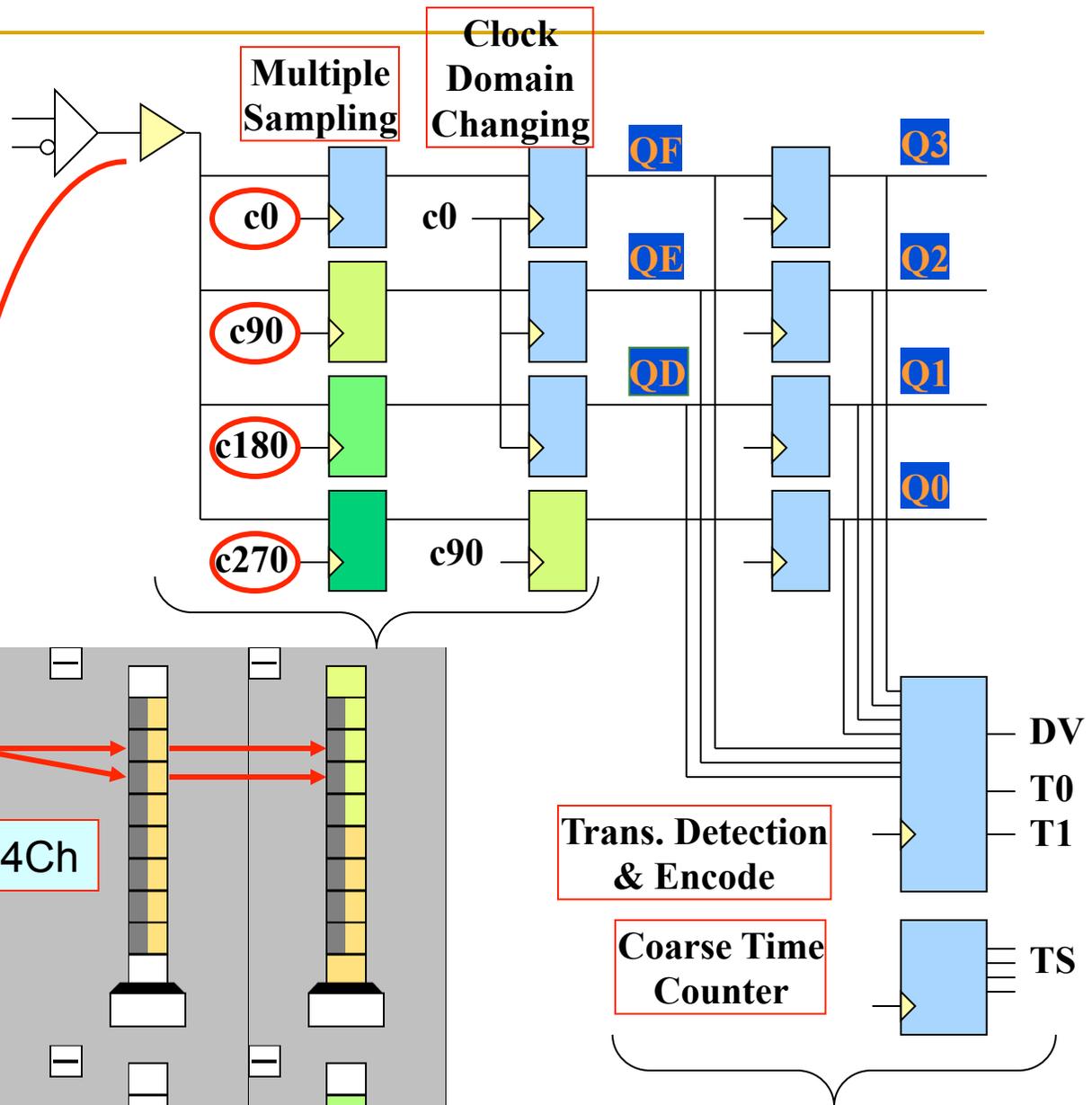
Phase Detection and Delay Lock Loop



TDC Implemented with FPGA

Multi-Sampling TDC FPGA

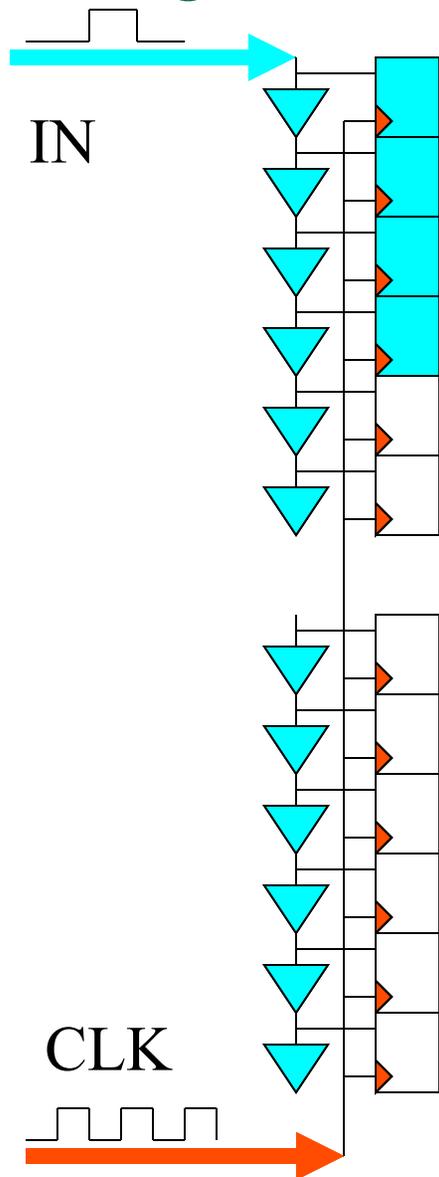
- Ultra low-cost: 48 channels in \$18.27 EP2C5Q208C7.
- Sampling rate: 360 MHz x4 phases = 1.44 GHz.
- LSB = 0.69 ns.



This picture represent a placement in Cyclone FPGA

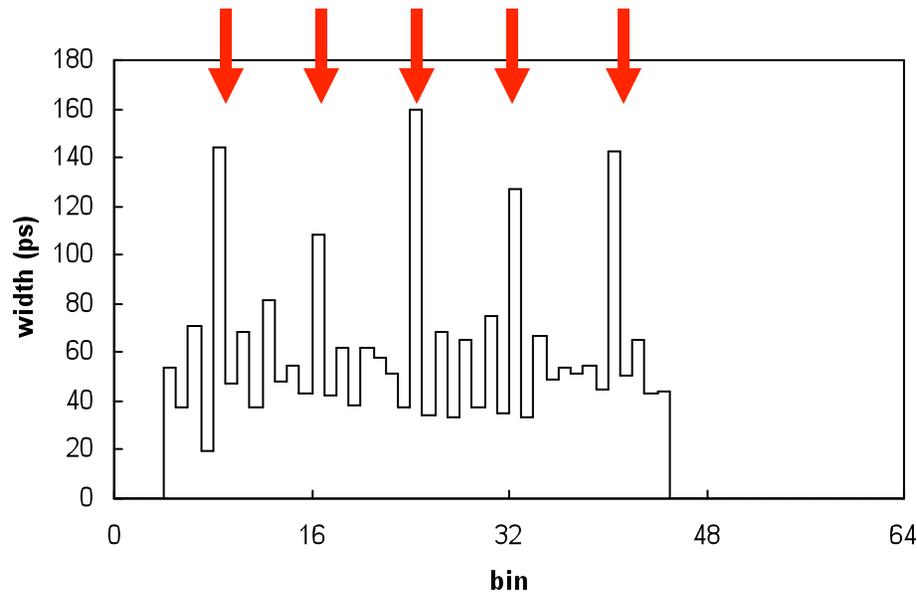
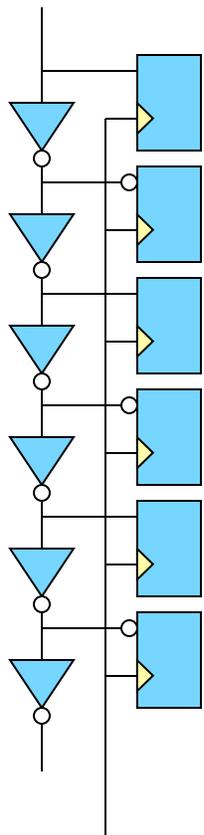
Logic elements with non-critical timing are freely placed by the fitter of the compiler.

TDC Using FPGA Logic Chain Delay

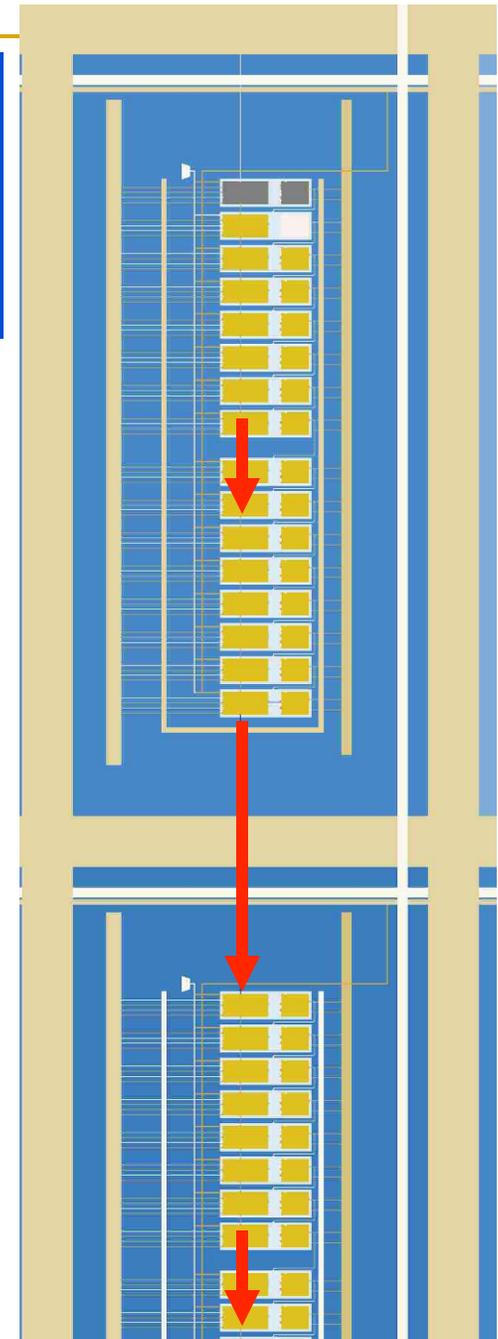


- This scheme uses current FPGA technology ☺
- Low cost chip family can be used. (e.g. EP2C8T144C6 \$31.68) ☺
- Fine TDC precision can be implemented in slow devices (e.g., 20 ps in a 400 MHz chip). ☺

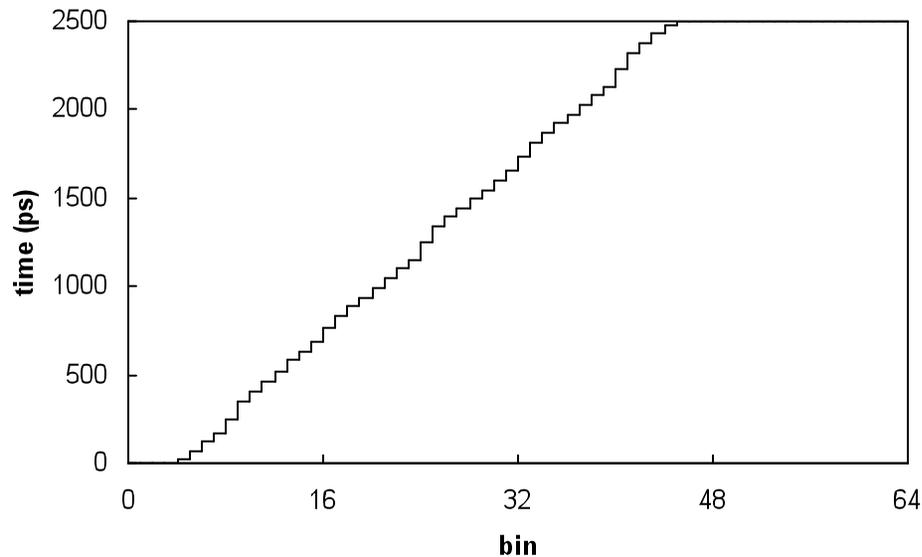
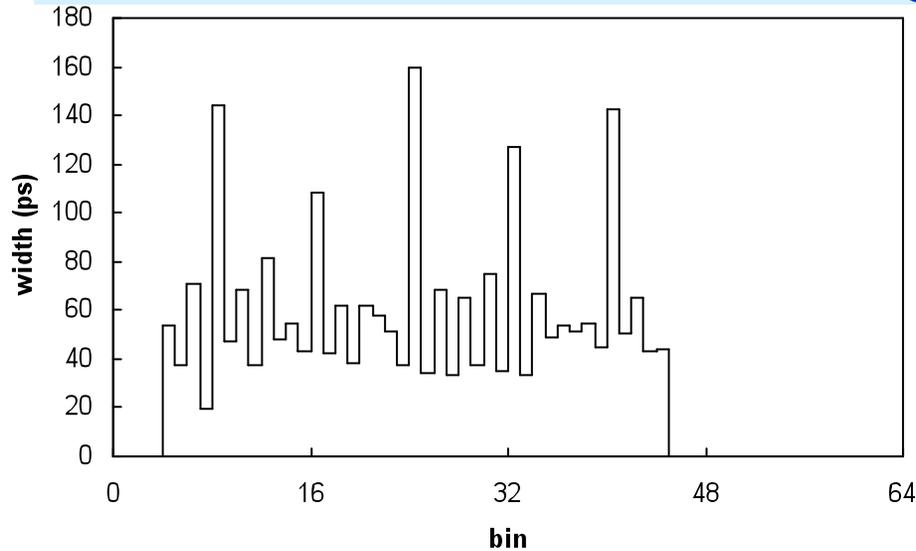
Two Major Issues Due To Differential Non-Linearity



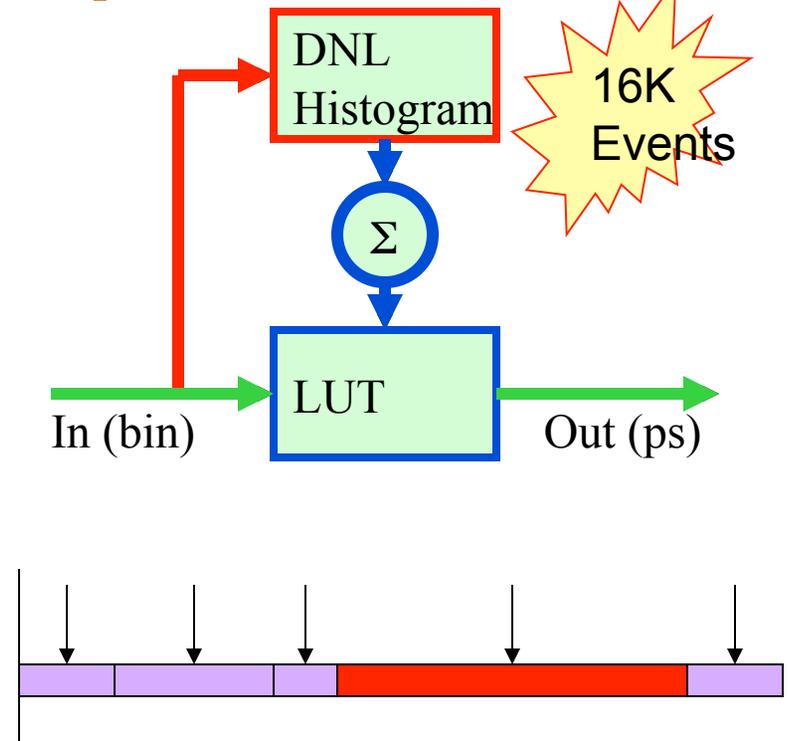
1. Widths of bins are different and varies with supply voltage and temperature.
2. Some bins are ultra-wide due to LAB boundary crossing



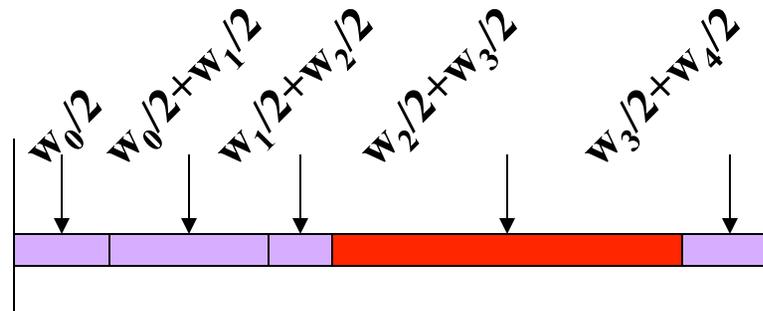
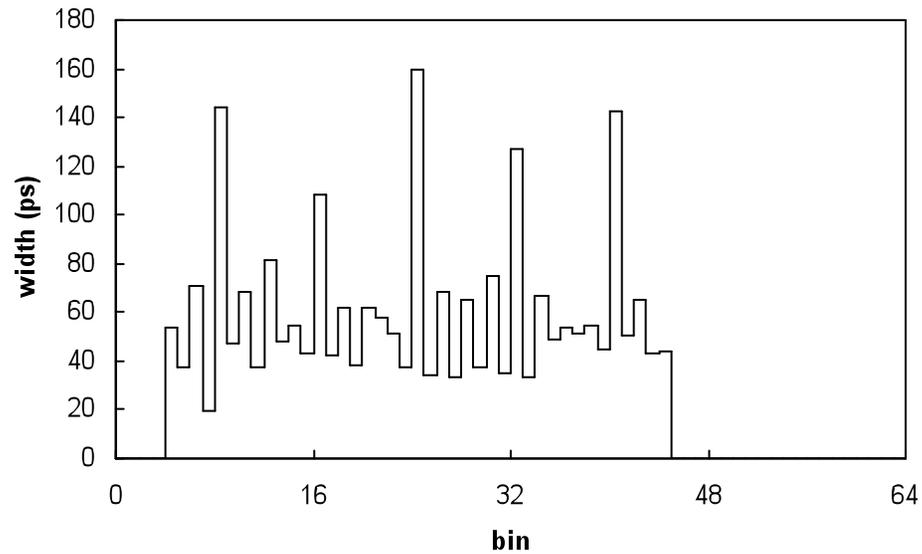
Auto Calibration Using Histogram Method



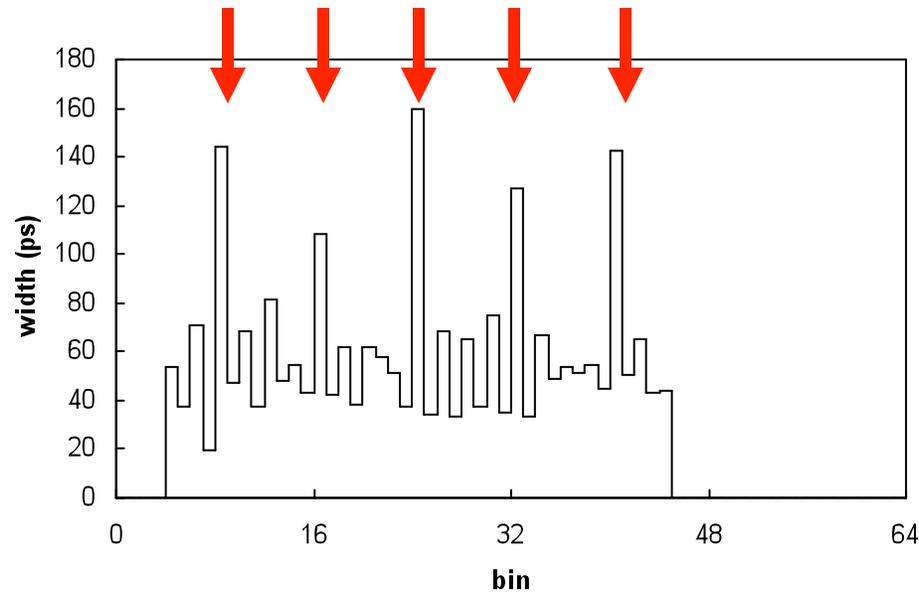
- Turn-key solution (bin in, ps out)
- Semi-continuous (auto update LUT every 16K events)
- Calibrates both DNL and temperature.



Calibration to the Center of Bins

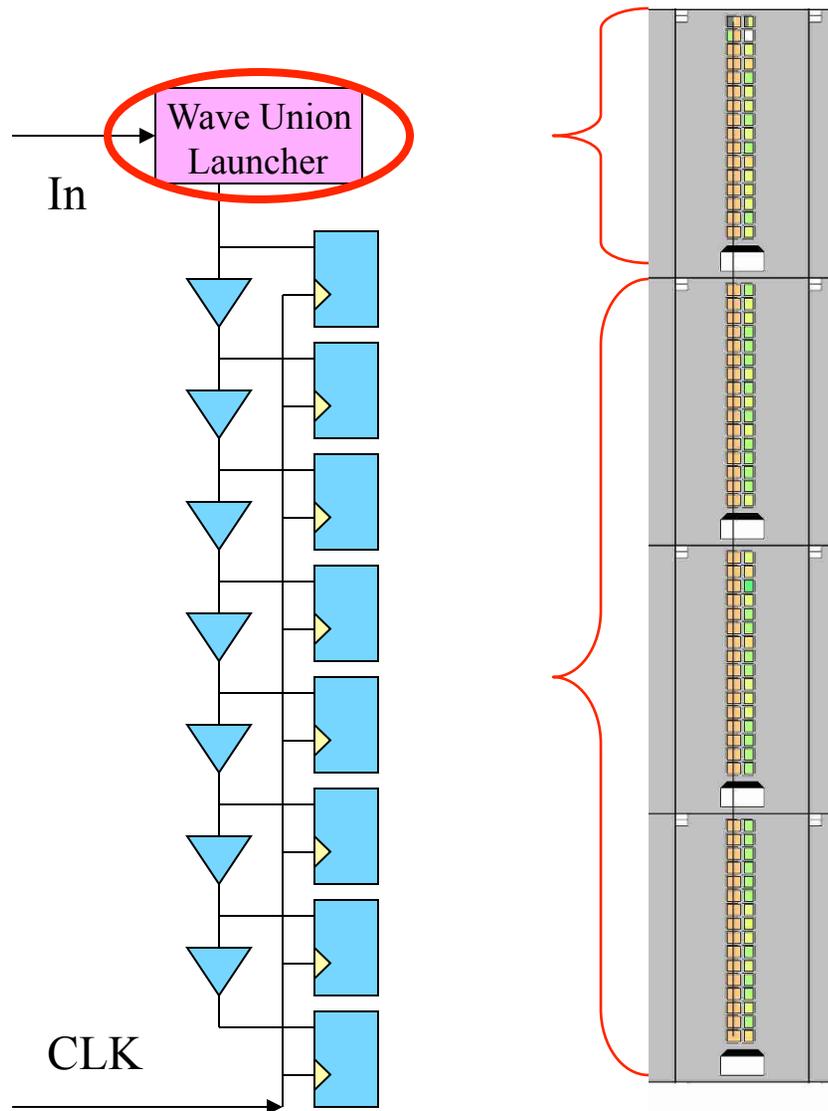


Good, However



- Auto calibration solved some problems 😊
- However, it won't eliminate the ultra-wide bins 😞

Cell Delay-Based TDC + Wave Union Launcher



The wave union launcher creates multiple logic transitions after receiving a input logic step.

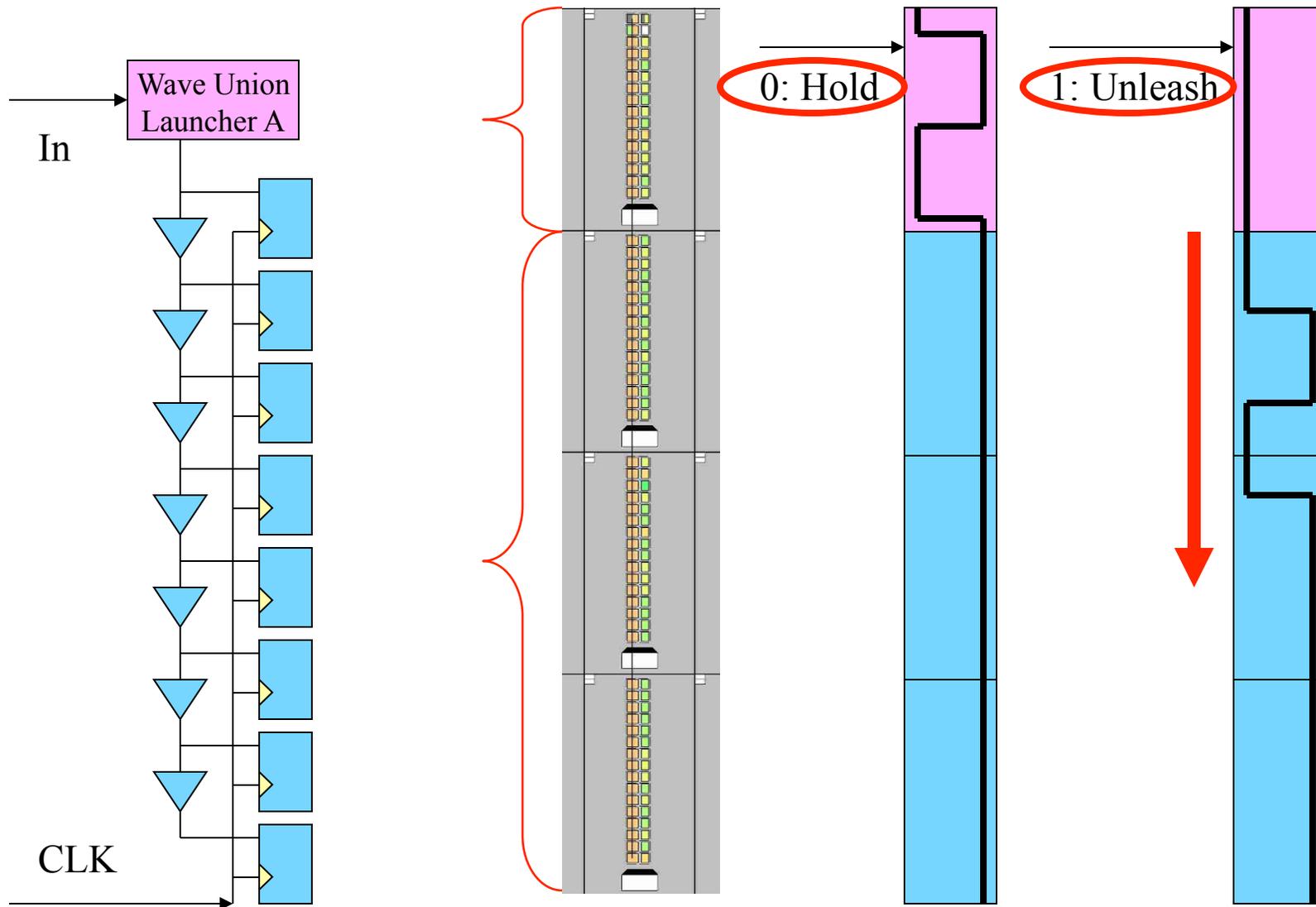
The wave union launchers can be classified into two types:

- Finite Step Response (FSR)
- Infinite Step Response (ISR)

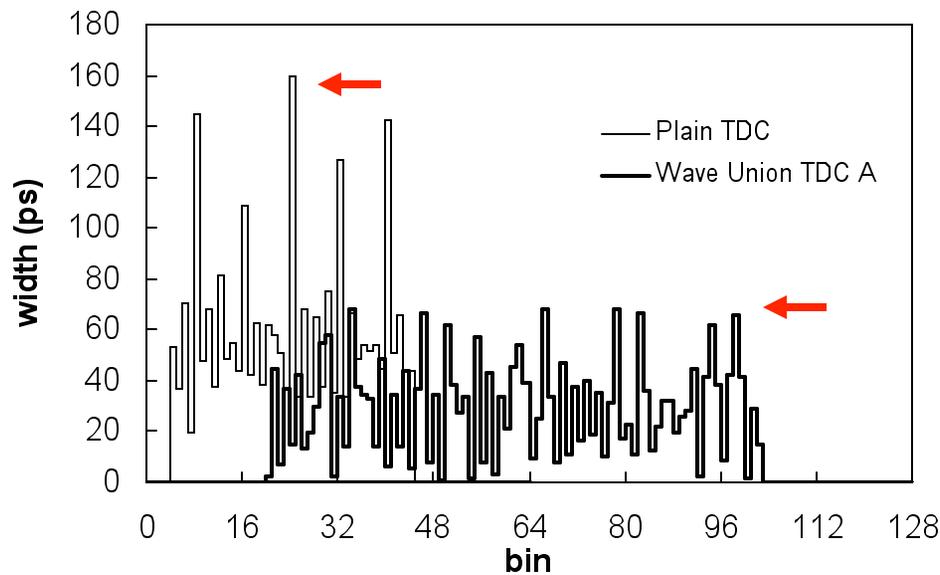
This is similar as filter or other linear system classifications:

- Finite Impulse Response (FIR)
- Infinite Impulse Response (IIR)

Wave Union Launcher A (FSR Type)



Sub-dividing Ultra-wide Bins



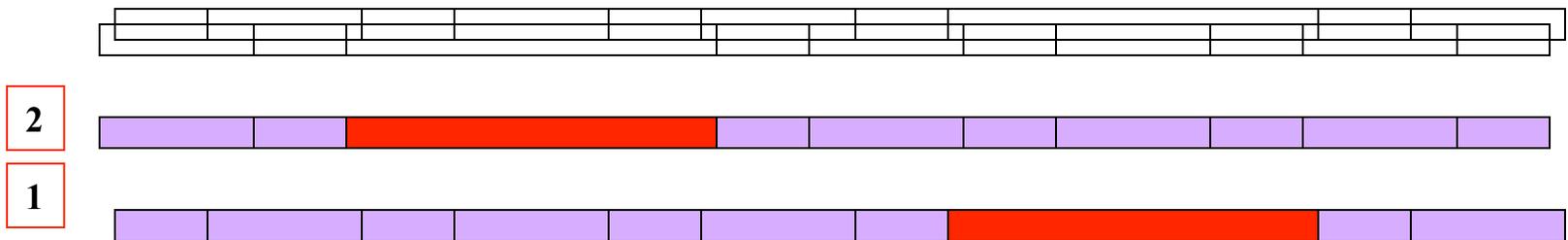
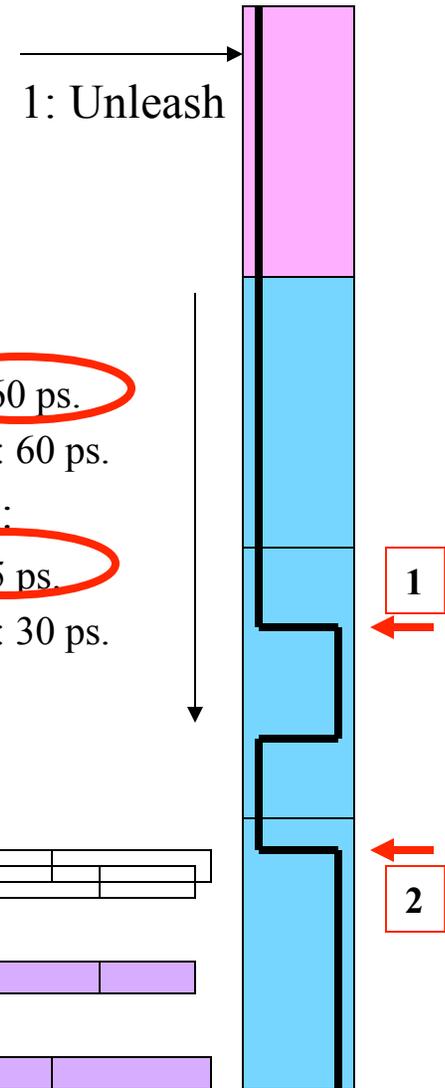
Device: EP2C8T144C6

■ Plain TDC:

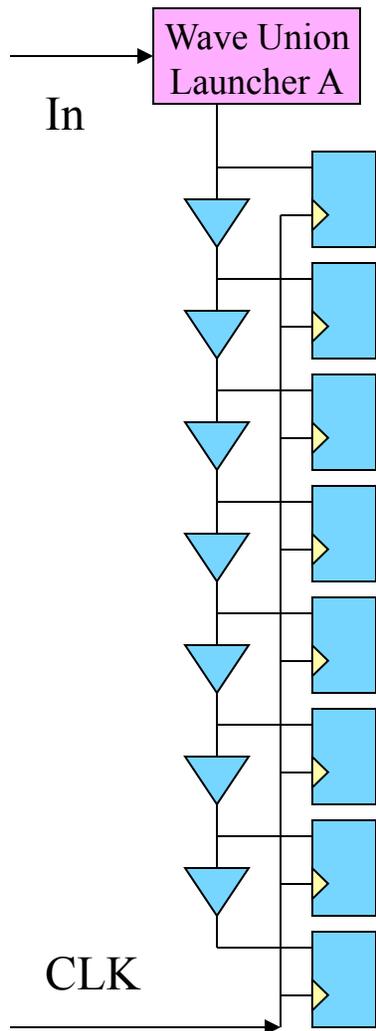
- Max. bin width: 160 ps.
- Average bin width: 60 ps.

■ Wave Union TDC A:

- Max. bin width: 65 ps.
- Average bin width: 30 ps.



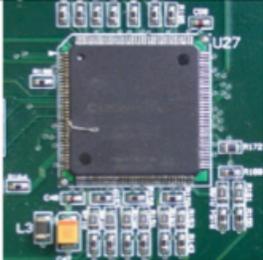
FPGA TDC



**18-Channel
Wave Union TDC on FPGA
WUTDC09a**

Features:

- ❑ A Wave Union TDC firmware with 18 channels implemented in an EP2C8T144C6 144-pin FPGA chip for time-of-flight applications.
- ❑ ASIC-like encapsulation to shorten learning curve for users.
- ❑ Two LVDS input banks each hosts 8 regular channels plus 1 channel for common timing reference.
- ❑ Digitizing both rising and falling edges for time-over-threshold (TOT) measurements or rising edge only for high-rate applications.
- ❑ On-chip histogram-based automatic bin-by-bin calibration for non-linearity correction and temperature compensation or optional raw data output without calibration if elected by users.
- ❑ Time measurement ΔT RMS resolution:
 - 25 ps (Rising edges).
 - 50 ps (Pulse Width).
 - 80 ps (Falling edges).
- ❑ Time measurement range: unlimited.
- ❑ Double hit separation:
 - Rising edge to next falling edge: > 7.5 ns.
 - Falling edge to next rising edge: > 7.5 ns.
- ❑ Continuous digitization with no dead-time nominally.
- ❑ Free running with local crystal or running with distributed system clock.
- ❑ Jam-prevention logic: < 8 hits/CH in each $2.64 \mu\text{s}$ time slice.
- ❑ Un-triggered data output via LVDS differential ports at 193.75 Mbits/s using DC balanced 8B/10B coding.



- ❑ Output capacity for 16 channels in each $5.28 \mu\text{s}$ time frame:
 - 24 hits with 1 output port.
 - 48 hits with 2 output ports.
 - 72 hits with 3 output ports.
 - 96 hits with 4 output ports.
- ❑ Common timing reference channels support:
 - Single pulse (common start/stop) mode.
 - Common burst mode with 2, 4 or 8 pulses and
 - Mean-timing mode.
- ❑ Register-setting-free for most common operations.
- ❑ RS232 serial port for control commands and display of diagnostic information.
- ❑ On-chip time difference histograms and channel hit counters.
- ❑ Data block display captured at the LVDS output ports after 8B/10B encoding.
- ❑ On-chip signals for calibration and operation evaluation.
- ❑ Outputs of selected test signal for debugging.

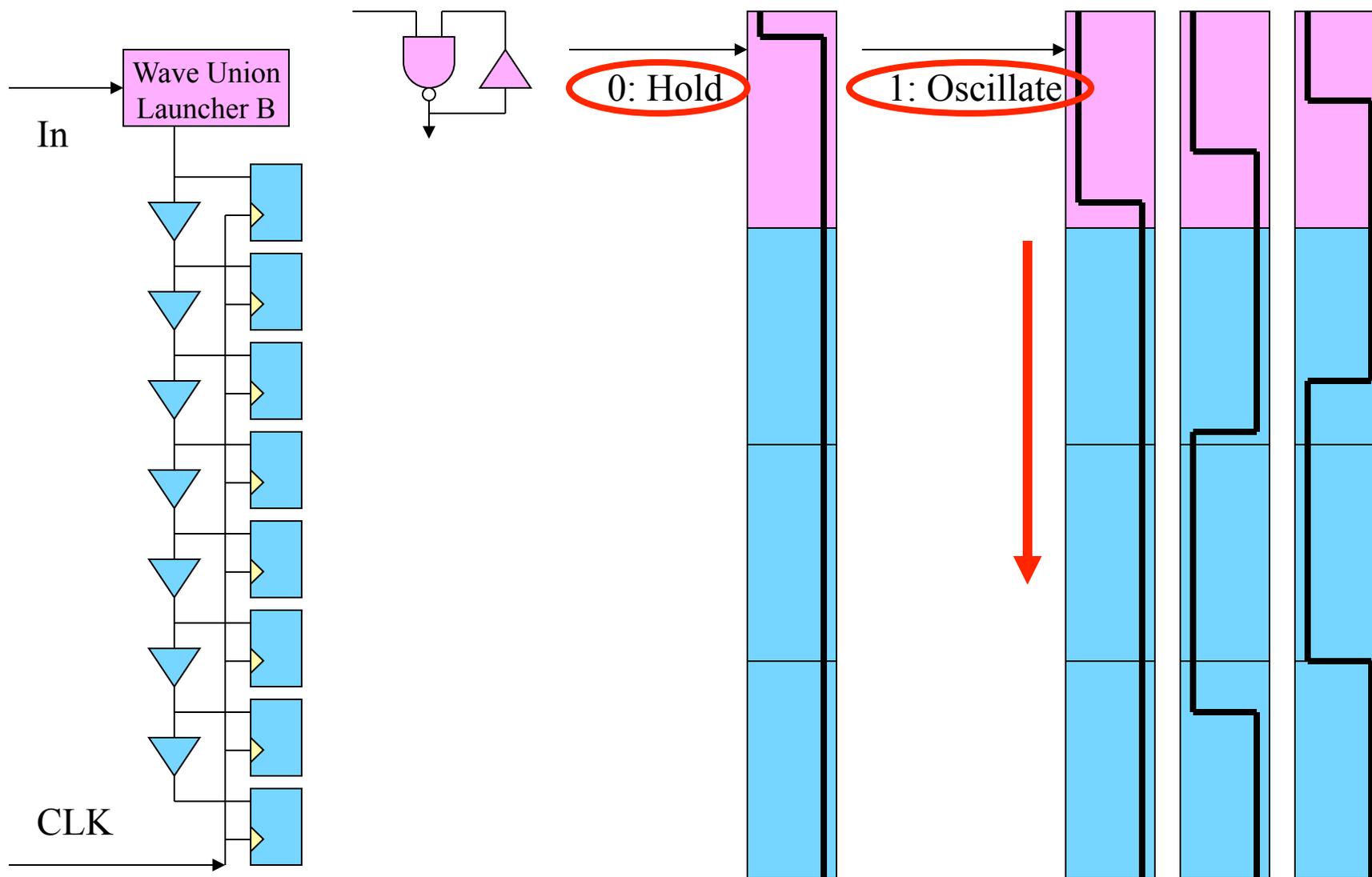
Jinyuan Wu, Fermilab, jywu168@fnal.gov 1

- A possible choice of the TDC can be a delay line based architecture called the Wave Union TDC implemented in FPGA.
- Shown here is an ASIC-like implementation in a 144-pin device.
- 18 Channels (16 regular channels + 2 timing reference channels).
- This FPGA cost \$28, \$1.75/channel. (AD9222: \$5.06/channel)
- LSB ~ 60 ps.
- RMS resolution < 25 ps.
- Power consumption 1.3W, or 81 mW/channel. (AD9222: 90 mW/channel)

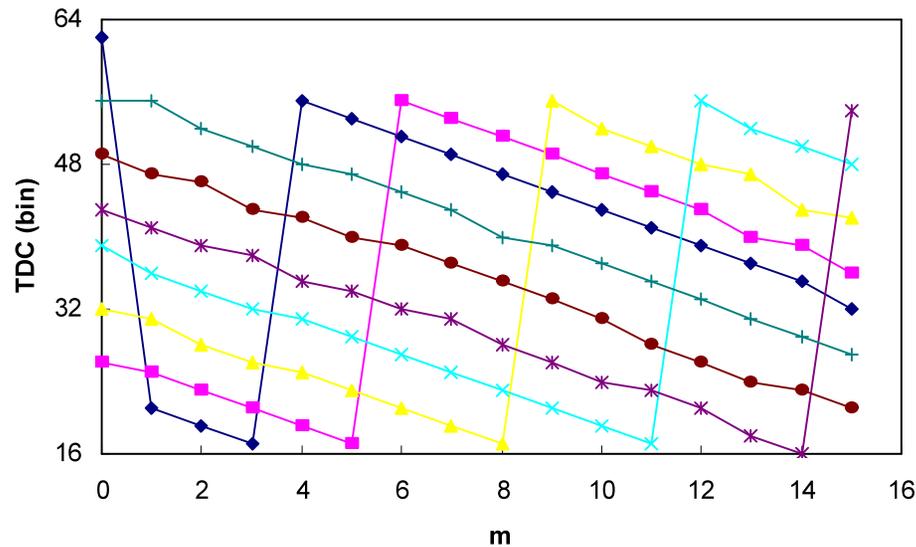
More Measurements

- Two measurements are better than one.
- Let's try 16 measurements?

Wave Union Launcher B (ISR Type)



Delay Correction

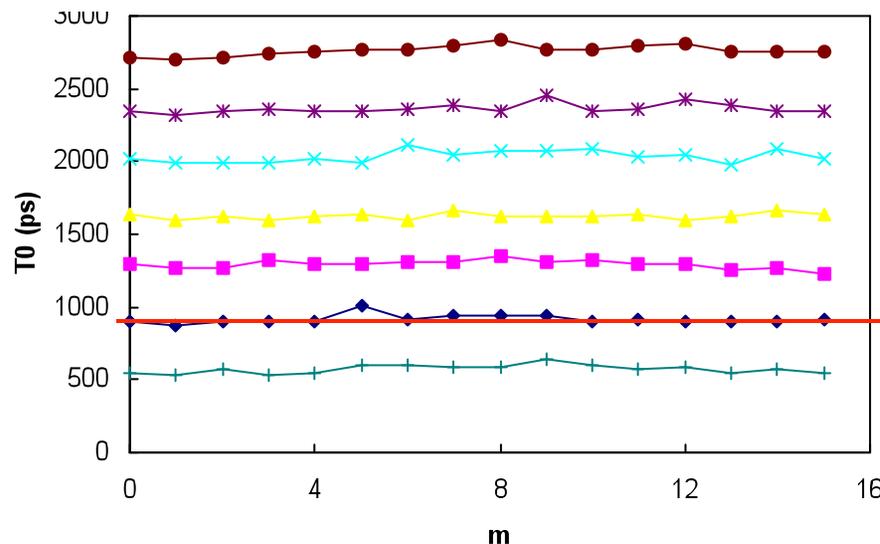


The raw data contains:

- U-Type Jumps: [48-63]→[16-31]
- V-Type Jumps: other small jumps.
- W-Type Jumps: [16-31]→[48-63]

Delay Correction Process:

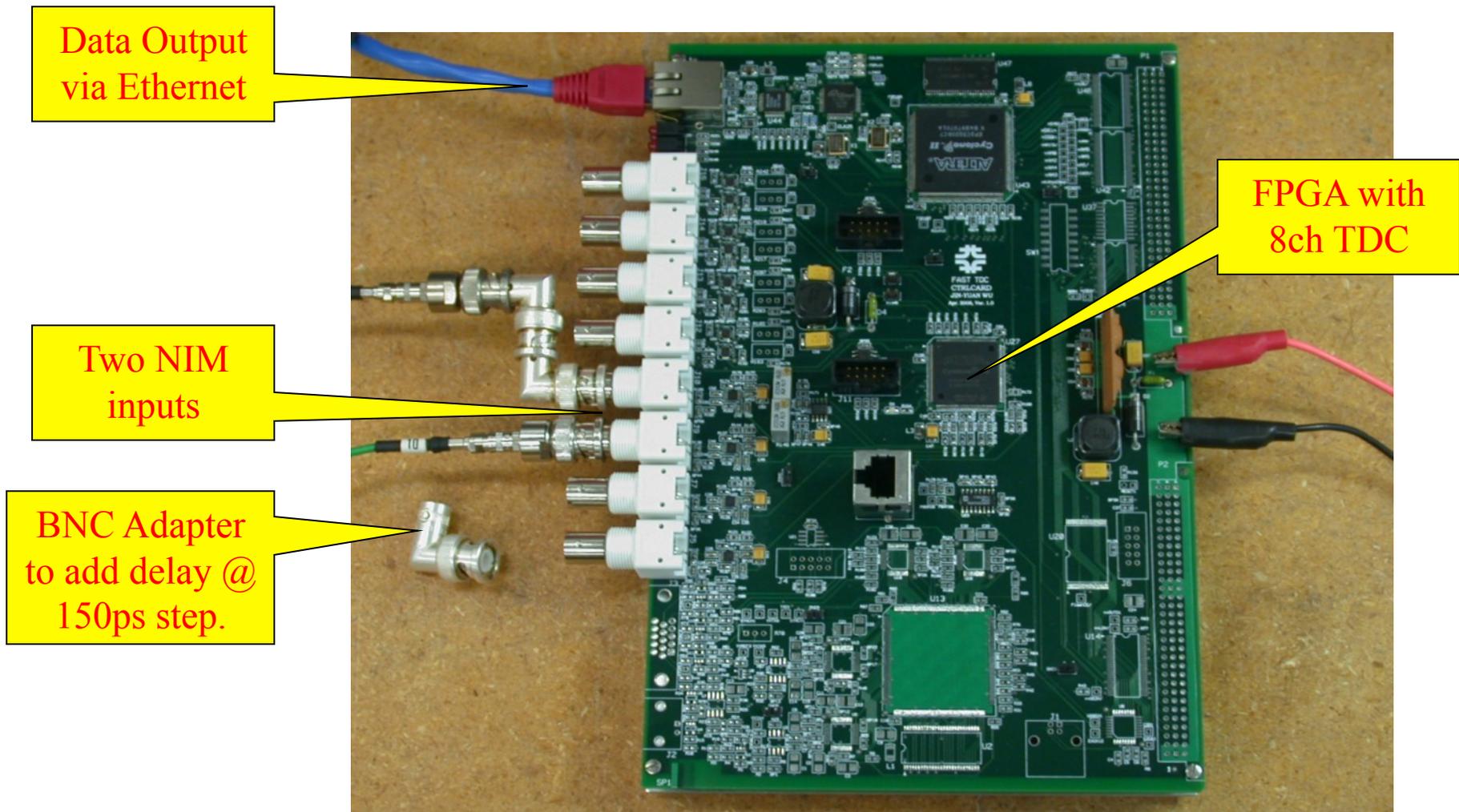
- Raw hits TN(m) in bins are first calibrated into TM(m) in picoseconds.
- Jumps are compensated for in FPGA so that TM(m) become T0(m) which have a same value for each hit.
- Take average of T0(m) to get better resolution.



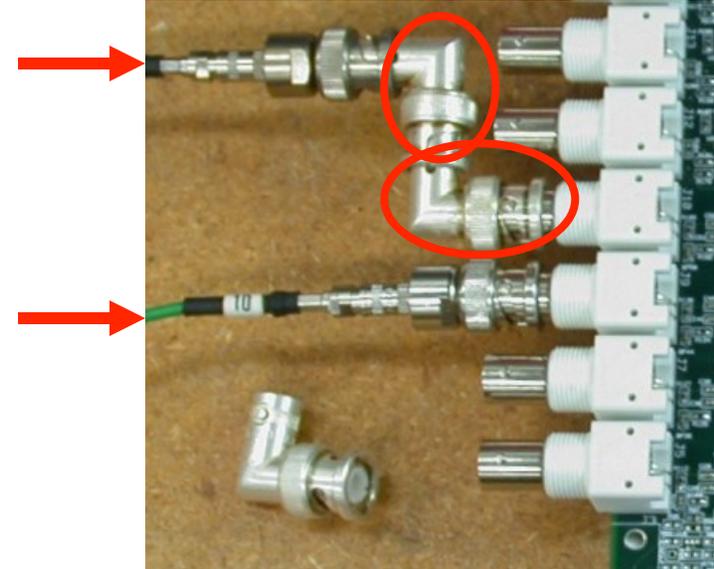
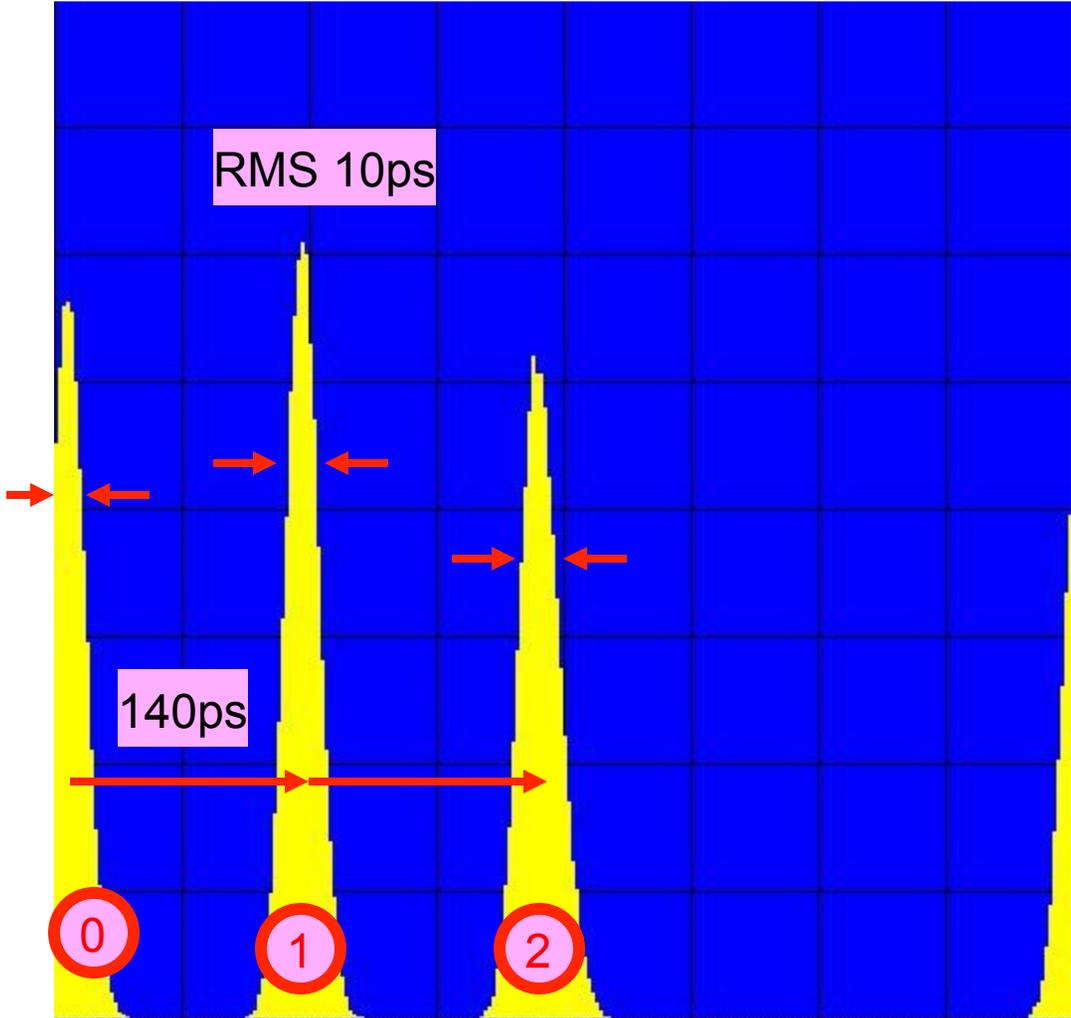
$$t_{0av} = \frac{1}{16} \sum_{m=0}^{15} t_0(m)$$

The processes are all done in FPGA.

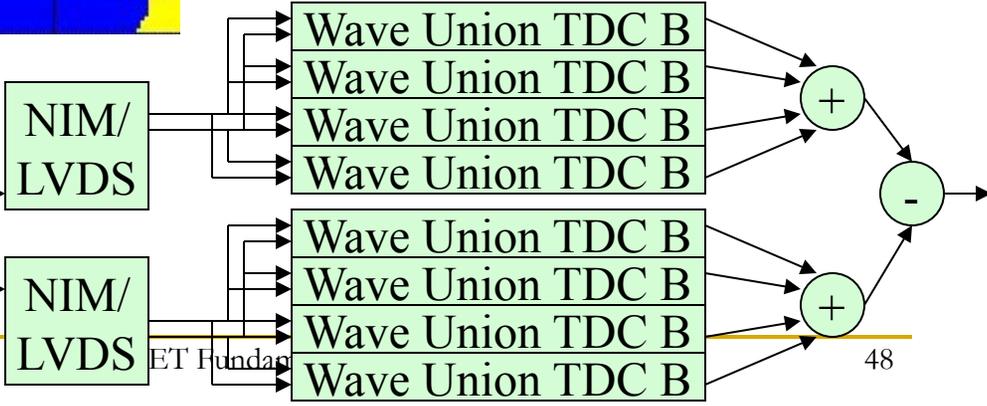
The Test Module



Test Result NIM Inputs



BNC adapters to add delays @ 140ps step.



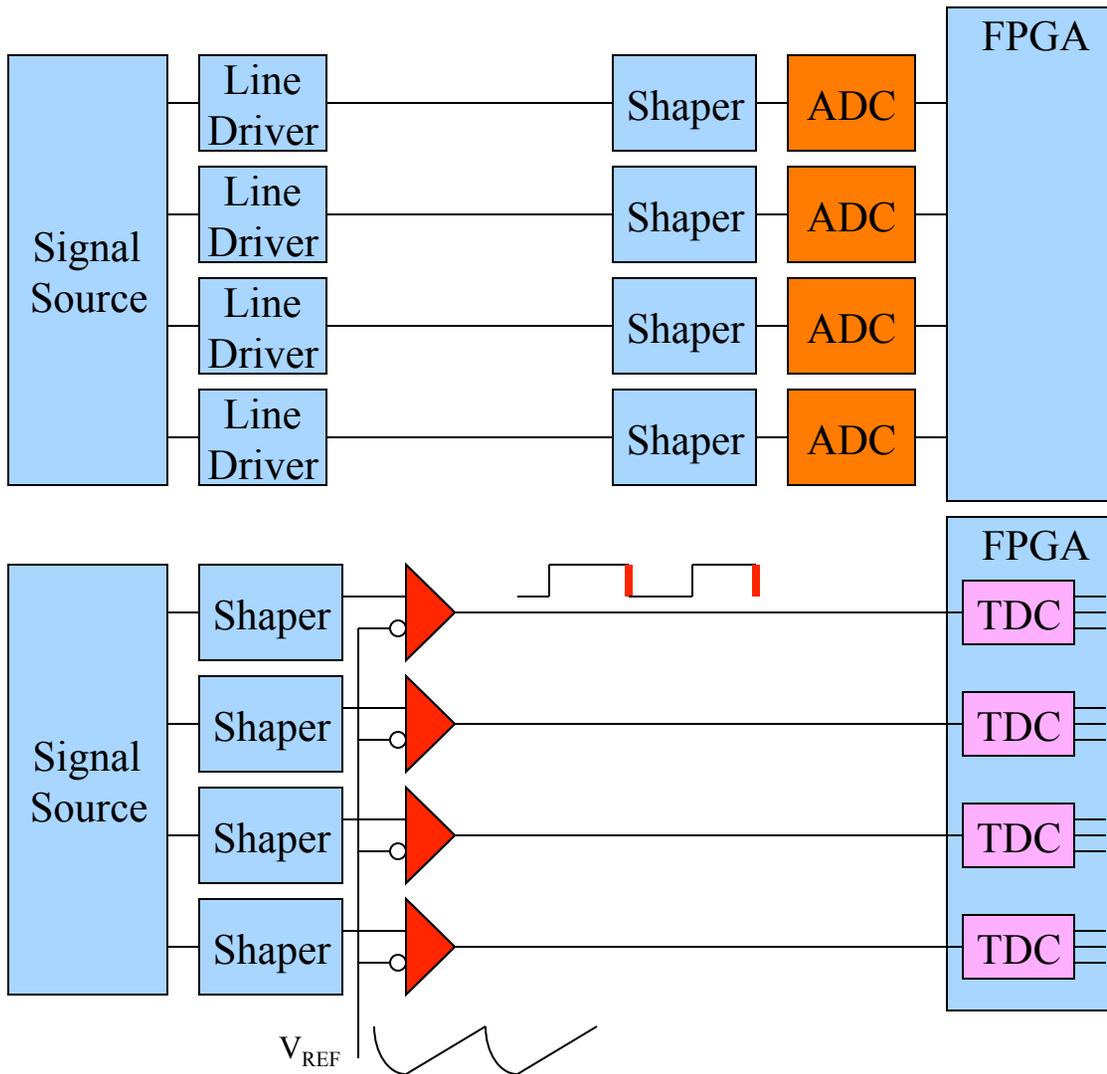
Wave Union?



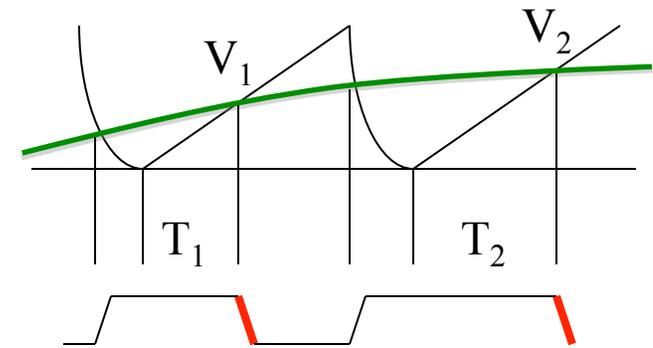
Photograph: Qi Ji, 2010

Using FPGA as ADC

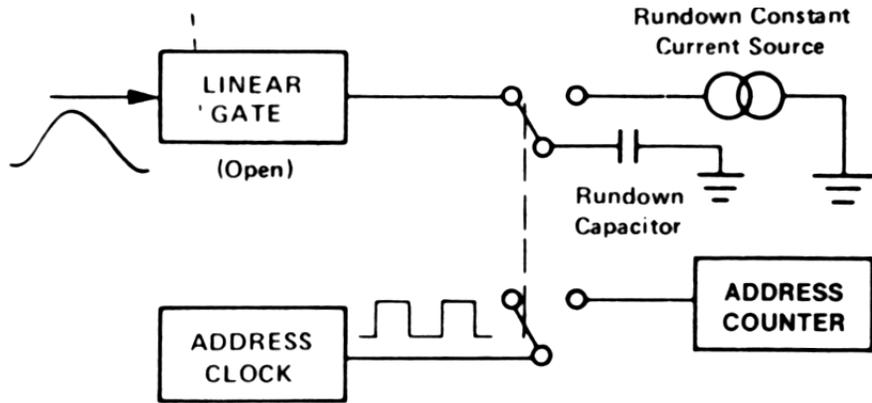
The Single Slope ADC



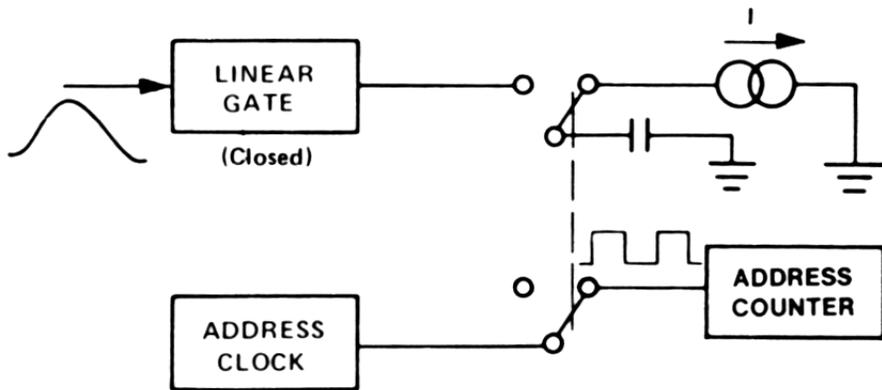
- Analog signal of each channel from the shaper is fed to a comparator and compared with a common ramping reference voltage V_{REF} .
- Pulses, rather than analog signals are transmitted on the cable.
- The times of transitions representing input voltage values are digitized by TDC blocks inside FPGA.
- This approach sometimes is (mistakenly) referred as “Wilkinson ADC”.



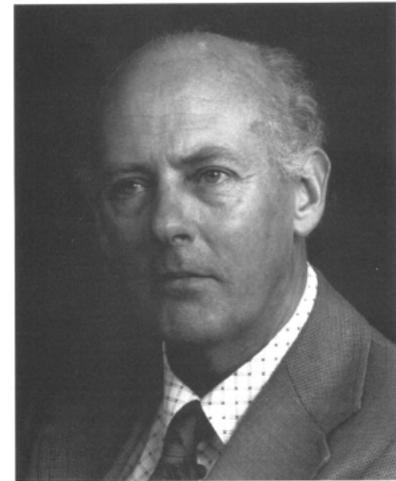
The Wilkinson ADC



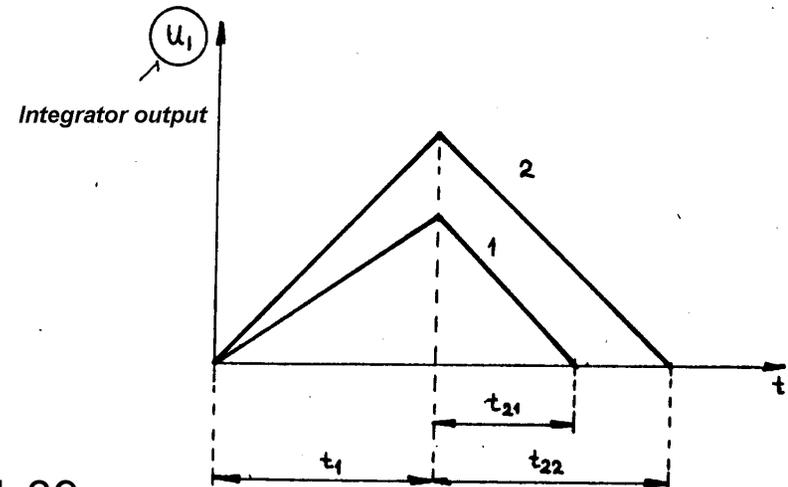
(a) Capacitor Charging



(b) Capacitor Rundown

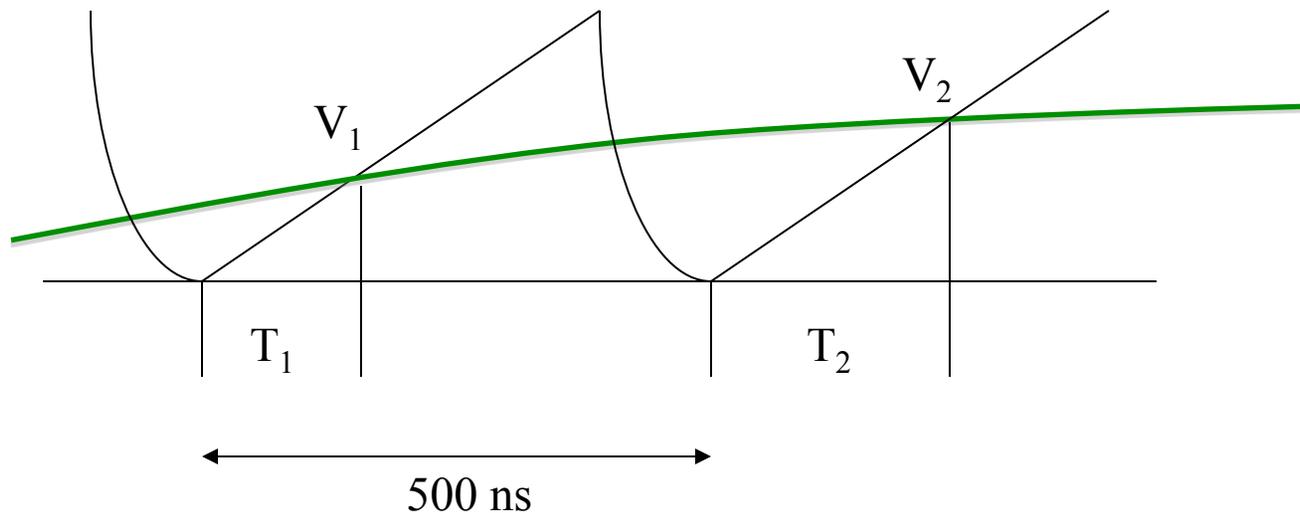


Denis Wilkinson



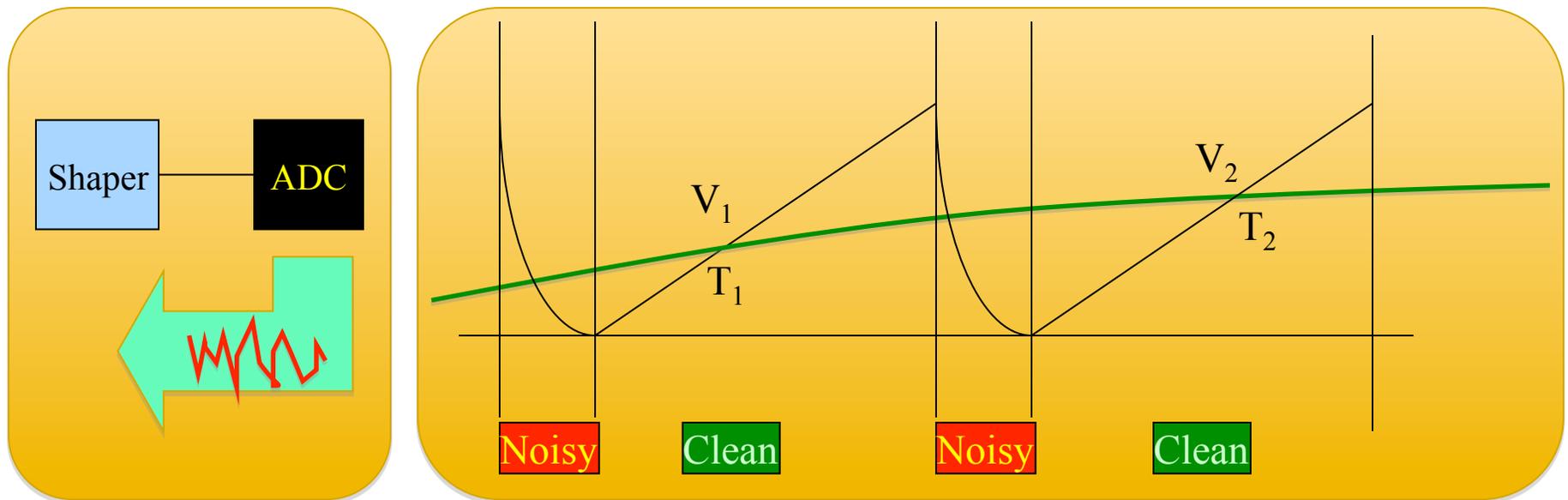
Ref: Annu. Rev. Nucl. Part. Sci. 1995.45.'1-39
http://www.dnp.fmph.uniba.sk/~kollar/je_w/el3.htm

TDC Resolution Requirement



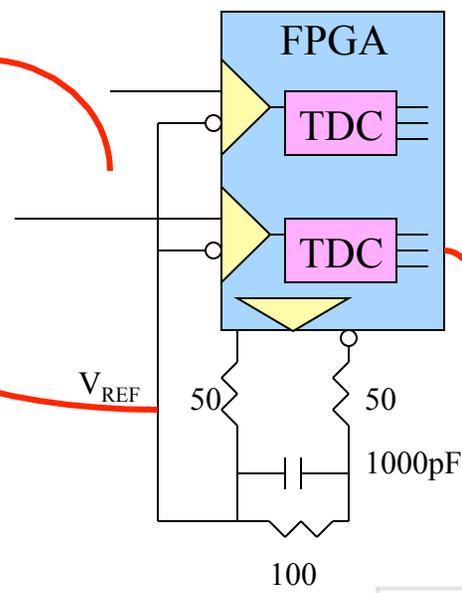
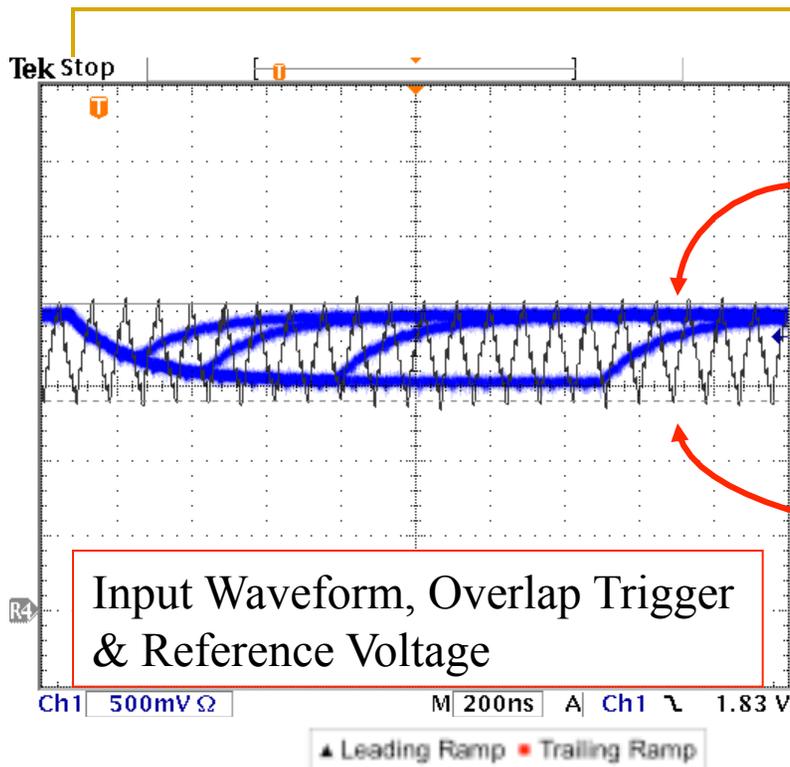
- ❑ Consider sampling rate at 2 MHz, the whole ramping cycle is 500 ns.
- ❑ Arrange 409.6 ns for upward ramping.
- ❑ To achieve 12-bit ADC precision, the TDC LSB is $(409.6 \text{ ns})/4096 = 100 \text{ ps}$.
- ❑ TDC with 100 ps LSB can be comfortably implemented in FPGA today.

Digital Noise During Digitization

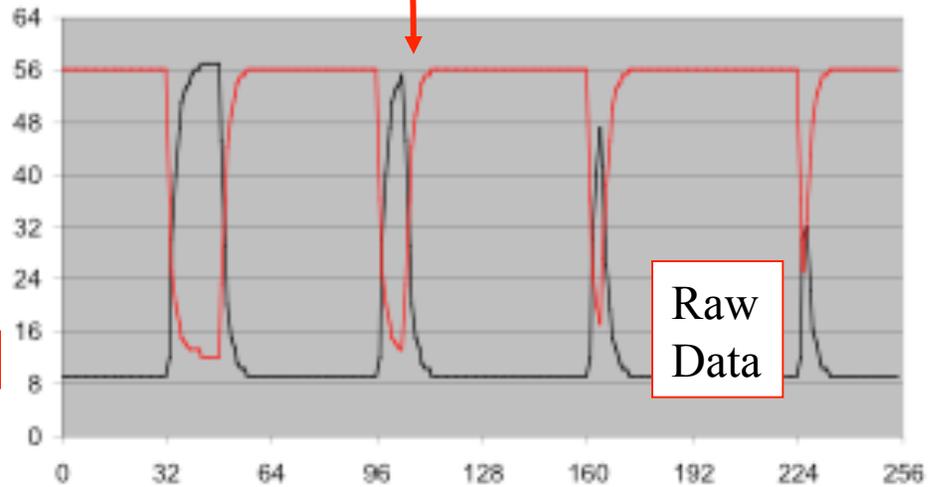
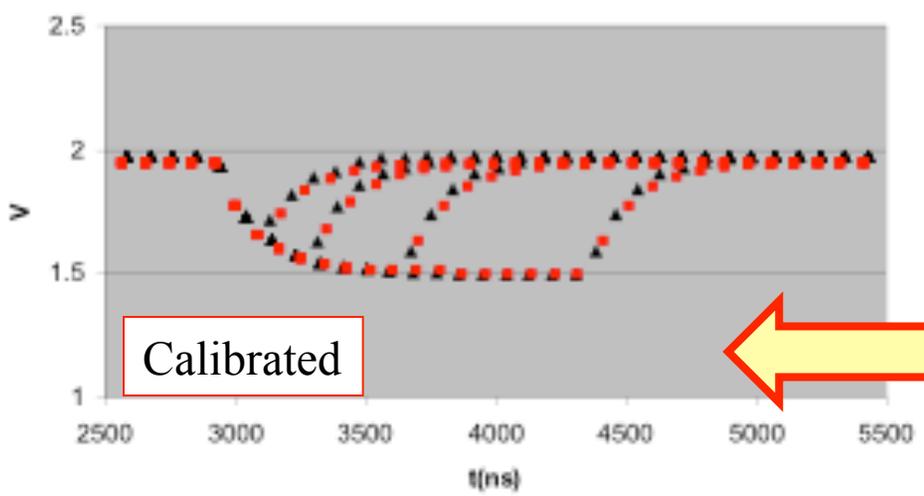


- ❑ Typical ADC devices creates noise that may interfere the analog circuits.
- ❑ The time interval for resetting of the common reference voltage may be noisy but analog signal is not sampled during it.
- ❑ There is no digital control activities during ramping up of the common reference voltage.

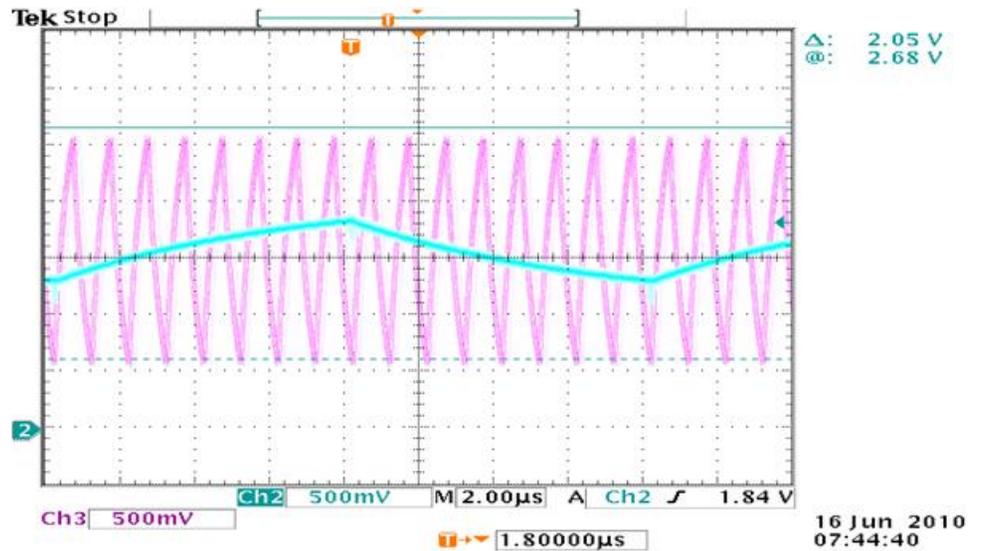
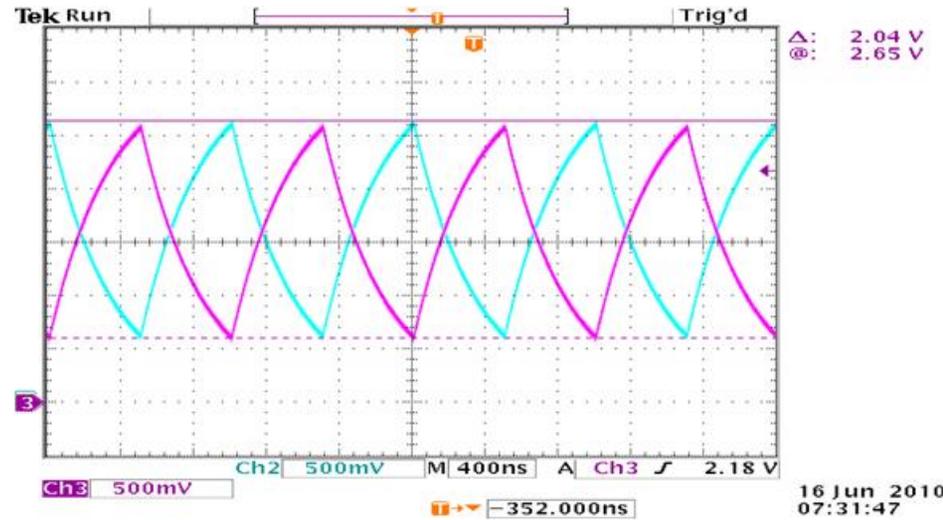
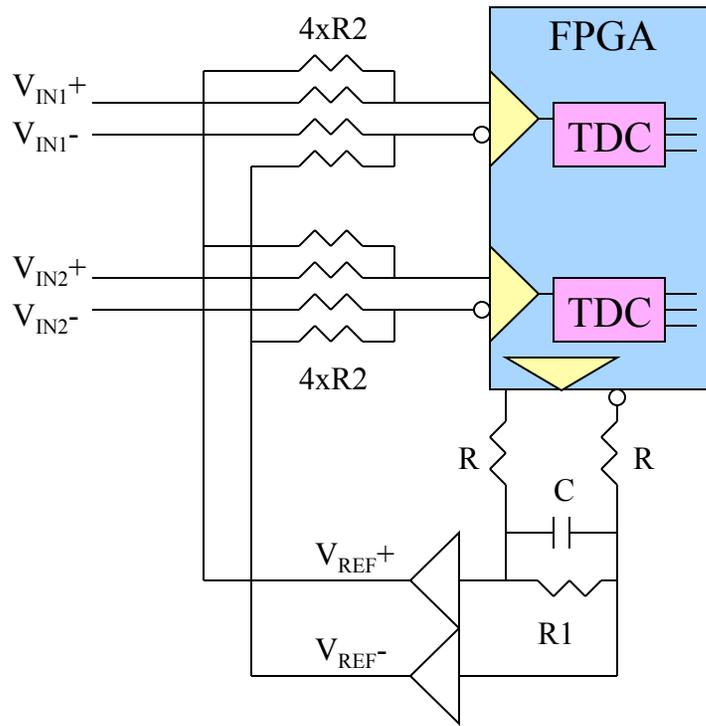
Single Slope ADC Test: Waveform Digitization



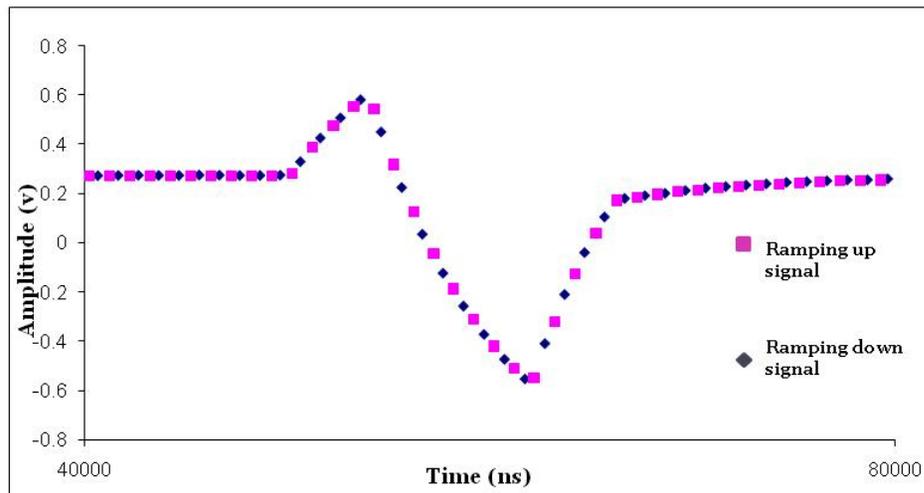
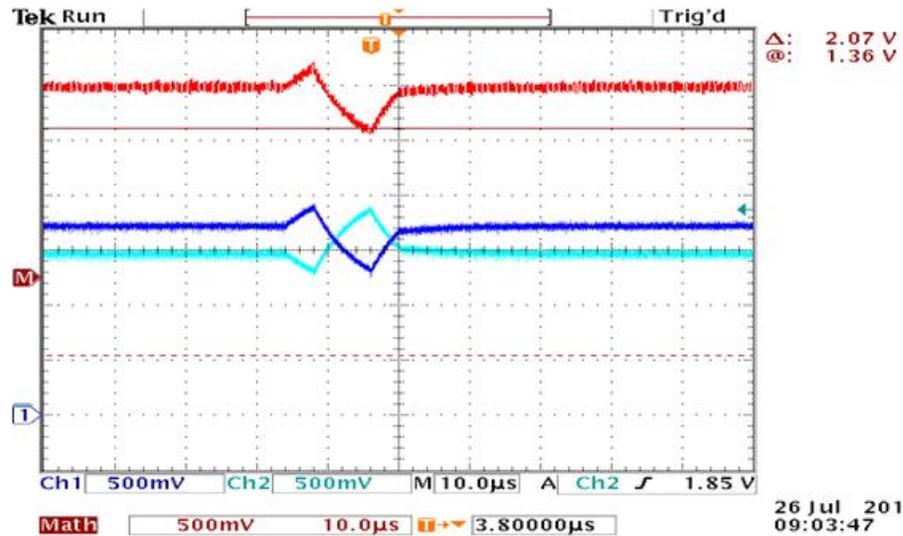
- Shown here is a demo of a 6-bit single slope TDC.
- Sampling rate in this test is 22 MHz.
- Both leading and trailing reference ramps are used in this example.
- Nonlinear reference ramping is OK. The measurement can be calibrated.



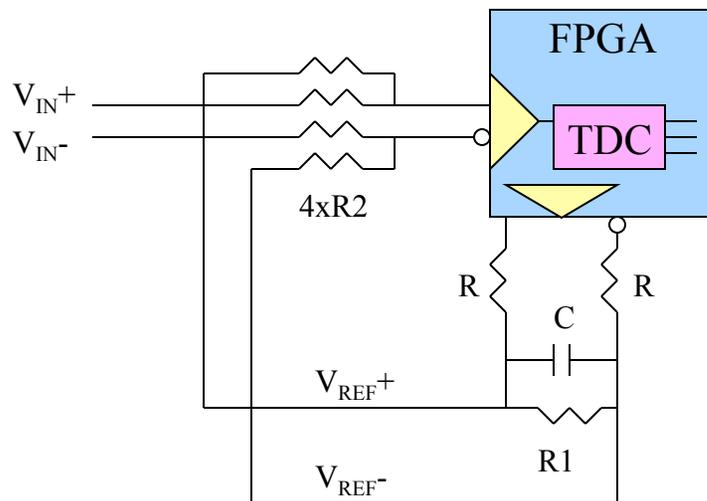
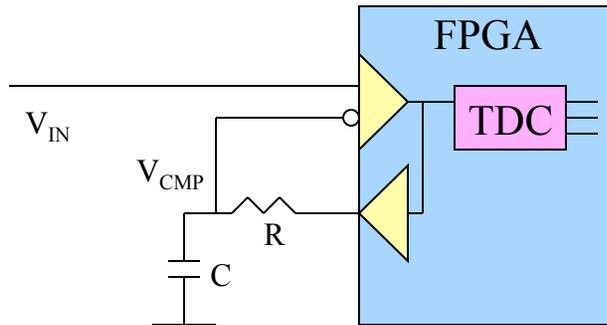
Differential Inputs and Ramping Reference Voltage



ADC Test Results

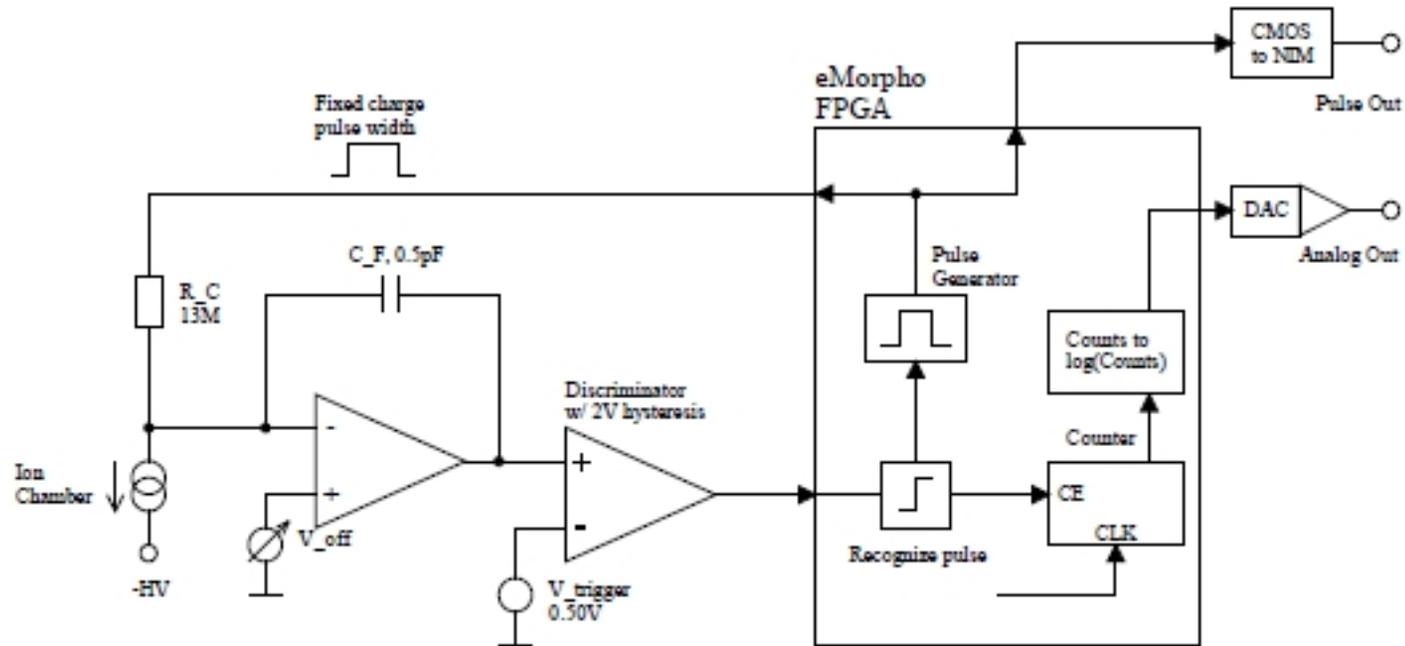


The Sigma-Delta ADC

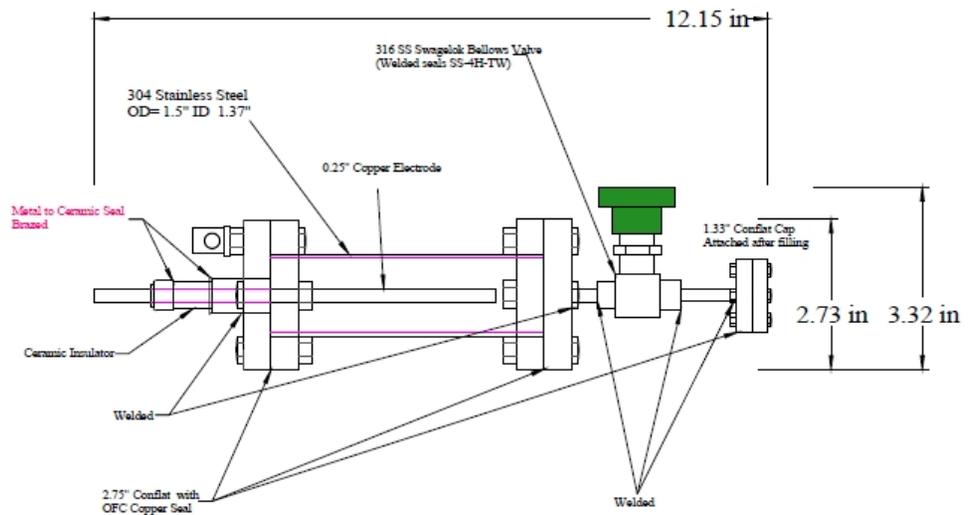
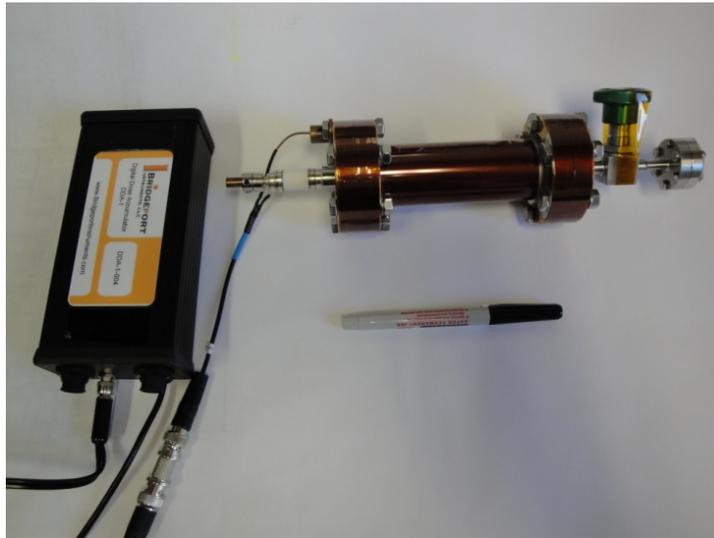


Recycling Integrator

Recycling Integrator for nA Measurement



Cryogenic Ionization chamber 5k - 350K



It is a helium-filled ionization chamber. It's current is proportional to the dose rate.

- The signal current is processed by a current to frequency converter to achieve a wide dynamic range and quick response dose rate excursions.
- All materials used are known to be radiation hard and suitable for operation at 5K.
- The electronics is self-contained and requires no computer to operate.



Cryogenic Loss Monitor operation

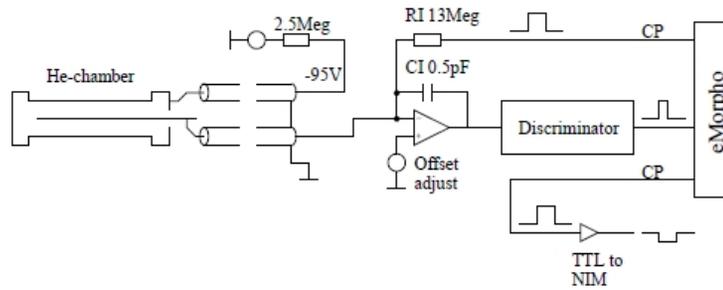
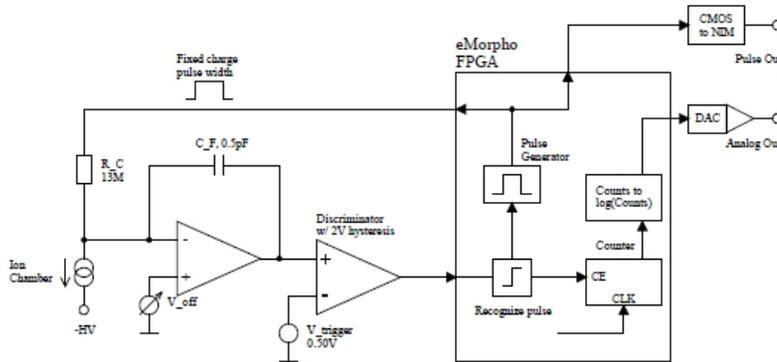


Figure 1: Schematic view of the dose rate monitor.

The chamber housing is held at negative potential and negative charge is collected on the center electrode. The HV is -95 V and is kept well below the minimum breakdown voltage of 156V in Helium.

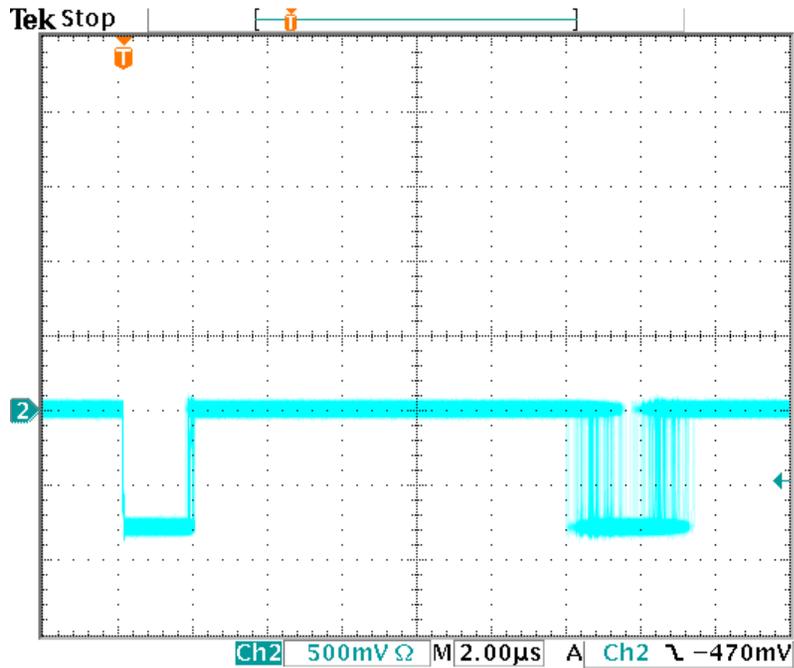
The electronics uses a recycling integrator as a current to frequency converter with a wide dynamic range. The charge per pulse is 1.63pC or 238μR at 1 atm (room temp) of He.



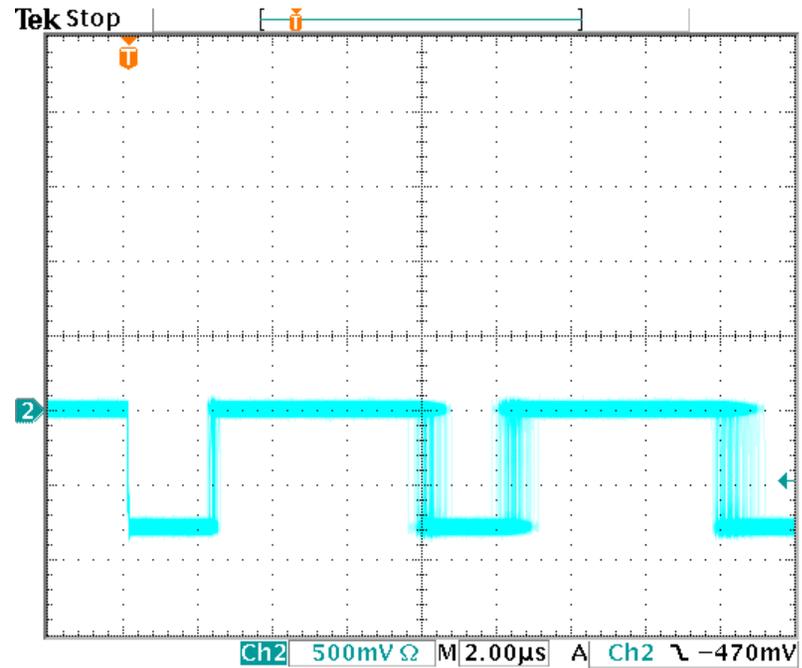
Drawing 1: Simplified schematics of the digital dose accumulator using a recycling integrator and the eMorpho platform. Future versions may use a lower-cost platform.

The recycling integrator consists of a charge integrating amplifier with a 0.50 pF capacitance followed by a discriminator which senses when the capacitor is fully charged.

Pulses at 150 nA and 300 nA



10.80 %

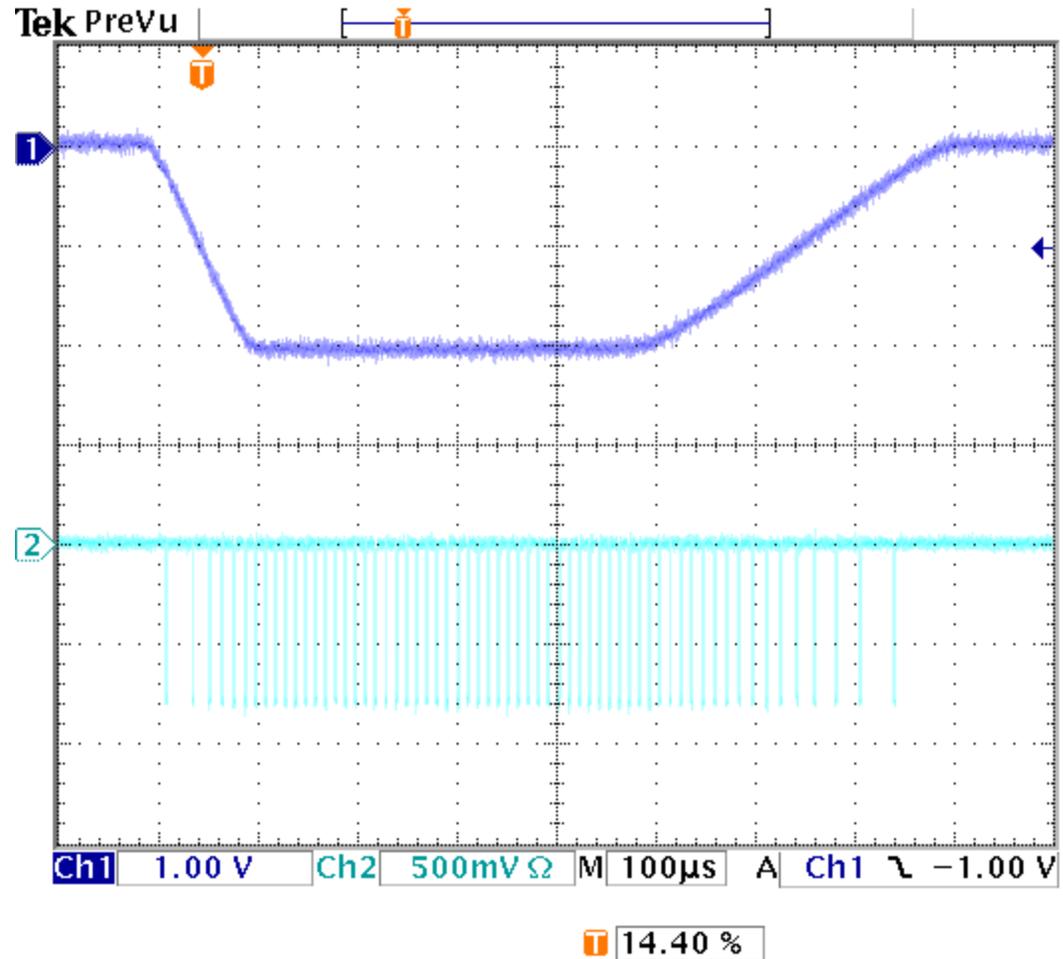


10.80 %

Input Current and Output Pulses

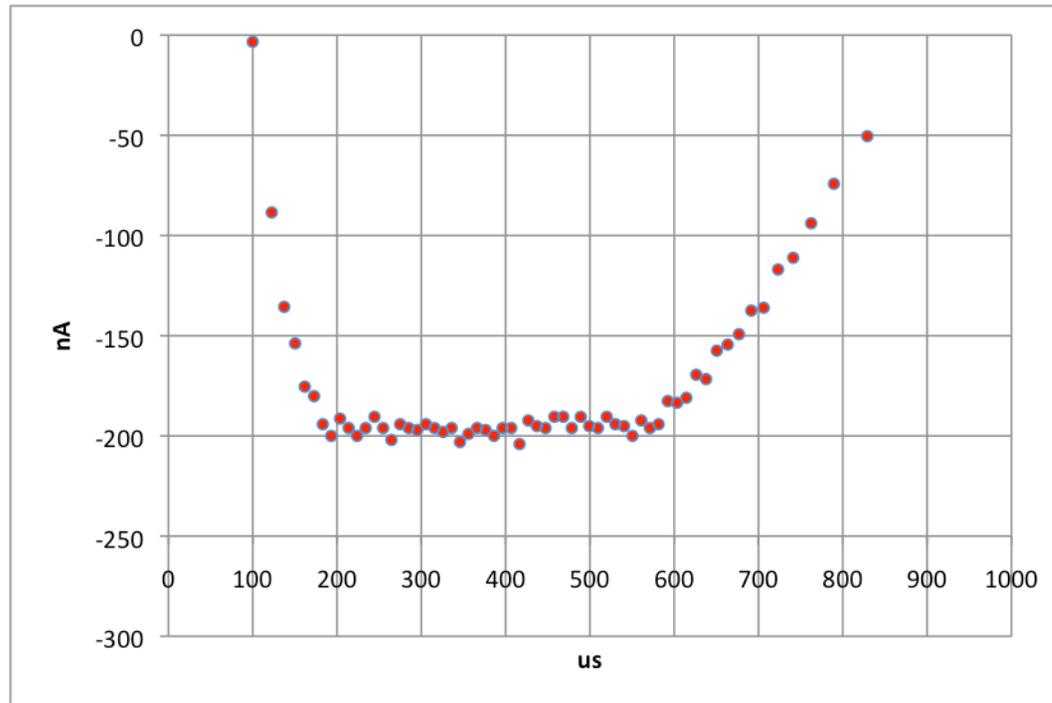
Input Current
100 nA/div

Output Pulses



Current Measurements Using TDC

$$I=Q/dt$$



An aerial photograph of a golf course. The course is a large, winding green with several holes and fairways. In the center-right, there is a clubhouse building with a distinctive white, curved roof. To the left of the clubhouse, a tall, white water tower stands prominently. The surrounding area includes various fields, some of which are brown, suggesting they might be harvested or fallow. There are also some residential or commercial buildings in the distance. The overall scene is a mix of natural greenery and man-made structures.

The End

Thanks

Gaussian Distribution

- Use MS Excel to plot the Gaussian distribution from $\mu - 5\sigma$ to $\mu + 5\sigma$. For simplicity, assume $\sigma=1$ and $\mu=10$.
- Show that $\text{FWHM} = 2.35482\sigma$.
- If a detector has a energy measurement error $\sigma=10\text{keV}$, after collecting 10000 photos of 511 keV, how many measurements will be within 511 keV ± 10 keV? ± 20 keV? ± 30 keV?
- (Optional) Use MS Excel to generate 10000 numbers with mean = 511 and $\sigma = 10$ and count numbers in [501, 521], [491, 531], [481, 541].

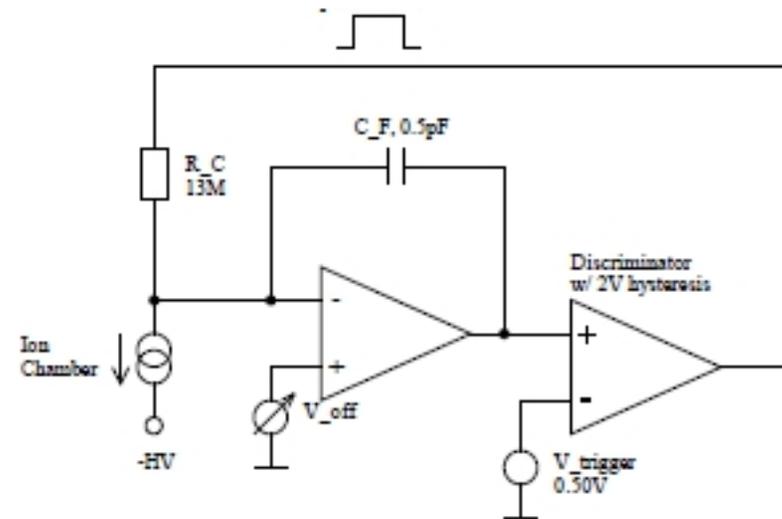
Digitization Error

- Consider a bin in a digitizer covering a range of $[a, a+w]$. If the input v is within $[a, a+w]$, the input is reported to have a nominal value $a+w/2$. Show that for uniform distribution, the standard deviation introduced is $w/\sqrt{12}$.
- Show that if the nominal value is not $a+w/2$, the standard deviation will be bigger.
- Use MS Excel to generate 10000 random numbers from 0 to 1 with uniform distribution, compare the standard deviation with the theoretical number.

Ultra-wide Bins

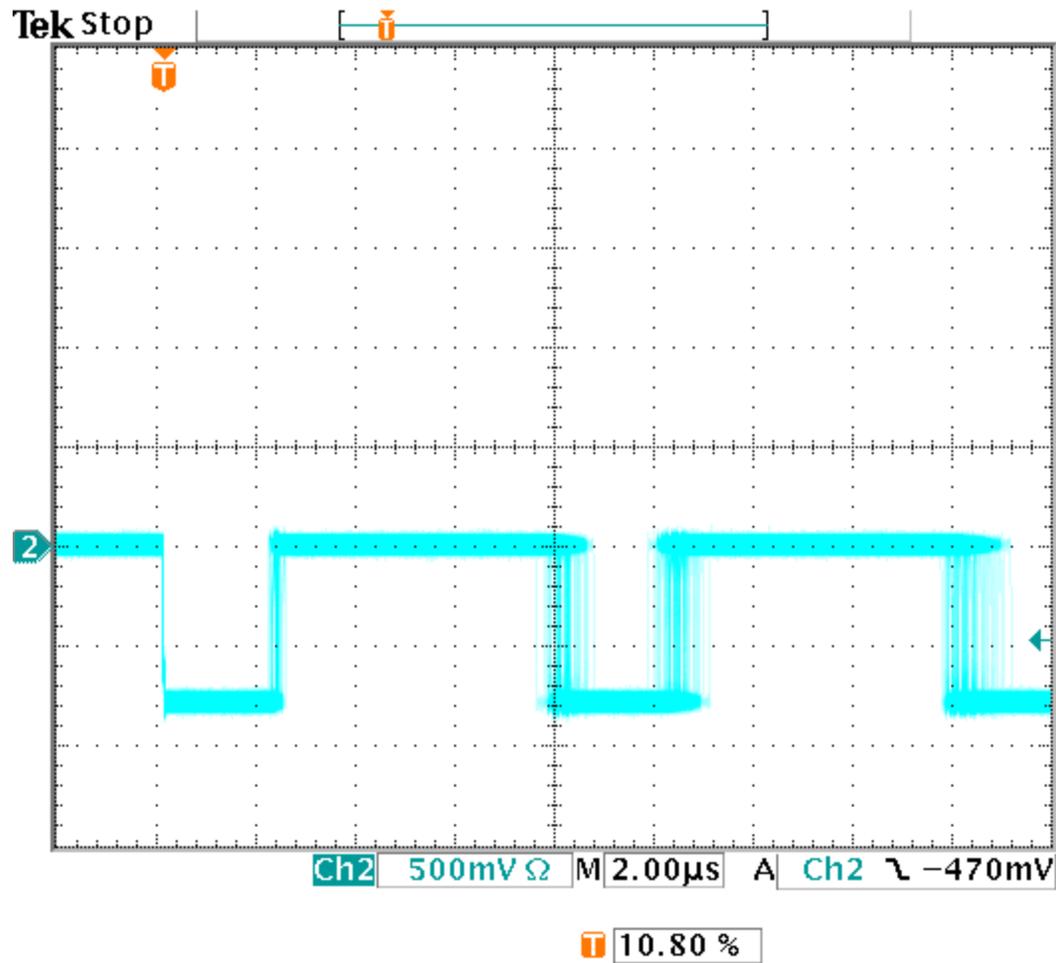
- Consider an ADC with 8 bins with widths: 3V, 1V, 1V, 1V, 1V, 1V, 1V, 1V, will the outputs of the ADC be different for inputs 4.7 and 5.7V? And for inputs 1.7 and 2.7V?
- If N input values are evenly distributed in 0 to 10V, how many measurement points will be found in each of these bins?
- For measurements in bins with width=1V and width=3V, what are the standard deviations of the measurements?
- What is the standard deviation of all measurements in entire 0 to 10V range.
- What is the equivalent bin width corresponding to the standard deviation calculated above?
- (Optional) Use MS Excel to generate 10000 random numbers from 0 to 10 with uniform distribution, compare the standard deviation with the calculated number.

Recycling Integrator

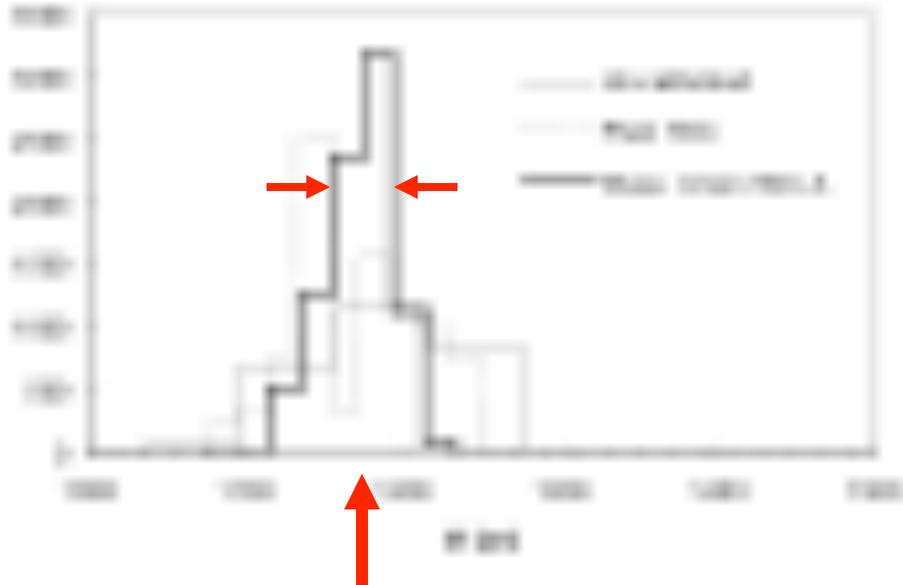


- Consider the recycling integrator above. If the charging current through R_C is 250 nA when the discriminator output is high, what are the output pulse width and interval between two pulses when the ion chamber current is 10 nA? 100 nA? 200 nA?

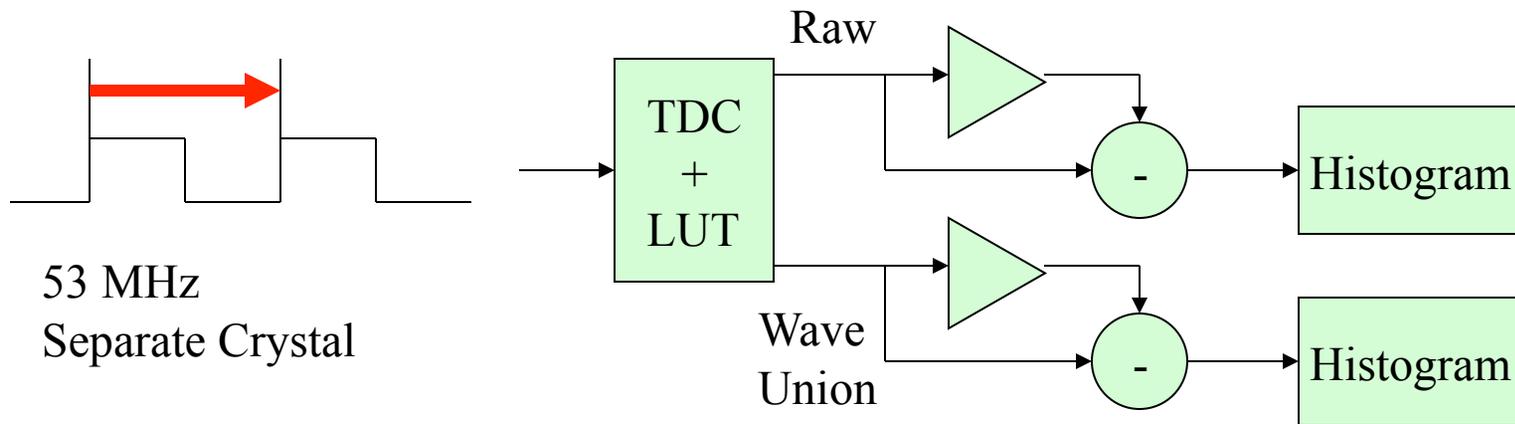
Pulses at 300 nA



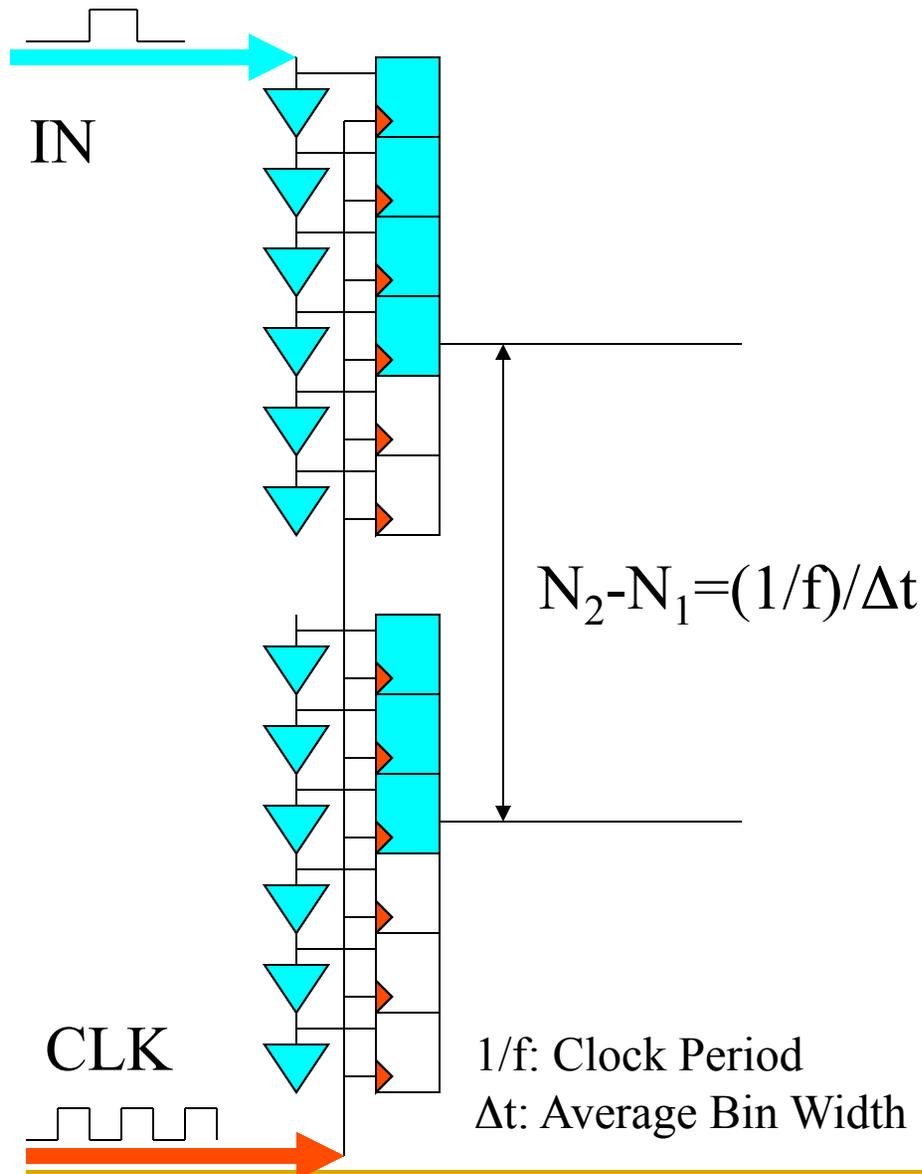
Measurement Result for Wave Union TDC A



- Plain TDC:
 - delta t RMS width: 40 ps.
 - 25 ps single hit.
- Wave Union TDC A:
 - delta t RMS width: 25 ps.
 - 17 ps single hit.



Digital Calibration Using Twice-Recording Method



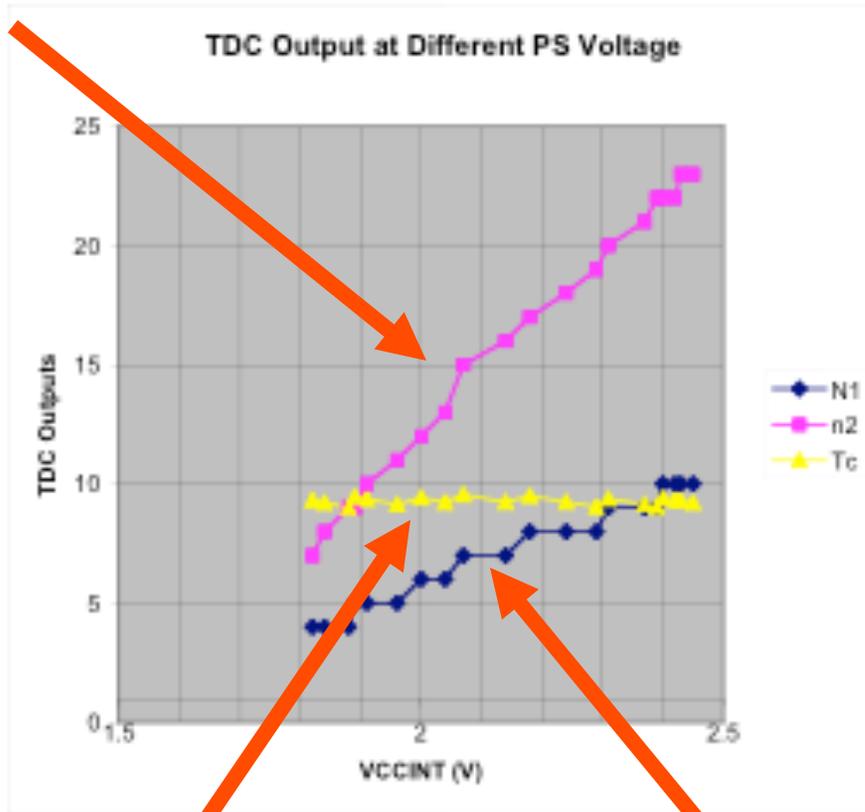
- Use longer delay line.
- Some signals may be registered twice at two consecutive clock edges.

The two measurements can be used:

- to calibrate the delay.
- to reduce digitization errors.

Digital Calibration Result

N_2



Corrected Time

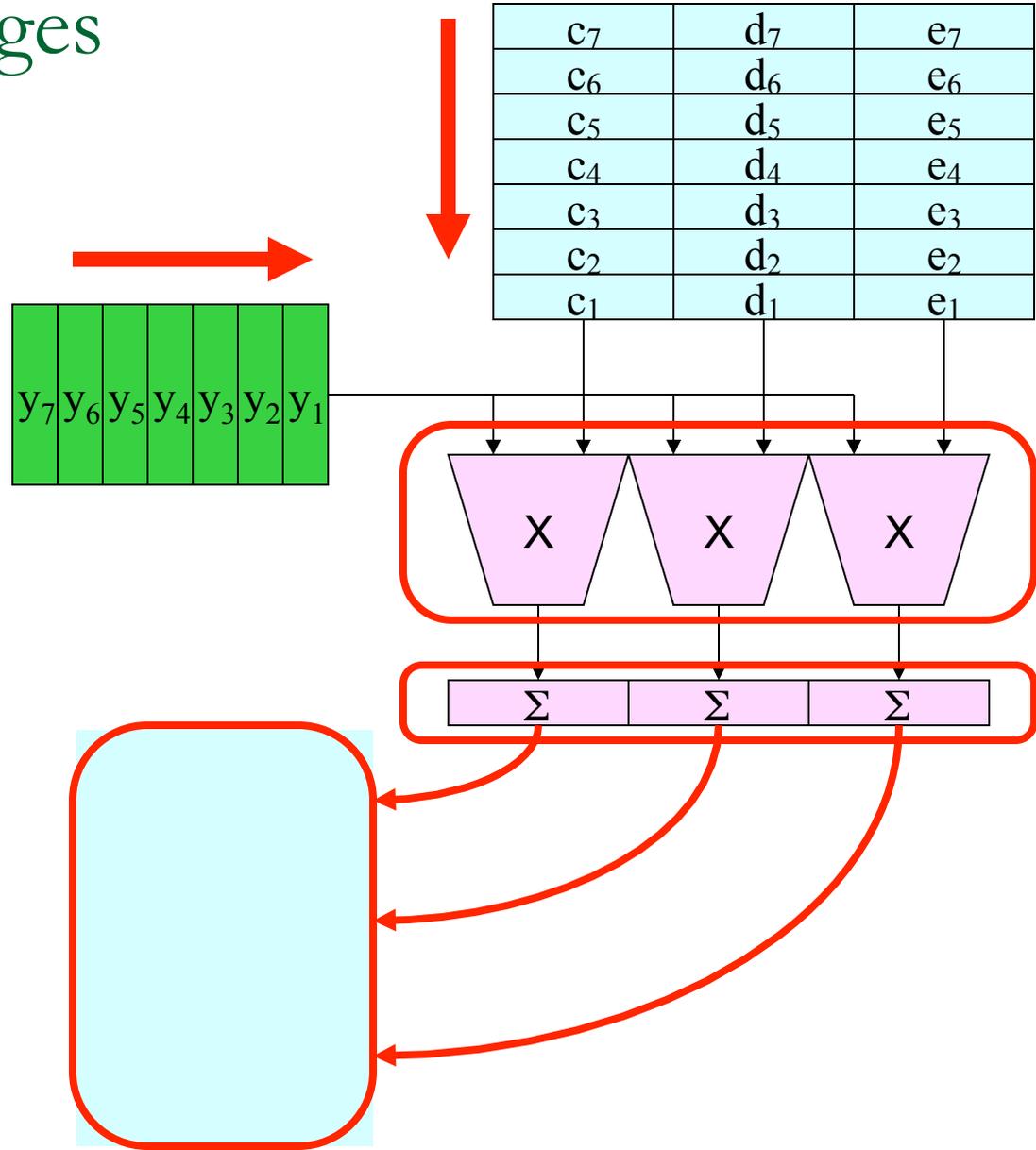
N_1

- Power supply voltage changes from 2.5 V to 1.8 V, (about the same as 100 °C to 0 °C).
- Delay speed changes by 30%.
- The difference of the two TDC numbers reflects delay speed.

■ **Warning: the calibration is based on average bin width, not bin-by-bin widths.**

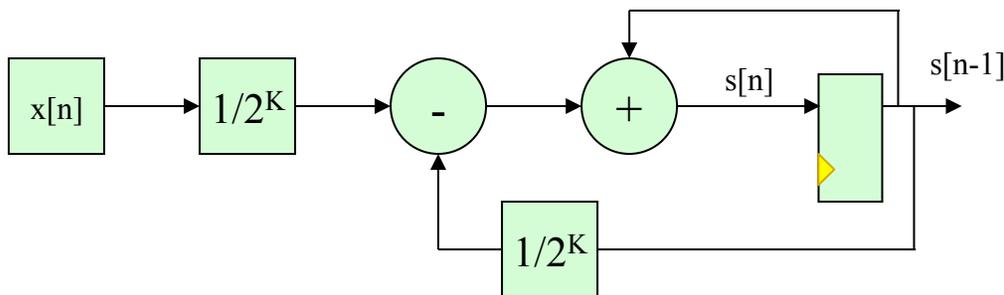
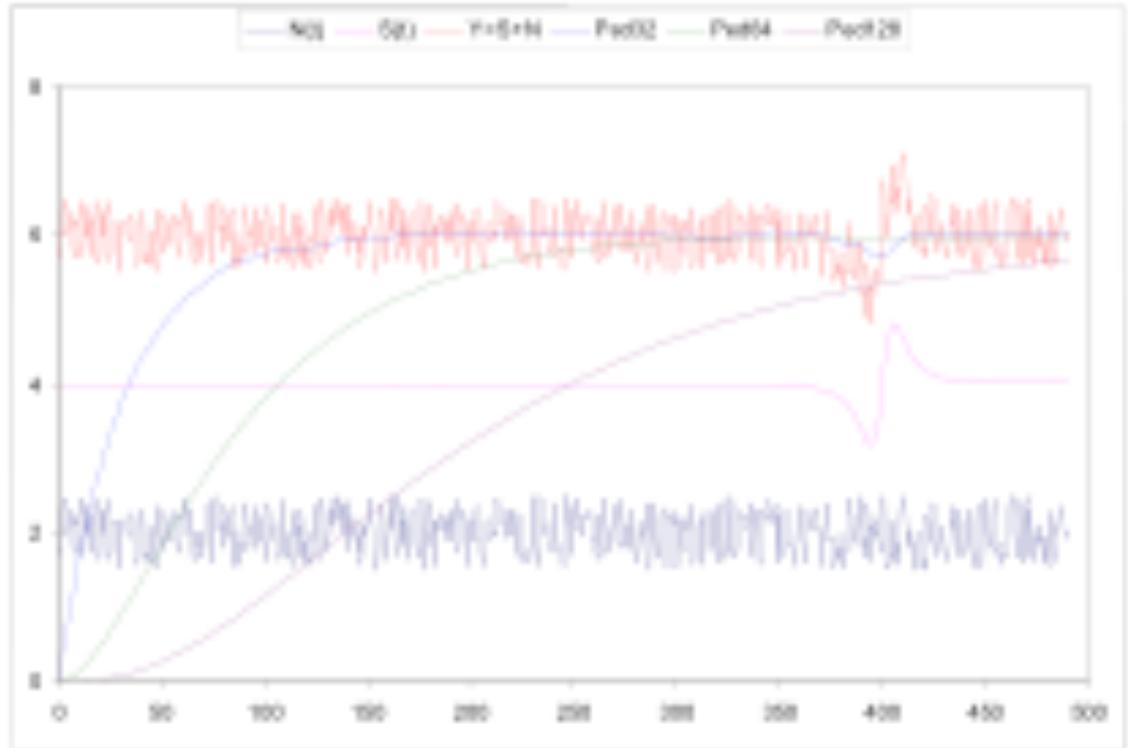
Weighted Averages

- The weighted average is a special case of inner product.
- Multipliers are usually needed.



Exponentially Weighted Average

- No multipliers are needed.
- The average is available at any time.
- It can be used to track pedestal of the input signals.



$$s[n] = s[n-1] + (x[n] - s[n-1]) / N$$
$$N = 2, 4, 8, 16, 32, \dots$$