An aerial photograph of the Fermilab facility. The image shows a large, circular track or road that winds through a green, wooded area. In the background, there are several large, modern buildings, including a prominent white, curved structure. The surrounding landscape is a mix of green fields and brown, cleared areas. The sky is clear and blue.

PET Fundamentals: Electronics (2)

Wu, Jinyuan

Fermilab

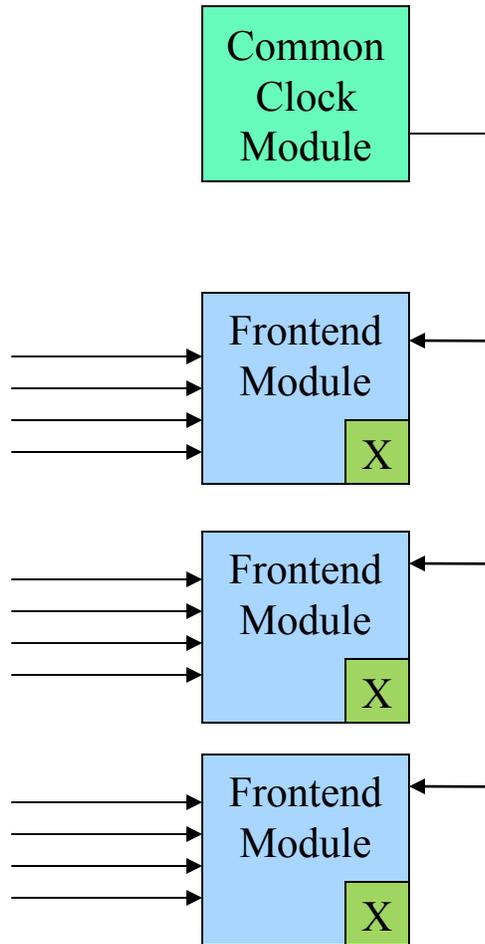
Apr. 2011

Introduction

- Clock Distribution.
- Timing Reference.
- Coincidence Trigger.
- Serial Communication

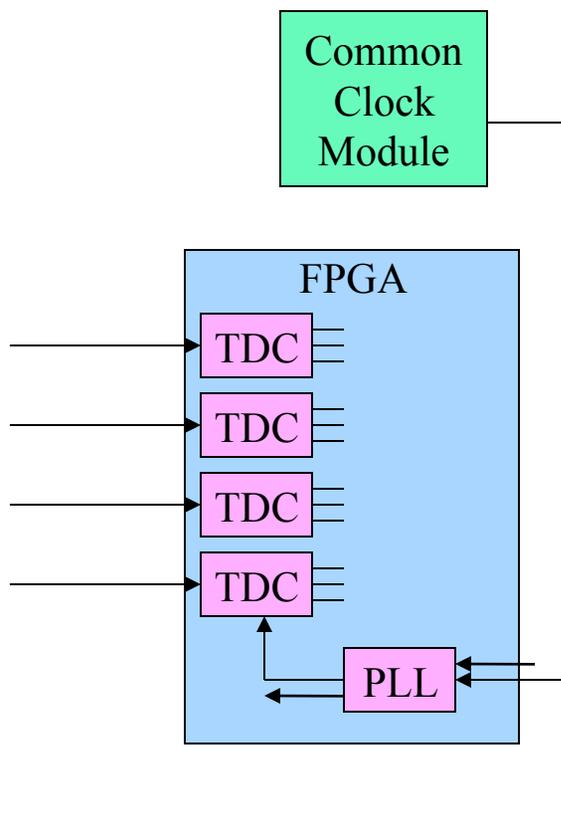
Common Clock Distribution

Common Clock Distribution

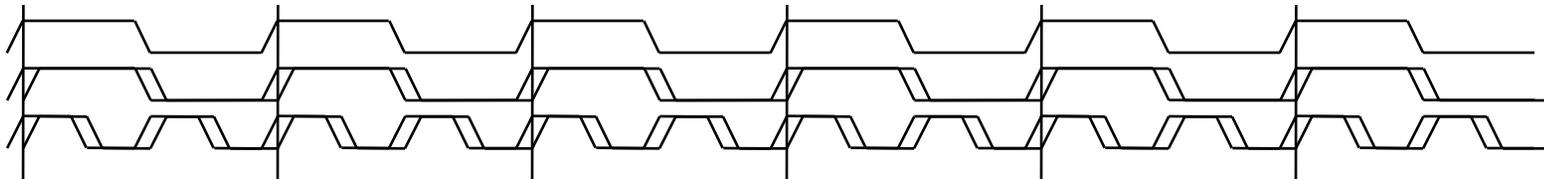


- Frontend modules have their own crystal oscillators: (X).
- The frequencies of the oscillators may be slightly different.
- The relative phases in different module change with time.
- Usually, a common clock is generated and sent to all modules.
 - Frequency: same.
 - Phase: may still have limited drift.

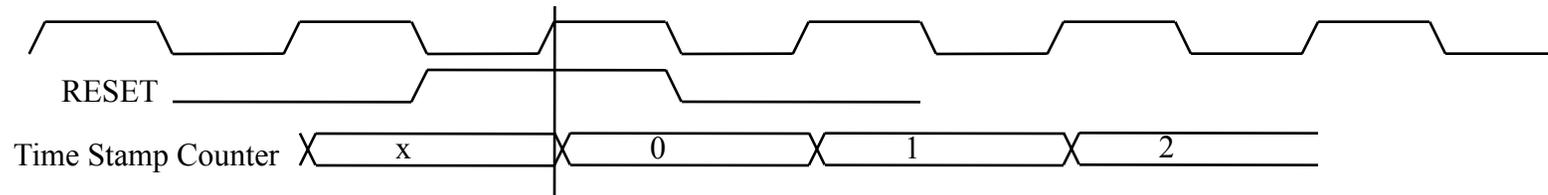
Phase Lock Loop (PLL)



- The phase lock loop (PLL) circuit is a common building block. It can be an IC chip or a functional block inside an FPGA.
- The PLL recreate clock signals with phases lock to the input clock.
- The PLL may create clocks with frequency $f = (n/m) * f_{\text{input}}$. (Therefore, one can distribute slower clock and create faster clock.)
- The outputs of PLL may have small phase shift.
- The PLL in today's FPGA usually allows users to switch clock sources between the local crystal or external clock from the common clock module.

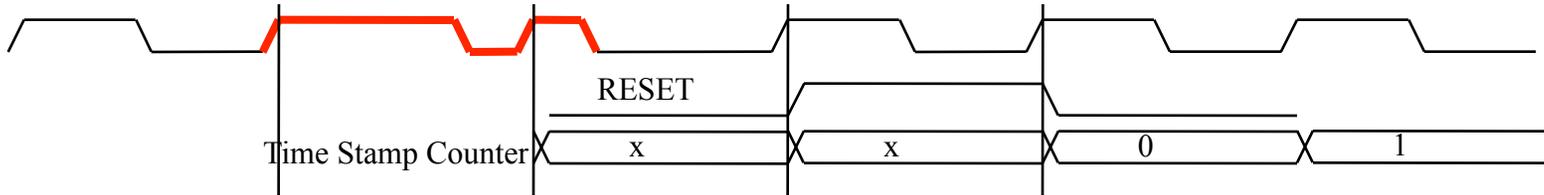


The First Clock Cycle? Reset Signal



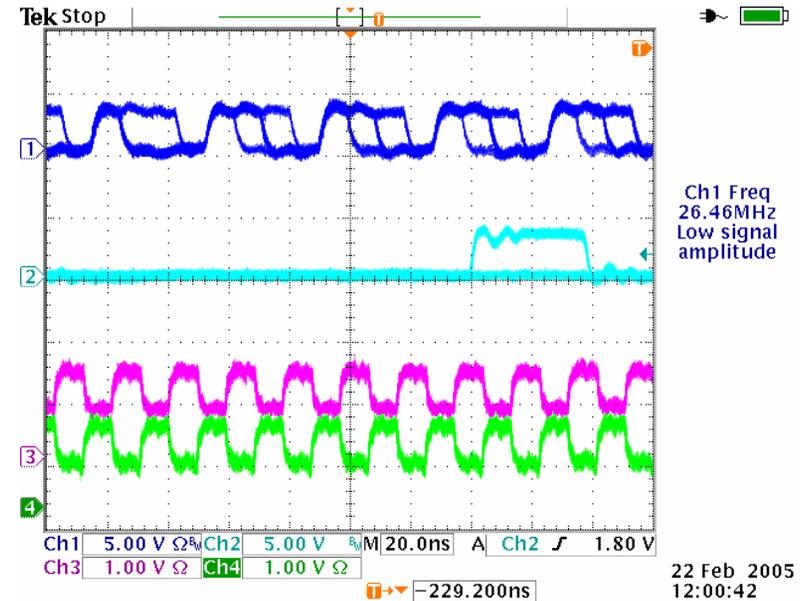
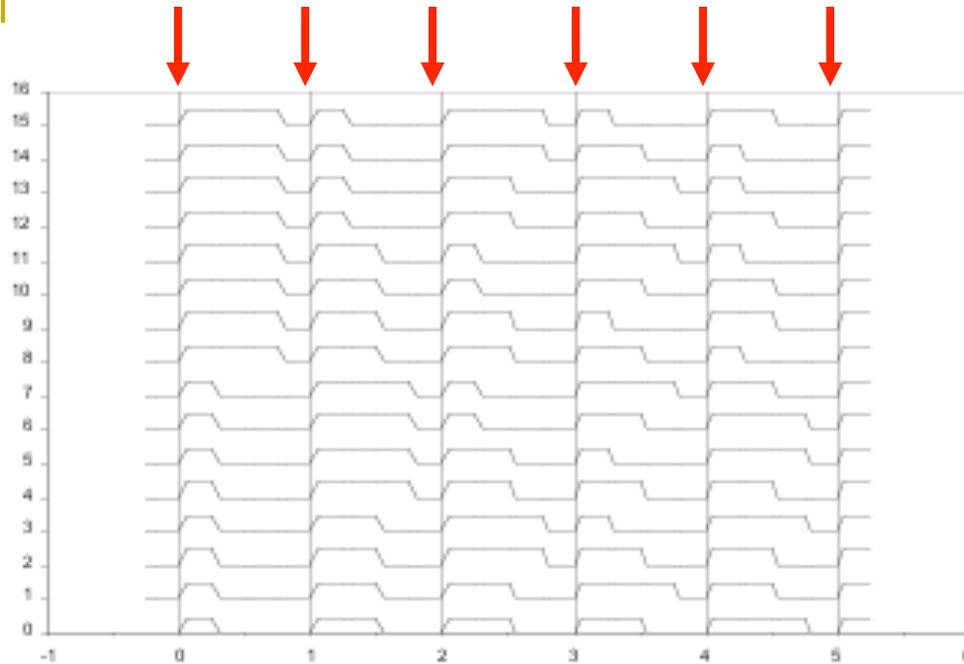
- The phase lock loop (PLL) circuit creates a clock signal with locked phase.
- But which clock cycle is the first cycle is still to be defined.
- One method to provide the first clock cycle information is to send a RESET signal using another cable.
- A time stamp counter is reset and the subsequent clock cycles are indicated by the counter.
- This scheme needs **two critical timing cables**: one for clock and the other for RESET.

Sending Clock and Reset in the Same Cable



- A wide-narrow pulse sequence is generated in the normal clock train.
- The pulse train is DC balanced.
- The receiving circuit detects the pulse sequence and generate a reset signal.
- The time stamp counter is reset and the subsequent clock cycles are indicated by the counter.
- The scheme uses only one critical timing cable.
- A possible receiving circuit is given in the backup slides.
- The scheme is a special case given in next slide.

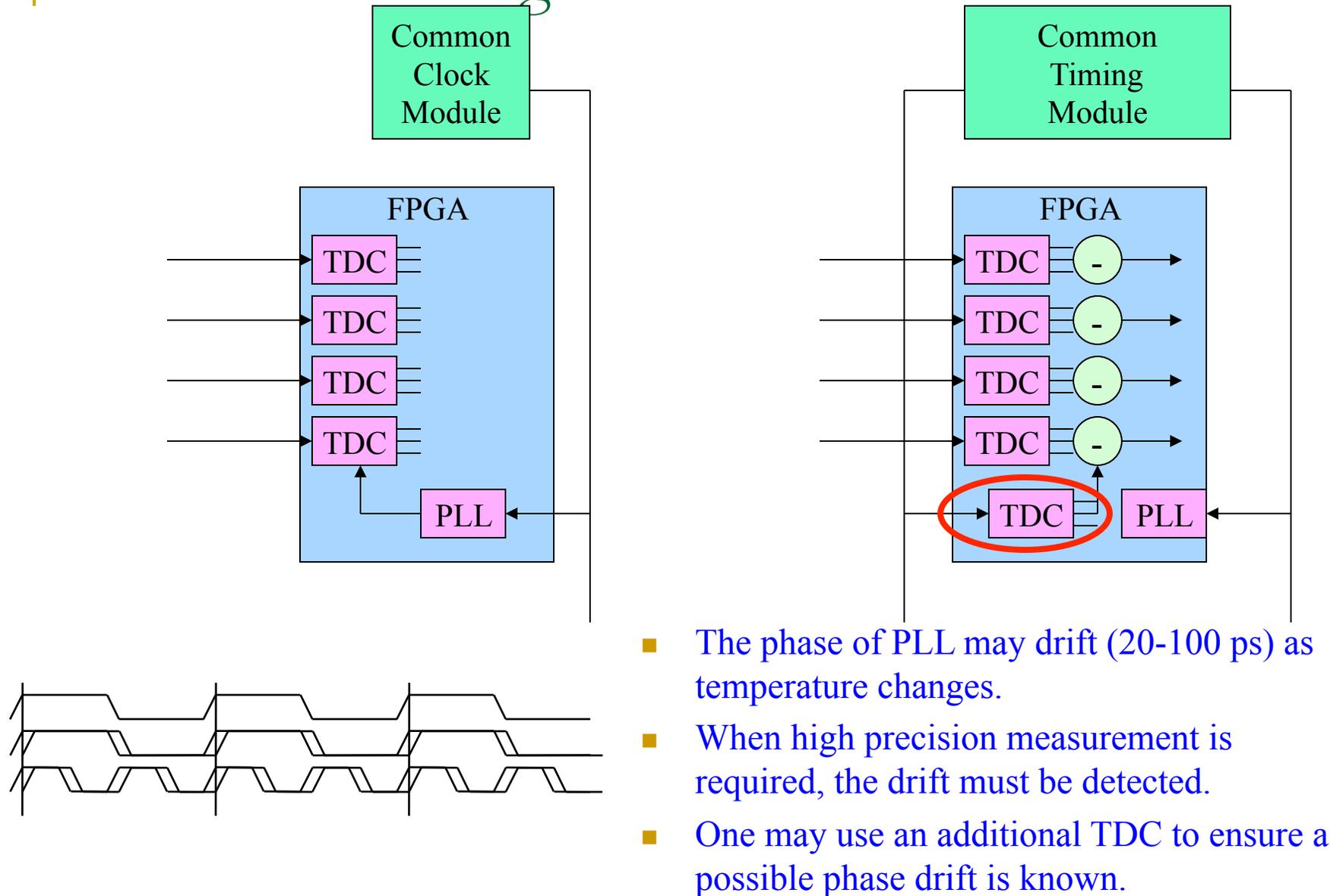
The Clock-Command Combined Carrier Coding (C5)



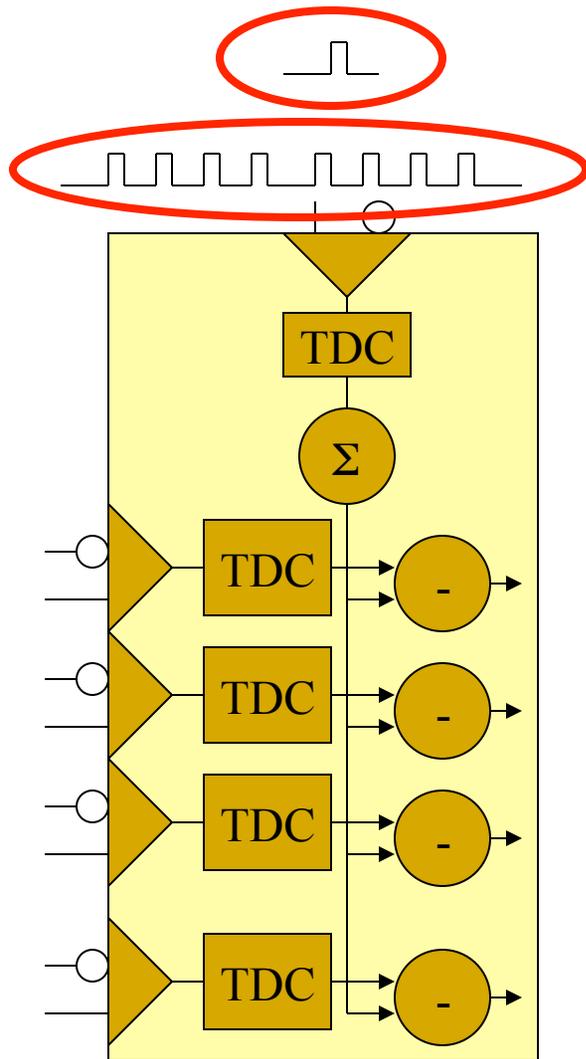
- A data train contains 5 pulses and each pulse is transmitted in four unit time intervals, usually in four internal clock cycles at frequency f .
- Information is carried with wide, normal and narrow pulses and the first pulse is always wide or narrow.
- When not transmitting data, all pulses have normal width.
- The data stream is DC balanced over 5 pulses suitable for AC coupled transmission.
- All leading edges are evenly spread so that the pulse train can be used directly drive the receiver side logic or PLL.

Common Timing Reference

Common Timing: A Cross Check

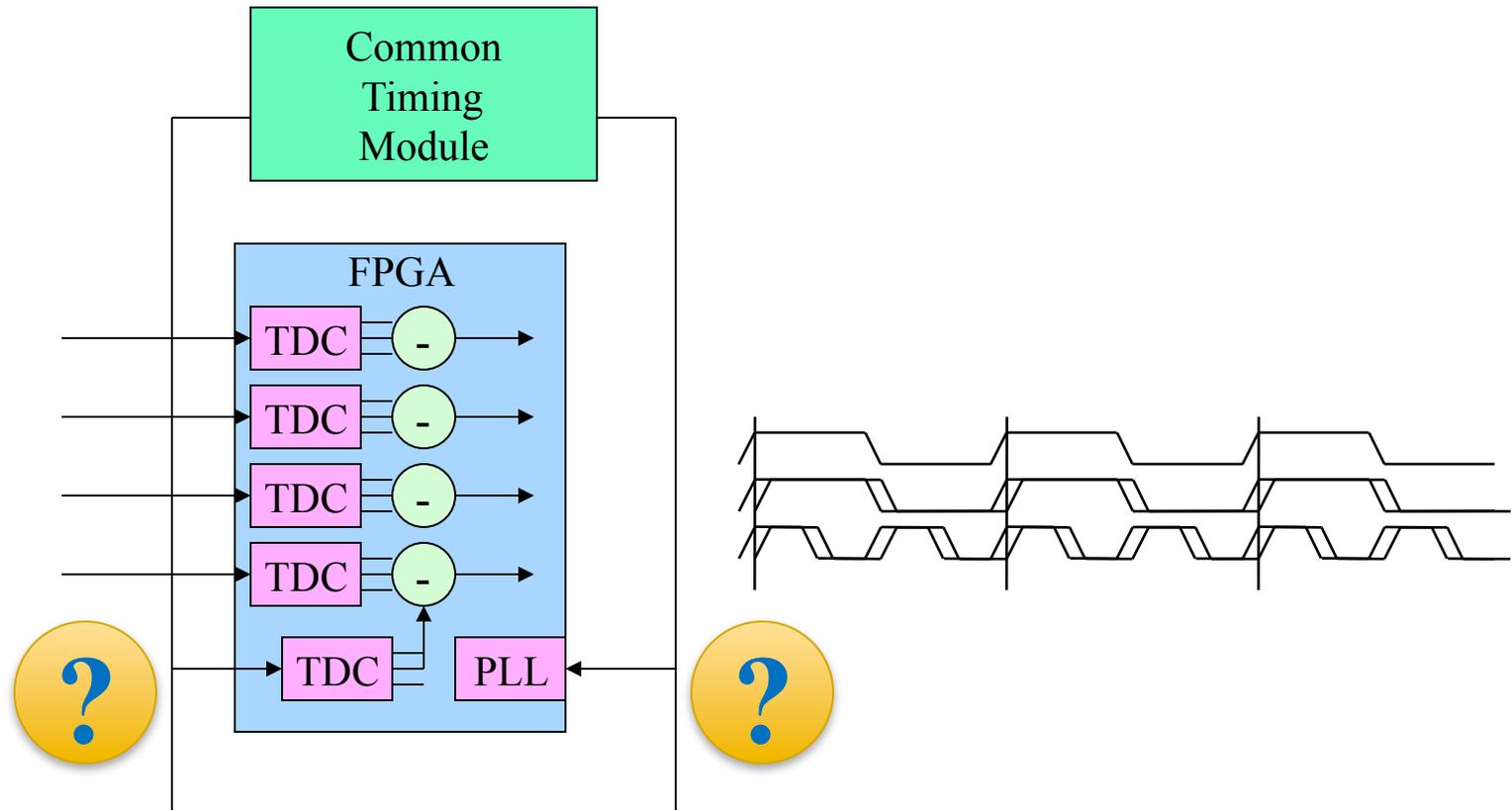


Common Single Pulse and Common Burst



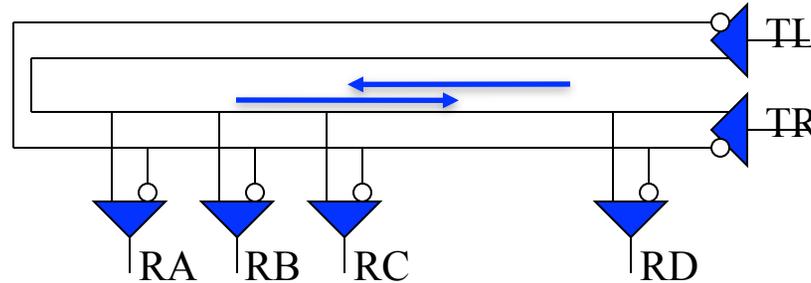
- Traditionally, **common start** or **common stop** signals are **single pulses**.
- Single common pulse increase timing error by $\sqrt{2}$.
- Using the average time of a **common burst** provides finer timing precision.

Good and Reliable Cable?



- The propagation delays in cables may change as temperature changes.
- In applications with high timing precision, is necessary to compensate temperature effect of the cables.
- See next slide for mean timing scheme.

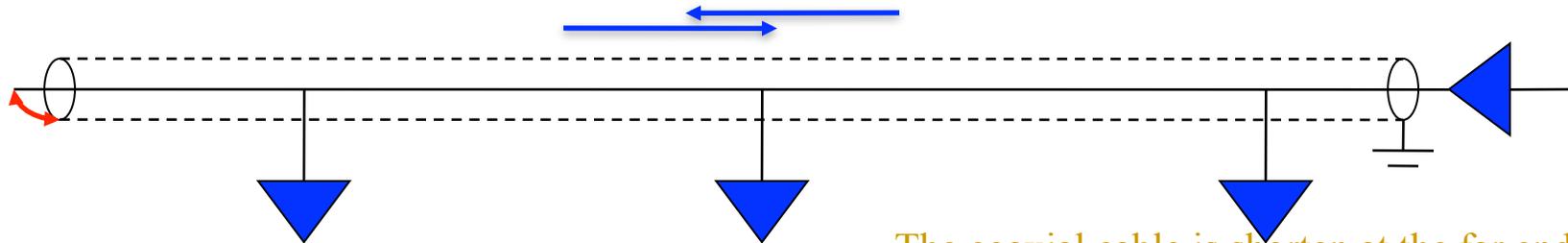
The Mean Timing Scheme



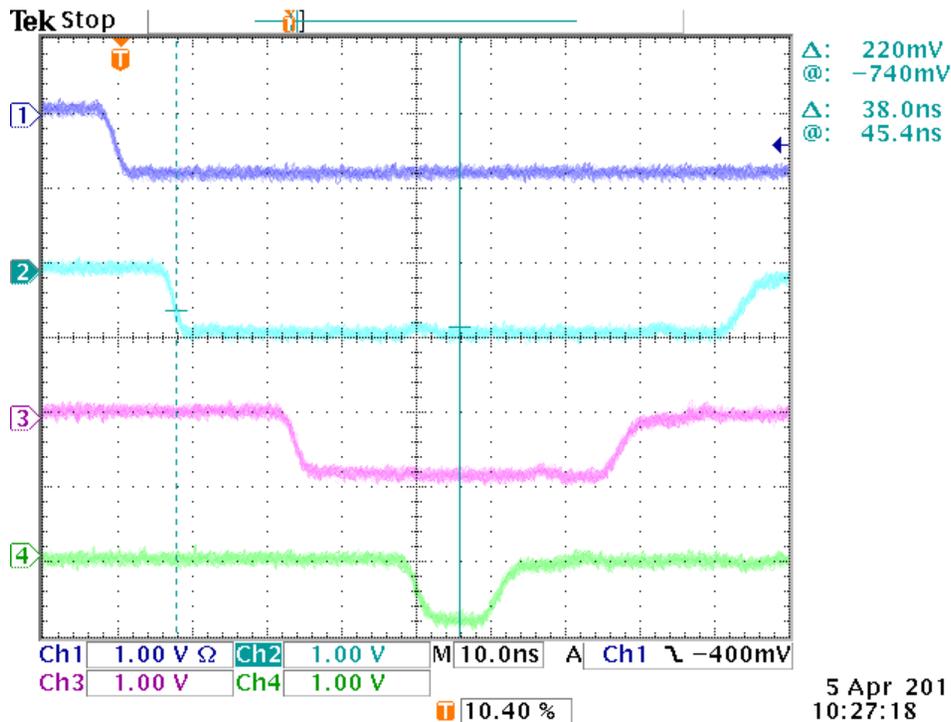
	Time to RA	Time to RB	Time to RC
Signal From Left	$T_L + T_{LA}$	$T_L + T_{LA} + T_{AB}$	$T_L + T_{LA} + T_{AB} + T_{BC}$
Signal From Right	$T_R + T_{RC} + T_{CB} + T_{BA}$	$T_R + T_{RC} + T_{CB}$	$T_R + T_{RC}$
Mean Times:	$\frac{1}{2}(T_L + T_{LA} + T_R + T_{RC} + T_{CB} + T_{BA})$	$\frac{1}{2}(T_L + T_{LA} + T_{AB} + T_R + T_{RC} + T_{CB})$	$\frac{1}{2}(T_L + T_{LA} + T_{AB} + T_{BC} + T_R + T_{RC})$

- The mean times are identical as long as: $T_{AB} = T_{BA}$, $T_{BC} = T_{CB}$, etc.
- In most cases, signals traveling left and right have the same speed.
- The timing relationship between mean times on different module won't change with temperature.
- Identical time can be established on all modules using mean timing scheme.

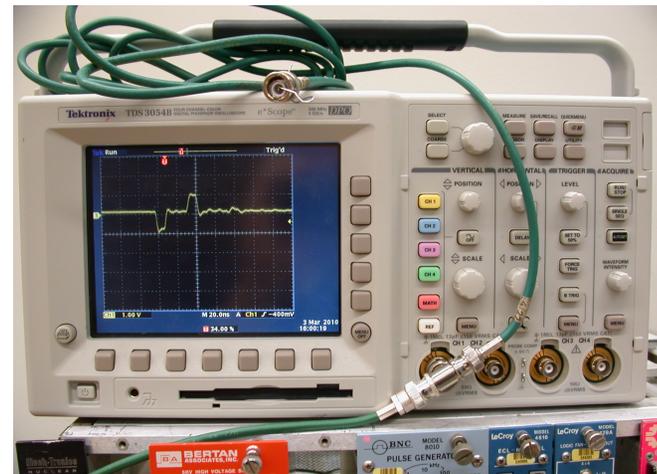
The NIM Clip Wire for Mean Timing



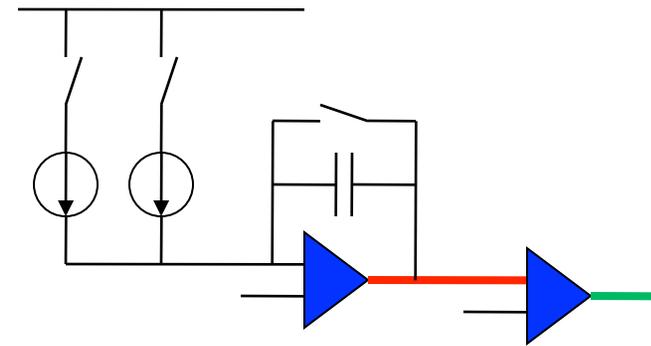
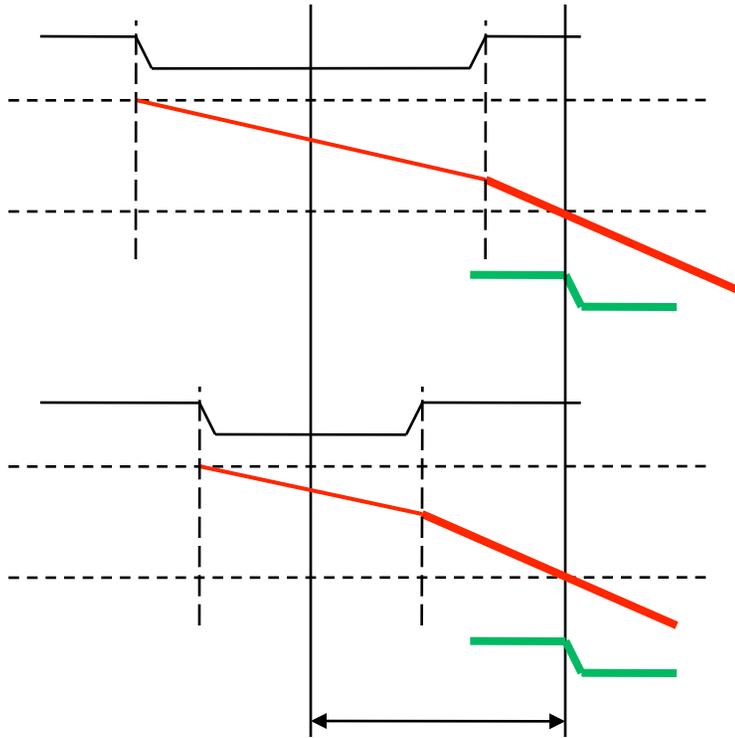
- The coaxial cable is shorten at the far end.
- A NIM transition propagates from driver and reflect back with polarity reversal.
- The times of the leading and the trailing edges at different receivers are different.
- But the mean times are identical.
- Note: Terminate 50 Ohms at the driver end.



5 Apr 2011
10:27:18

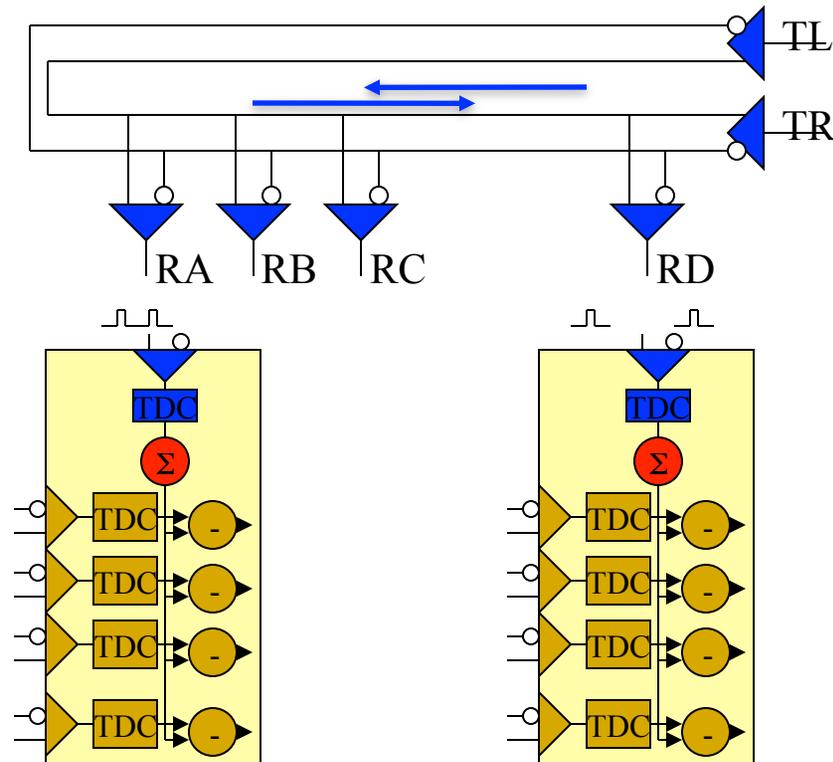


The Analog Mean Timer



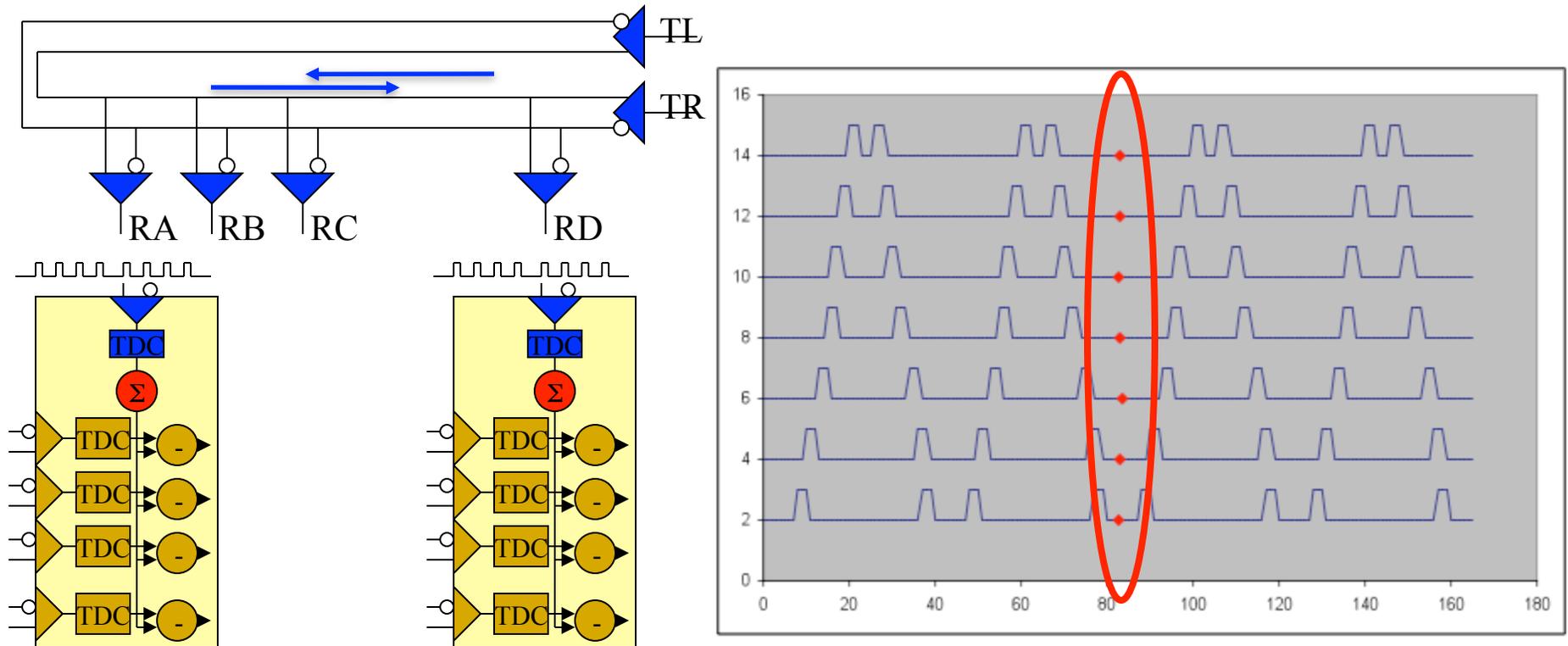
- After the first transition arrives, the integrator is charged with 1 unit current I .
- After the returning transition, the charging current is $2 \cdot I$.
- The output flips after a constant delay from the mean time.
- Analog noise etc. affects timing precision.

The Digital Mean Timing Scheme



- The left and right end drivers are alternatively enabled and drive pulses to travel from left or right end.
- The receivers on each TDC FPGA receive the pulses each delayed from left and right path.
- The arrival times at different TDC modules are different, but the **mean times** of the pulses are the same.
- **No requirement of using high quality cable.**

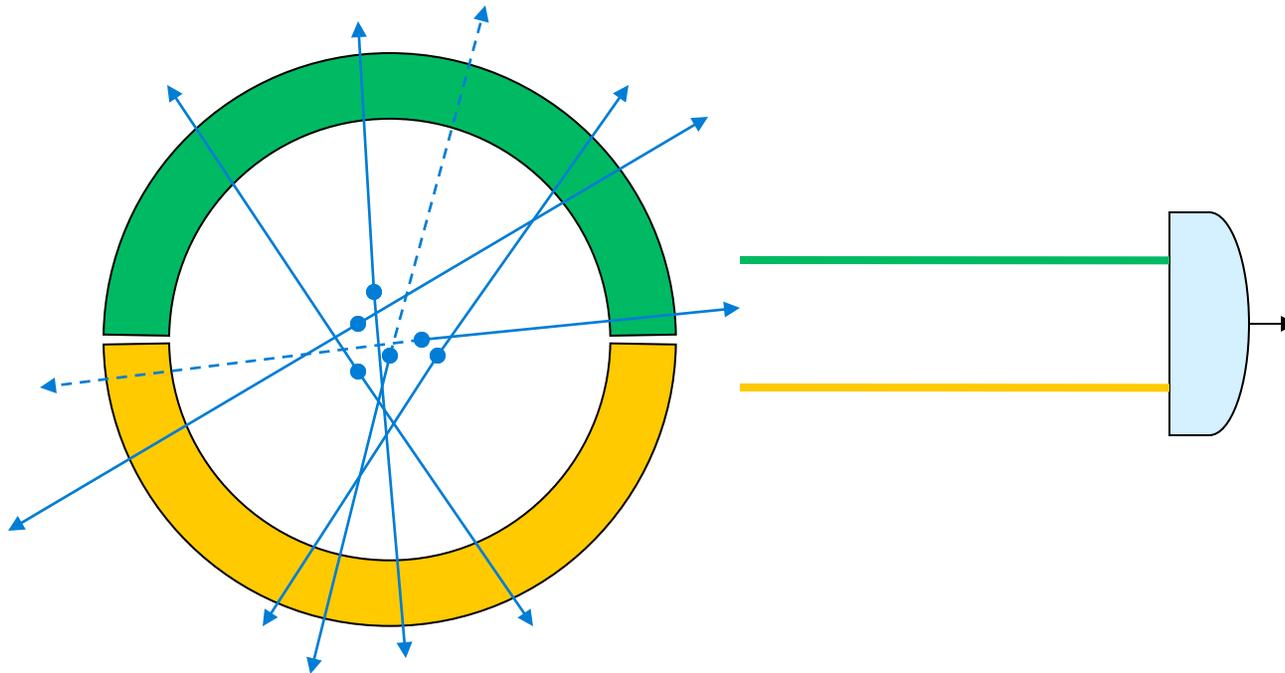
The Digital Mean Timing with Multi Pulses



- The mean timing burst has 8 pulses and the left and right end drivers are alternatively enabled and drive pulses to travel from left or right end.
- The receivers on each TDC FPGA receive the burst with 4 pulses each delayed from left and right path.
- The arrival times at different TDC modules are different, but the **mean times** of the 8 pulses as indicated with the red dots are the same.
- **Better timing precision is anticipated due to averaging of multiple measurements.**

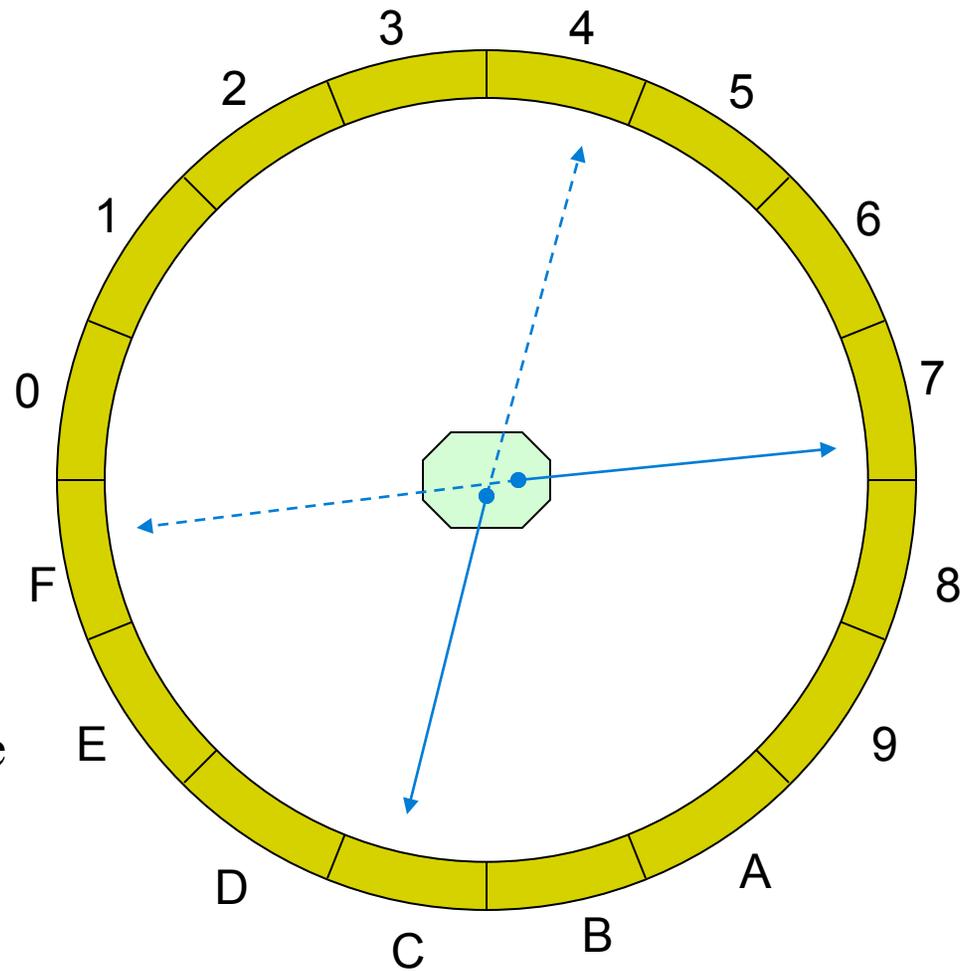
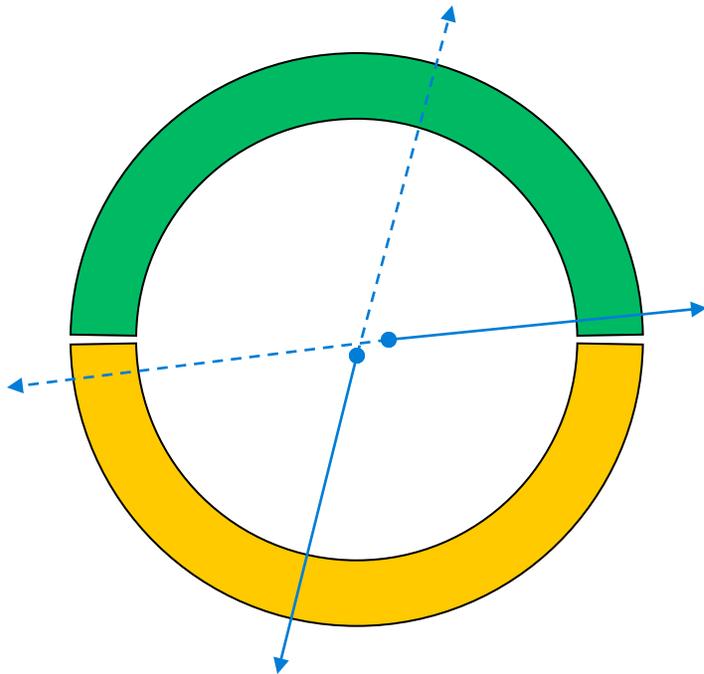
Coincidence Trigger (Trigger ~ Data Selection)

Coincidence in PET



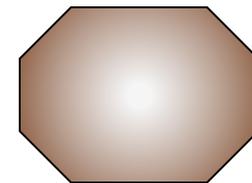
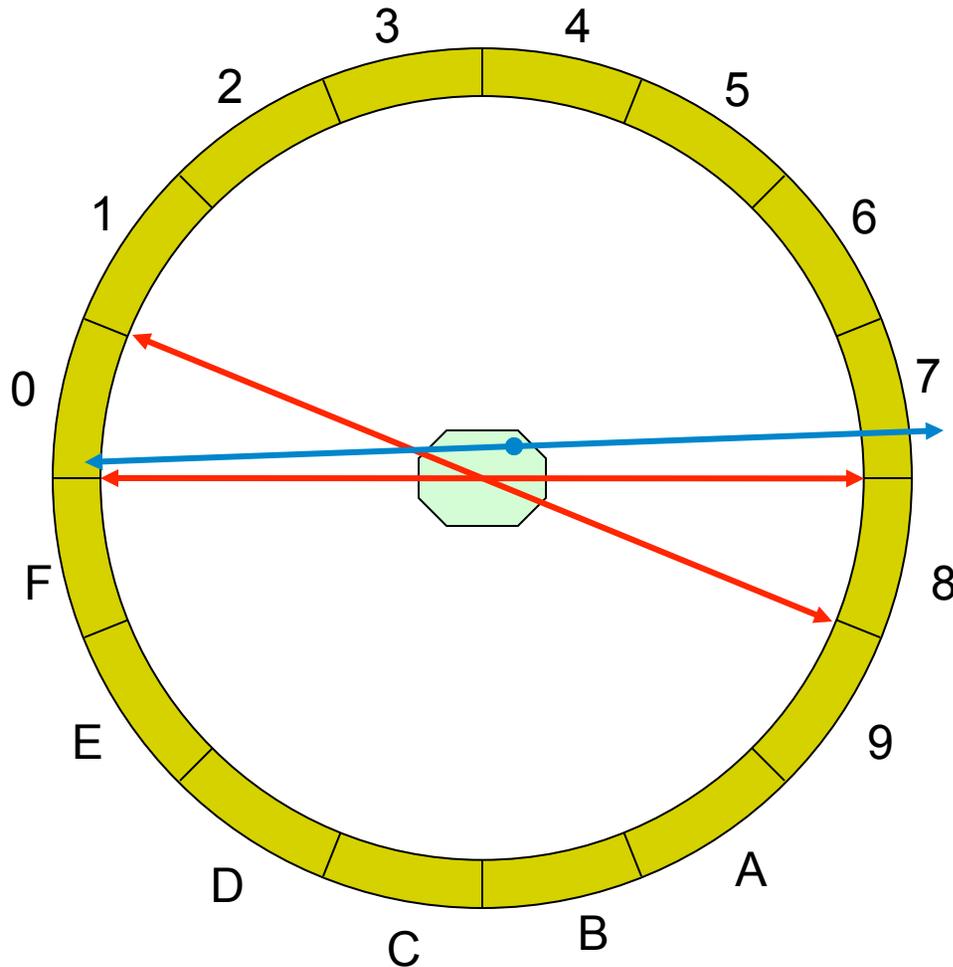
- Positrons and electrons annihilate to produce pairs of photons. The back-to-back photons hit the detector at nearly the same time.
- The data are selected only when both hits are detected.

Sectioning in Space Domain



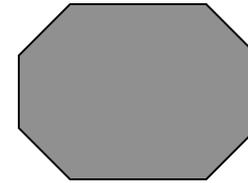
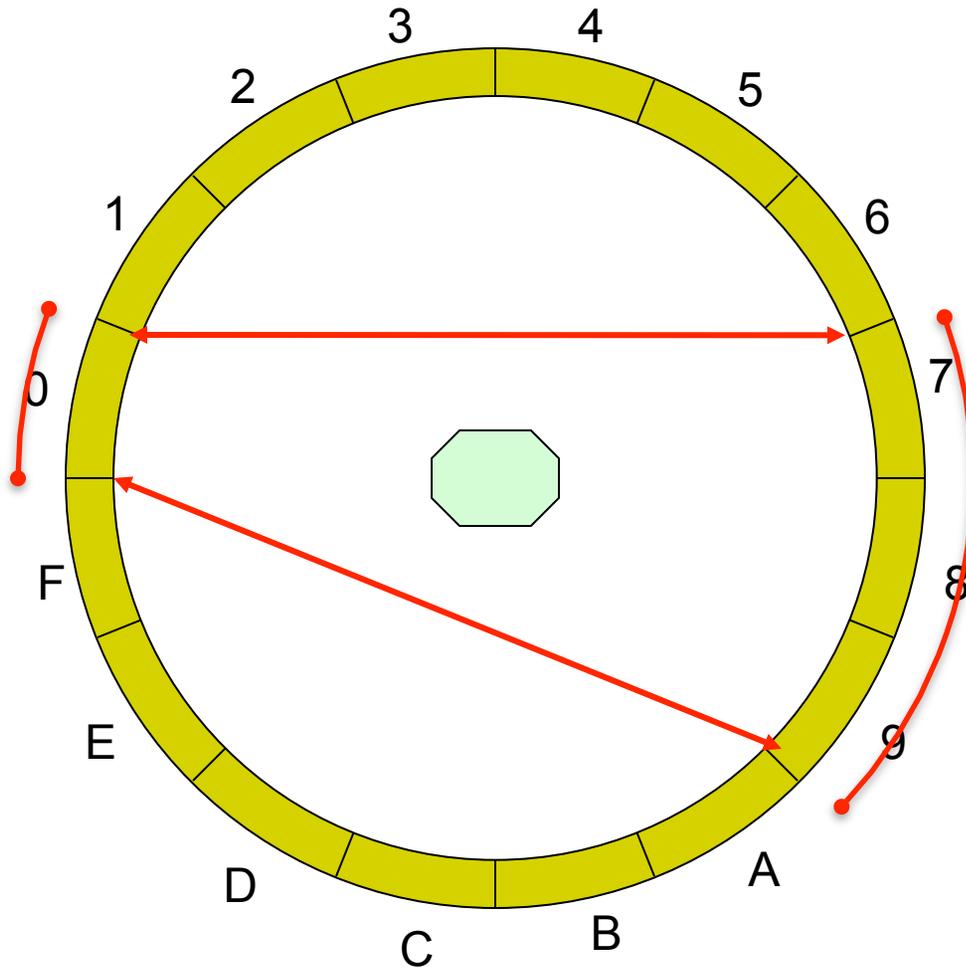
- Detector may be sectioned in space to reduce data volume.
- Fake coincidence can be avoided with appropriate sectioning.

Boundary Effect



- If coincidence is searched only between opposite sections, some valid hits will be lost.
- Artificial image brightness variation may be generated.

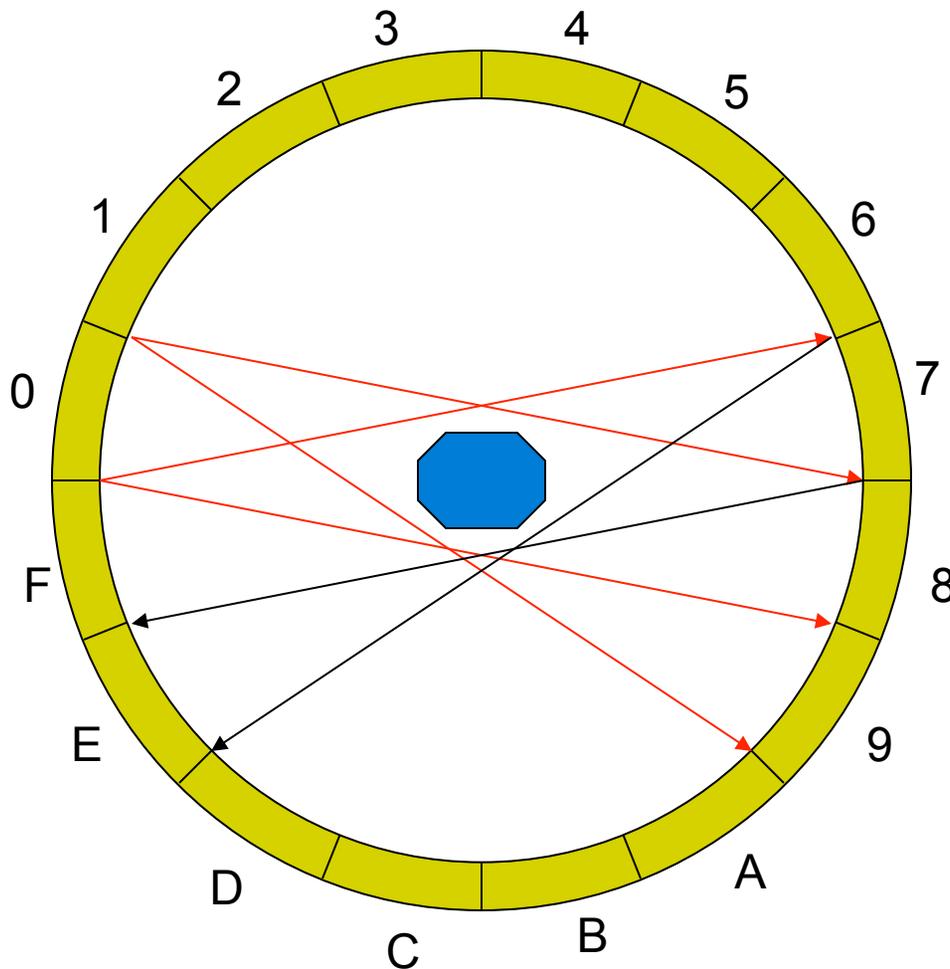
Boundary Coverage



- Coincidence is searched between opposite -1, +0 and +1 sections to include all valid hits.
- Reduce **bias** as much as possible.

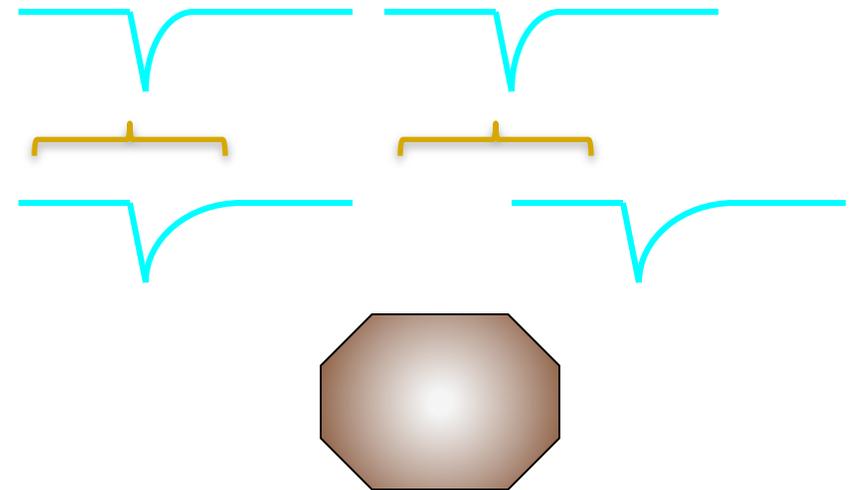
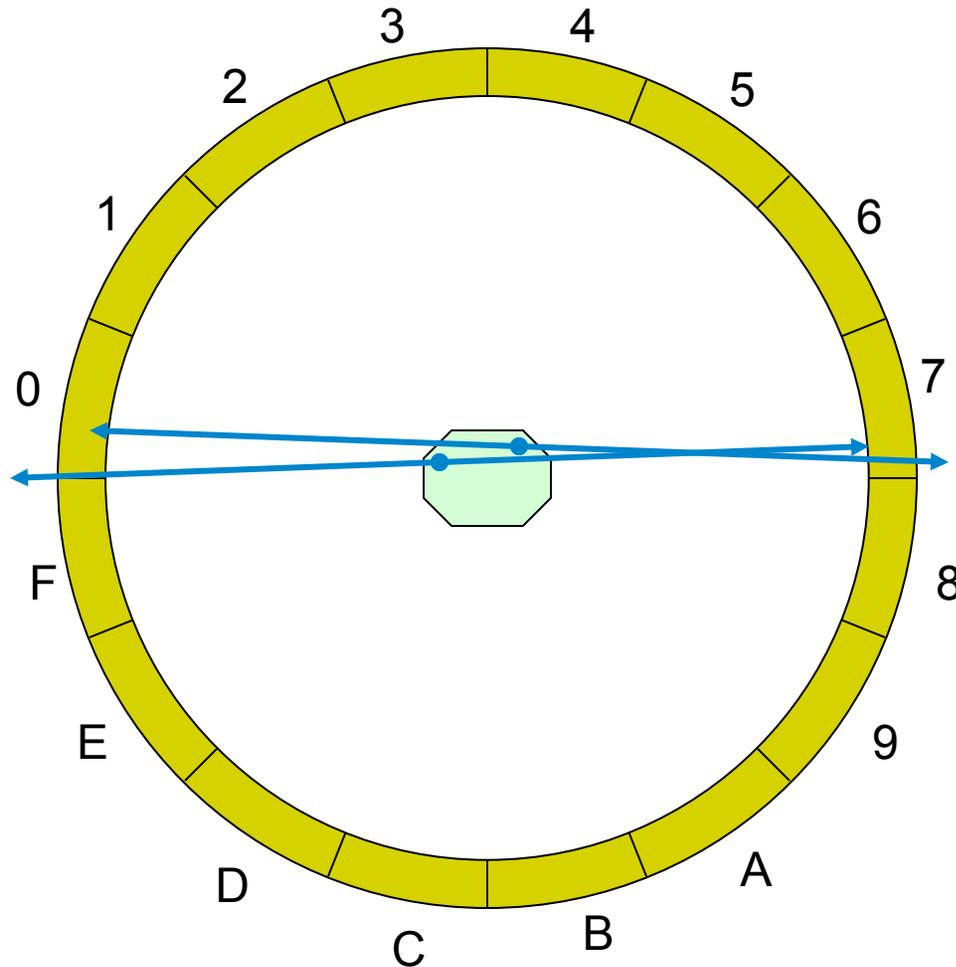
Avoiding Duplicated Coincidence Pairs

- If two hits A & B exist within time window and opposite ± 1 sectors from each other, they will be found twice, i.e., (A,B) and (B,A) when A and B are used as “seed”, respectively.
- To eliminate duplicated pairs, only hits on the sections 0-8 of the detector are used as seed.
 - This way, pairs will only be found once.
 - For seeds in section 7 and 8, some combinations are denoted as invalid using “ $\langle \rangle$ ” to avoid duplicate coincidence.



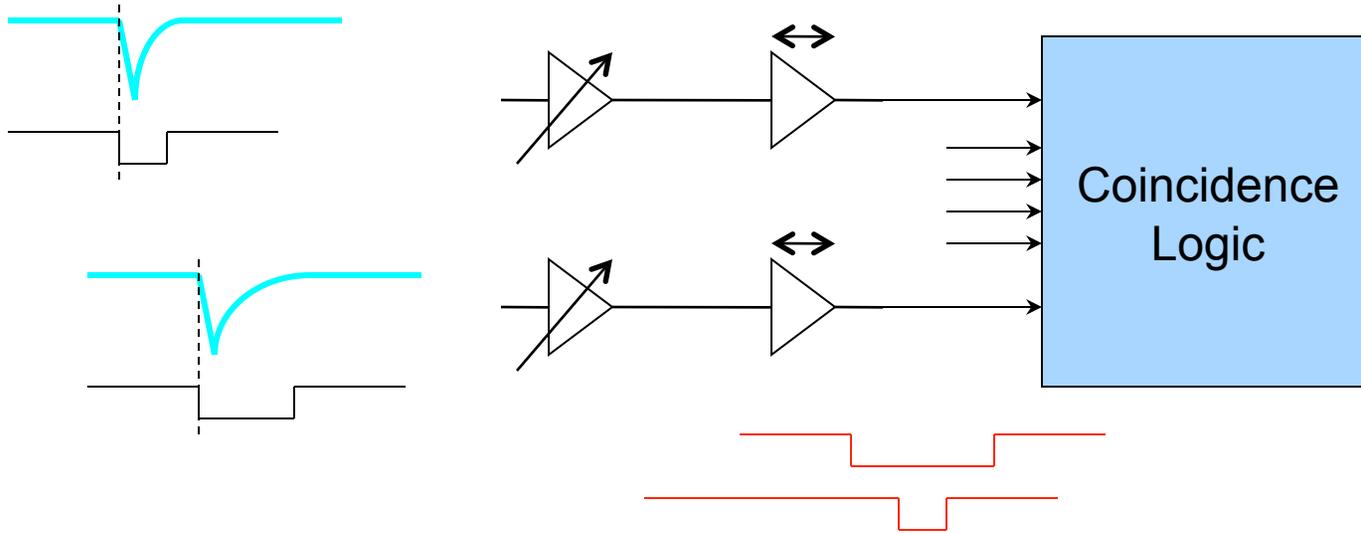
Seeds in Sector	Opposite -1	Opposite	Opposite +1
0	7	8	9
1	8	9	A
2	9	A	B
3	A	B	C
4	B	C	D
5	C	D	E
6	D	E	F
7	E	F	$\langle 0 \rangle$
8	F	$\langle 0 \rangle$	$\langle 1 \rangle$

Timing Window

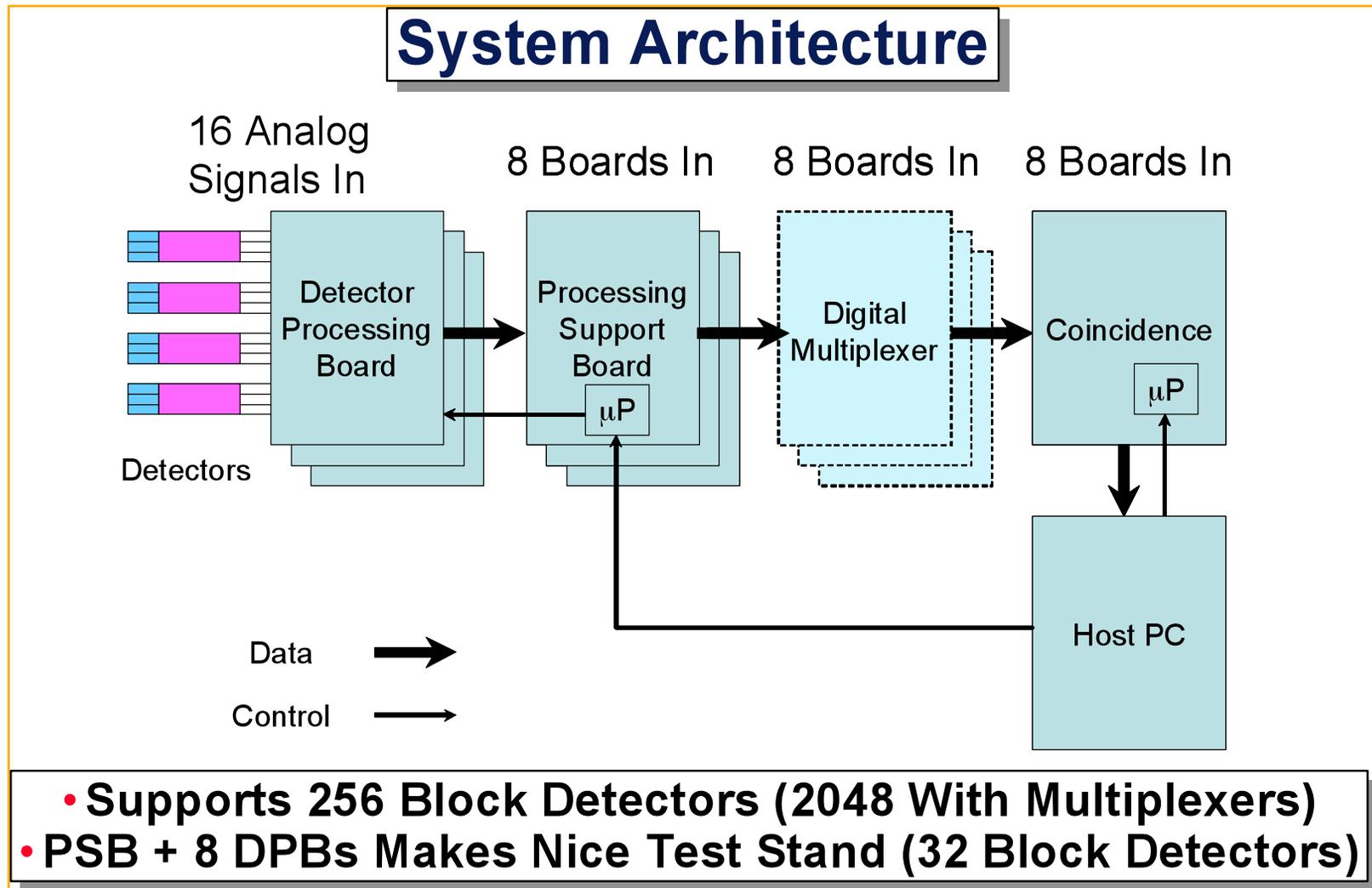


- The timing window can not be too narrow or it may cause artificial image brightness variation.
- The timing window can not be too wide either since it may bring in fake coincidence.

Analog Method of Timing Adjustment

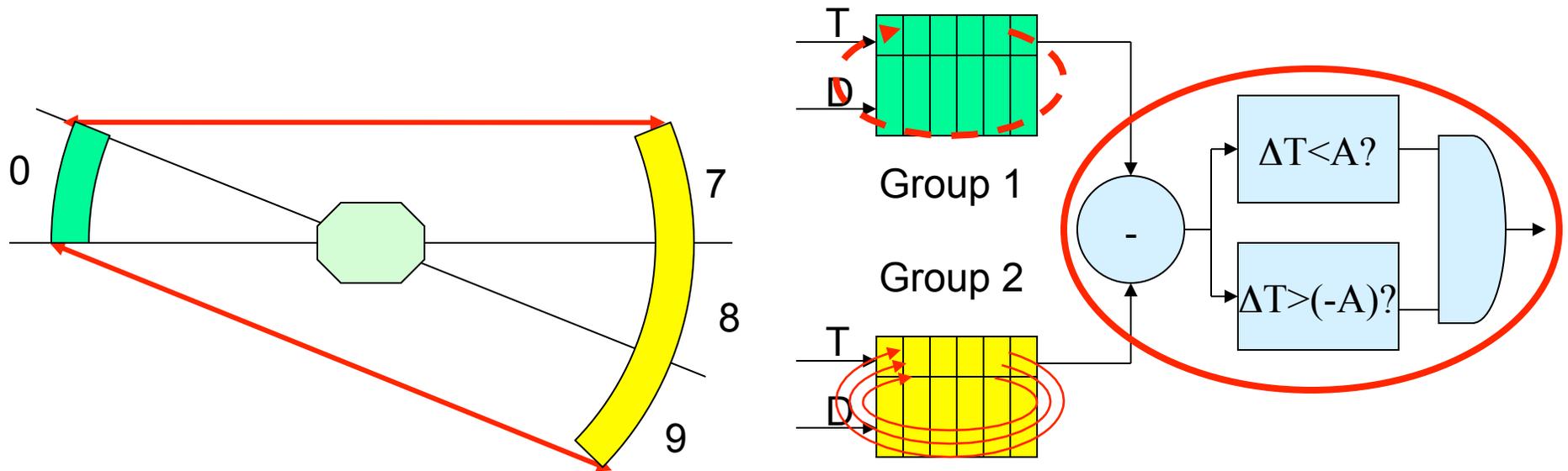


The Full Data Coincidence Approach



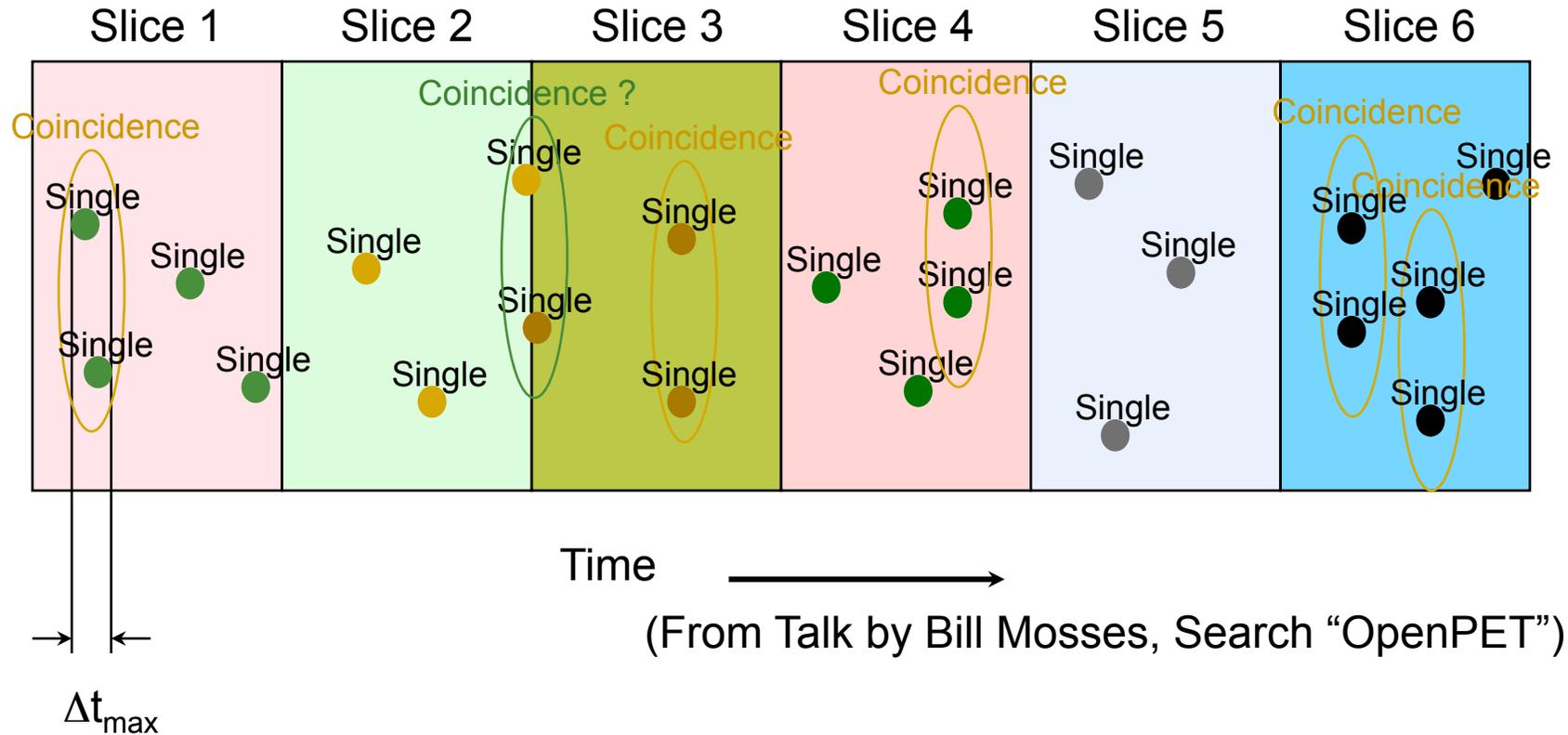
(From Talk by Bill Mosses)

Complexity of Doublet Matching



- Detector hits are digitized and hits at nearly the same time are to be matched together.
- The process takes $O(n^2)$ clock cycles.
- For example, if there 1000 hits in Group 1 and 3000 hits in Group 2, there are 3,000,000 combinations to check.

Identifying Time Coincidences



- Break Time Into Slices (100–250 ns / slice)
- Search for Singles Within Δt_{\max} (4–12 ns) in Each Slice
 - *Greatly* Reduces Combinatory

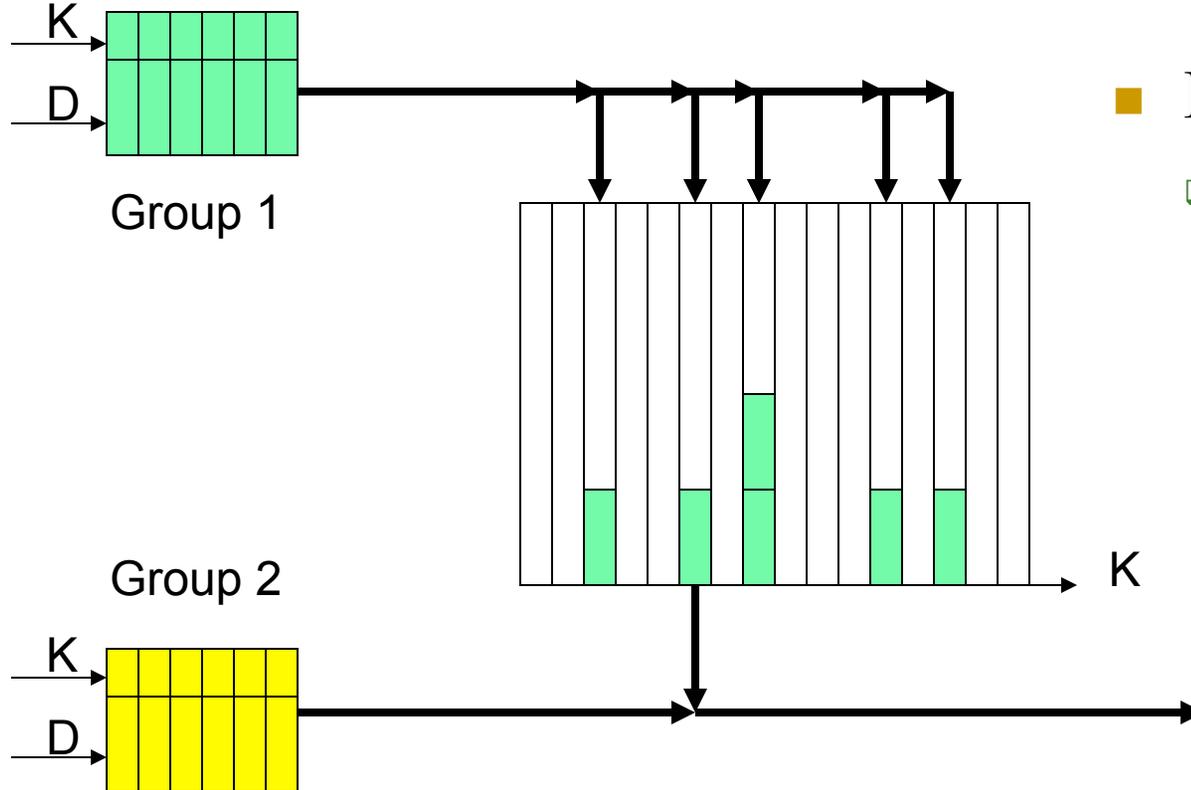
Slicing

	Group 1 Hits/slice	Group 2 Hits/slice	Combinations	Reduction
Total	1000	3000	$1000*3000=3,000,000$	
10 slices	100	300	$(100*300)*10=300,000$	1/10
100 slices	10	30	$(10*30)*100=30,000$	1/100
1000 slices	~1	~3	$(1*3)*1000=3,000$	1/1000

- Take the same example of 1000 hits in Group 1 and 3000 hits in Group 2.
- Total number of combinations reduces as the time slice becomes finer.

Hash Sorter: Slicing Finer and Finer

The entire pairing process takes $2n$ clock cycles, rather than n^2 clock cycles.

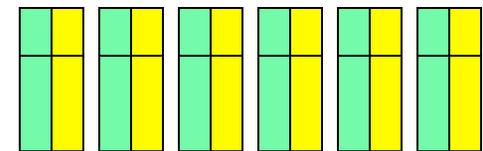


■ Pass 1:

- Data in Group 1 are stored in the hash sorter bins based on key number K .

■ Pass 2:

- Data in Group 2 are fetched though and paired up with corresponding Group 1 data with same key number K .

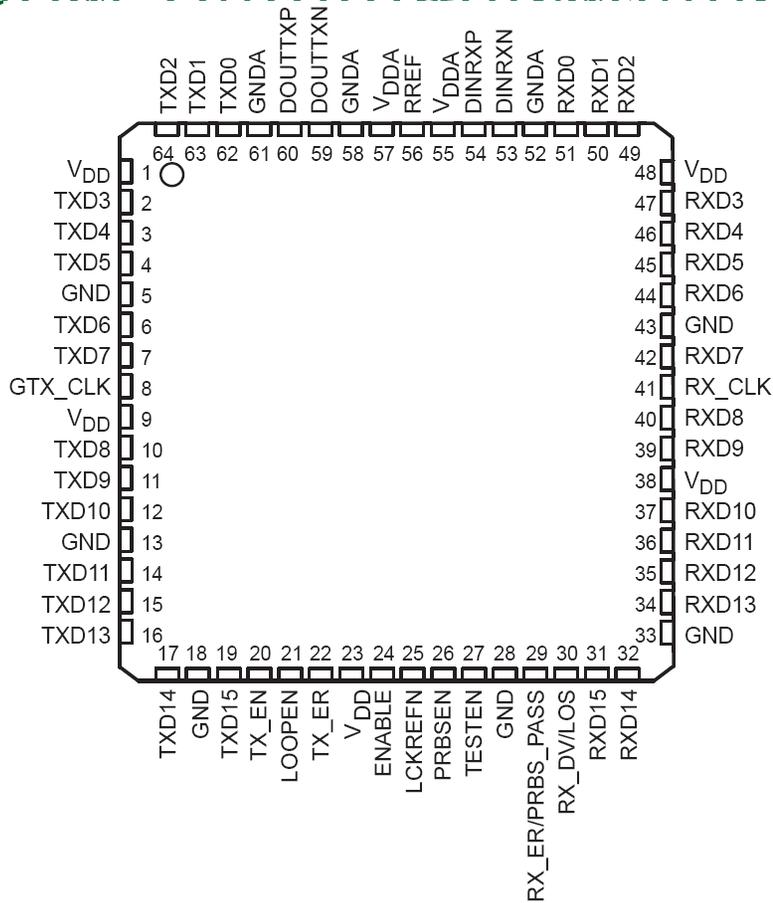


Data Communication Options

Data Communication

- Communications Between:
 - Functional blocks inside an FPGA.
 - Chips on a printed circuit board.
 - Boards in a crate.
 - Boards in different crates.
- Timing and Framing Scheme:
 - Serial Link: Timing and data are carried in the same physical channel.
 - Parallel Bus: Timing and data are carried in different physical channels.
- Physical Format:
 - Single ended: TTL, CMOS, NIM
 - Differential: LVDS, (ECL), PECL, LVPECL
 - Optical

Serial Communication: Commercial Chips



TLK2501
1.5 TO 2.5 GBPS TRANSCEIVER

SLLS427D - AUGUST 2000 - REVISED JULY 2003

block diagram

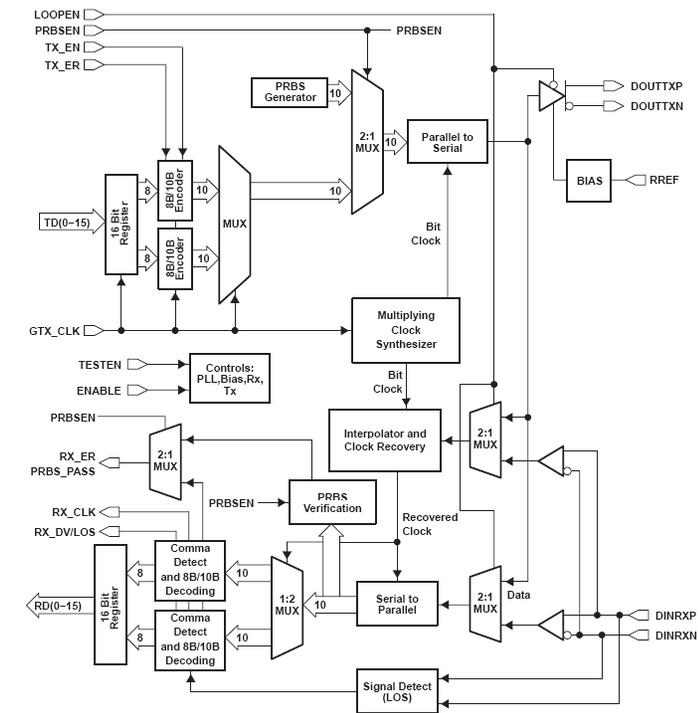
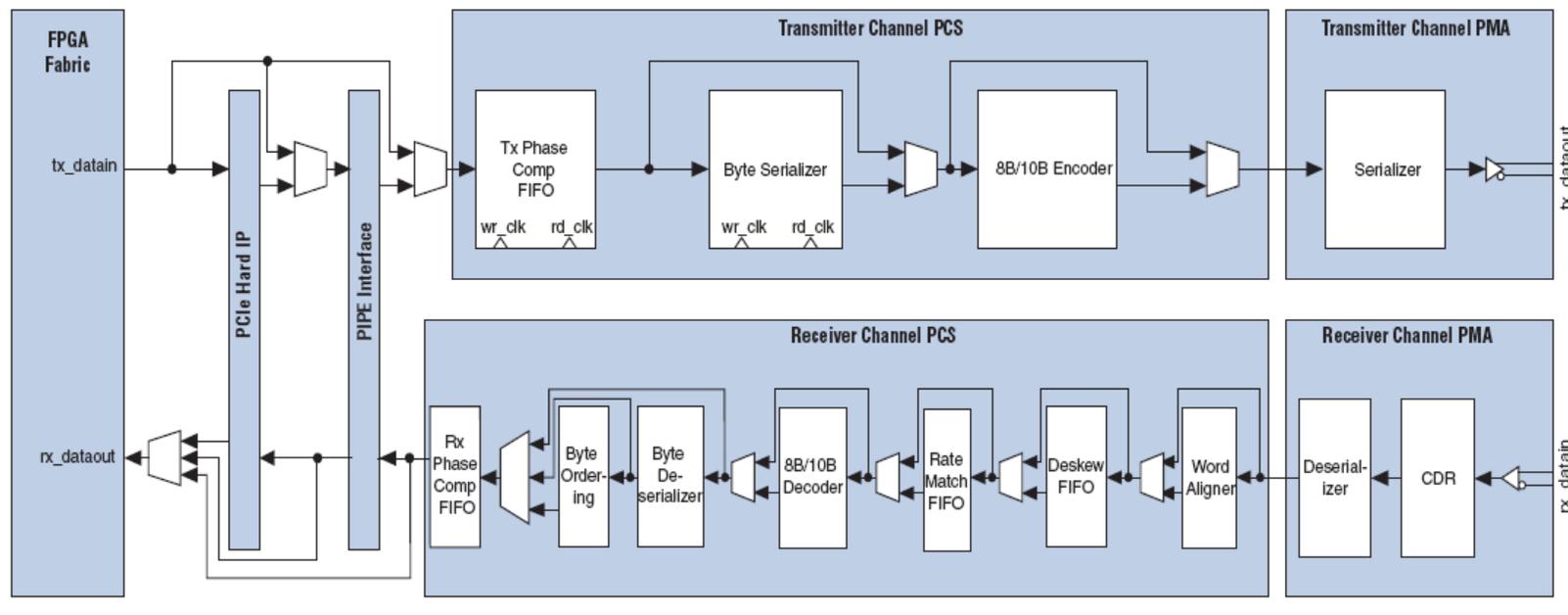


Figure 1. TLK2501 Block Diagram

- Parallel 16 bits data at 75 to 125 MHz
- Serial port at 1.5 to 2.5 GBPS.

Serial Communication: Dedicated High-Speed Transceivers inside FPGA

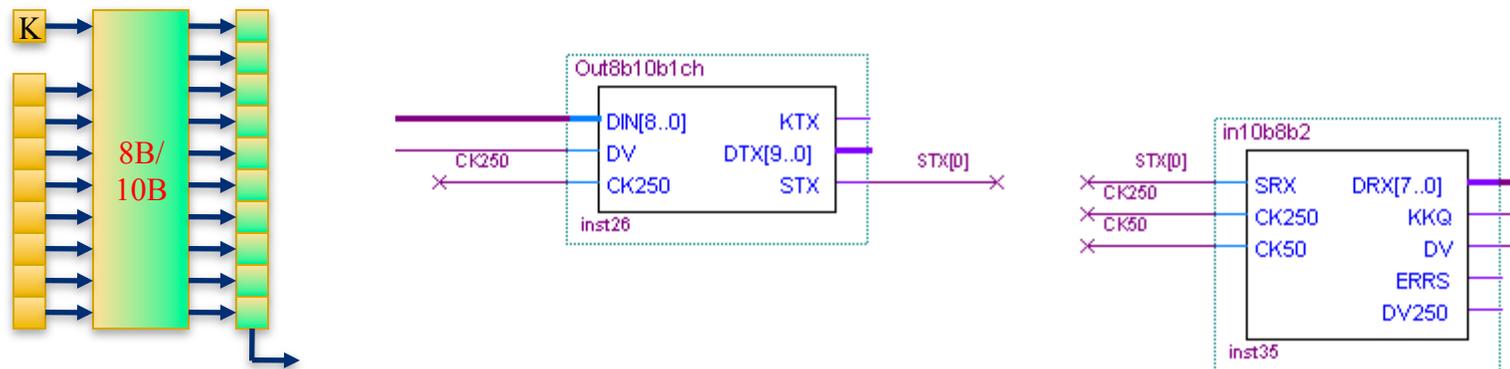
Figure 1-3. Transceiver Channel Datapath for Cyclone IV GX Devices



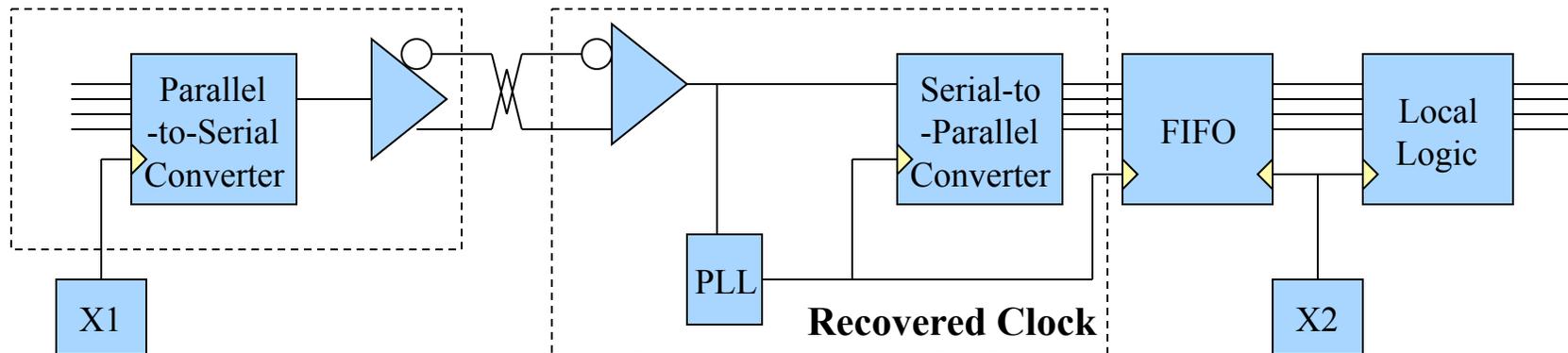
- Parallel data interfacing internally in FPGA
- Serial port up to 3.125 GBPS for external communications.
- Limited number of ports ☹ Higher cost ☹

8B/10B Standard

- Parallel 8-bit input data are broken into 3-bit + 5-bit sections.
- Conversions 3b/4b and 5b/6b are performed to create 10-bit data.
- The 10-bit sequences are **DC balanced** so that it can be transmitted communication channels with AC coupling (such as transformer) and optical fibers.
- Most of bit sequence has <5 continuous 0's or 1's.
- Bit sequences 0011111, or 1100000 in the “comma symbols” K28.1, K28.5 and K28.7 are used for synchronization.

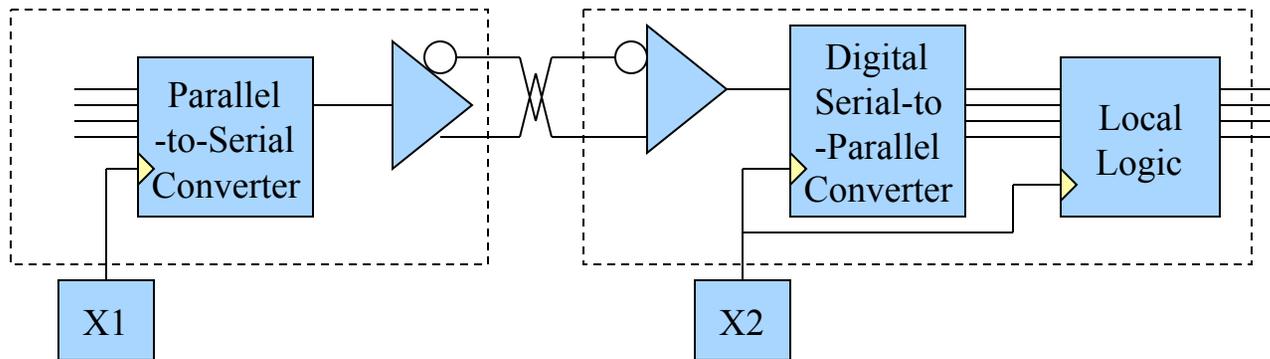


Classical Picture of Serial Communications



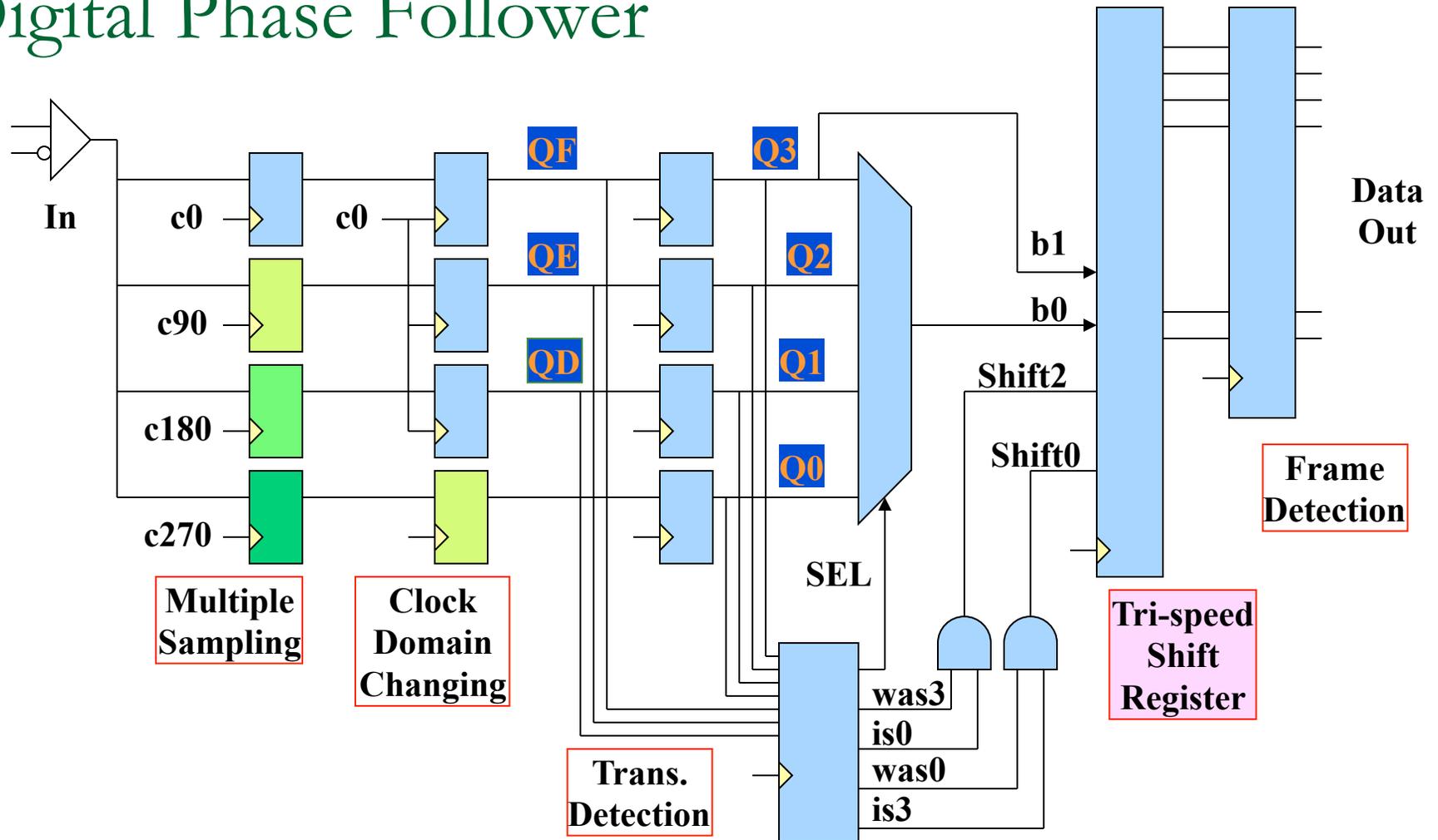
- The parallel data is converted to serial bits driven by crystal oscillator X1 in the transmitter device.
- The serial data stream is used to generate a recovered clock at the receiver device with a phase lock loop (PLL).
- The recovered clock is used to drive the serial-to-parallel converter and store the data into a first-in-first-out (FIFO) buffer.
- The FIFO buffer is used to transfer data from the recovered clock domain to the local clock domain generated by crystal oscillator X2.

Serial Data Receiving Without PLL etc.



- Generating recovered clock with PLL, VCO, VCXO etc. is an analog process and it is not convenient to generate in an FPGA, especially for applications with multiple receiving channels.
- There are pure digital methods to receive the serial data.
 - Digital Phase Follower: 1bit/CLK *See*
 - The Two-Cycle Serial IO: 1bit/(2CLK) *Backup Slides*
 - FM Encoder and Decoder: 1bit/(2-16CLK)
 - Clock-Command Combined Carrier Coding (C5): 4bits/(20CLK)
- The transmitter and receiver can be driven by two independent free running crystal oscillators.

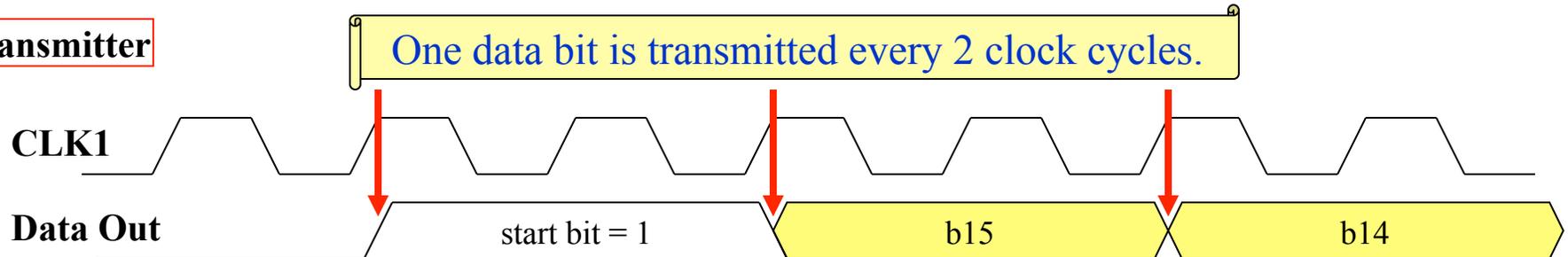
Digital Phase Follower



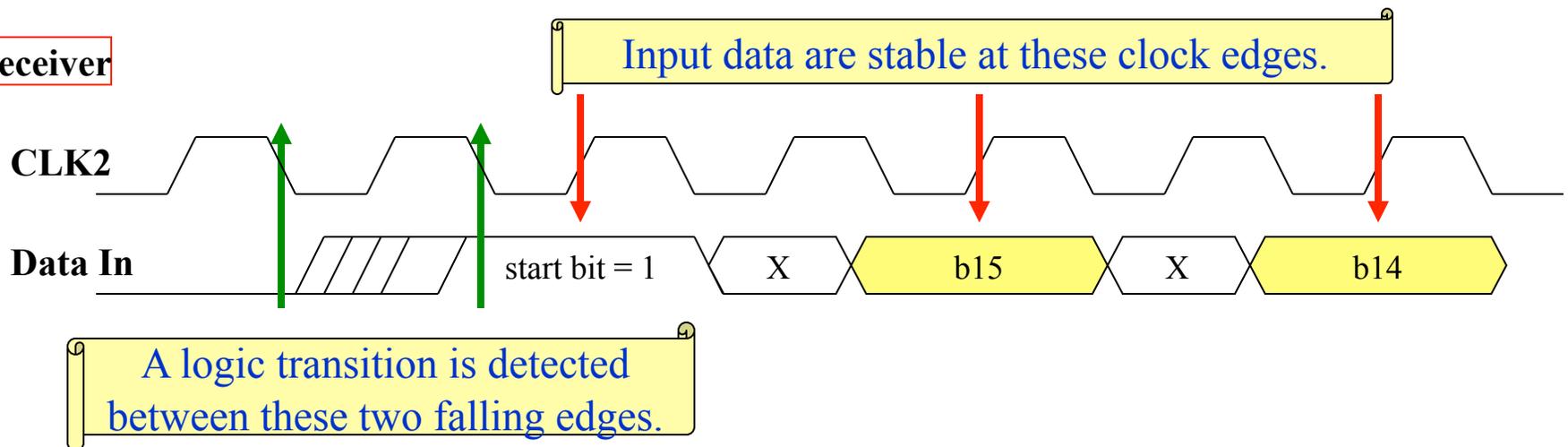
- The input data rate is 1bit/clock cycle.
- Four clock phases, c0, c90, c180 and c270 are used to detect input transition edge.
- The phase for data sample follows the variation of the transition edge.

The Two-Cycle Serial IO

Transmitter

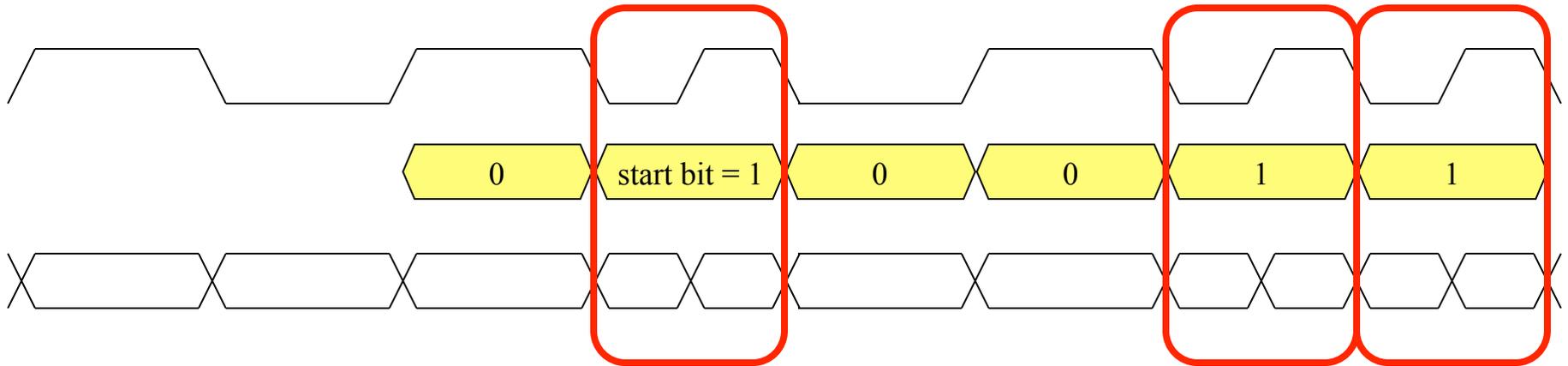


Receiver

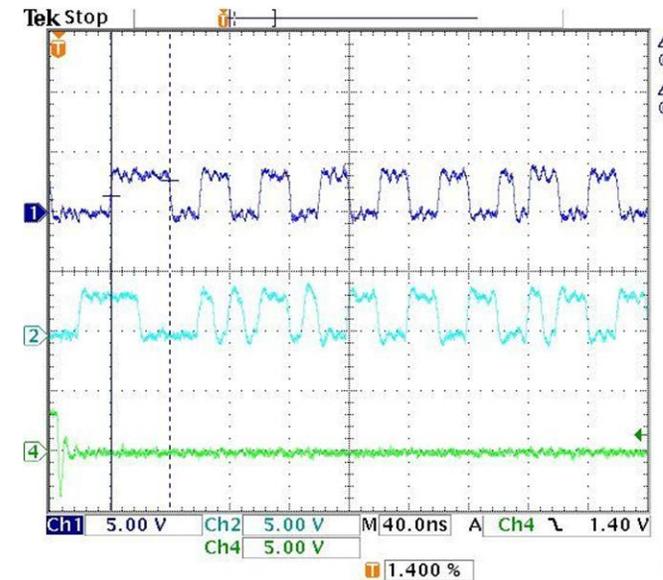


- This scheme is slower than digital phase follower but the logic is simpler.
- The CLK1 and CLK2 can be generated with two free running crystal oscillators.

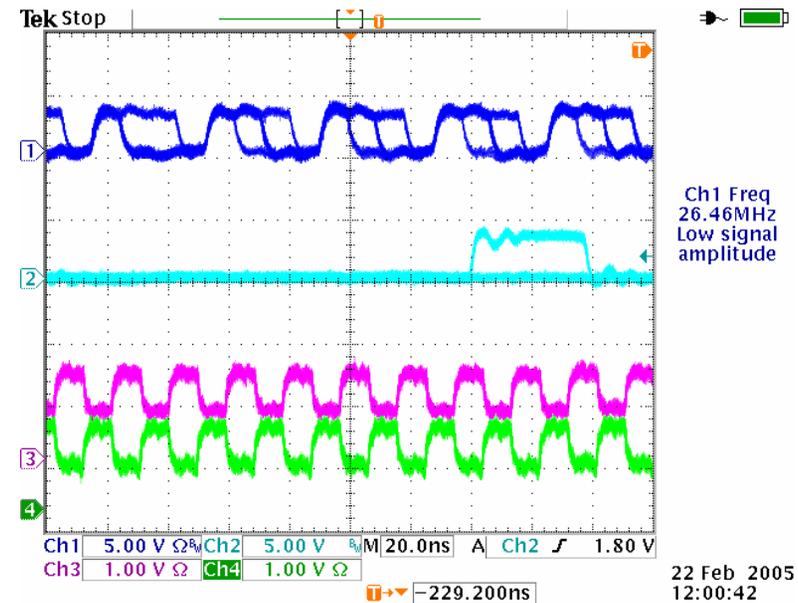
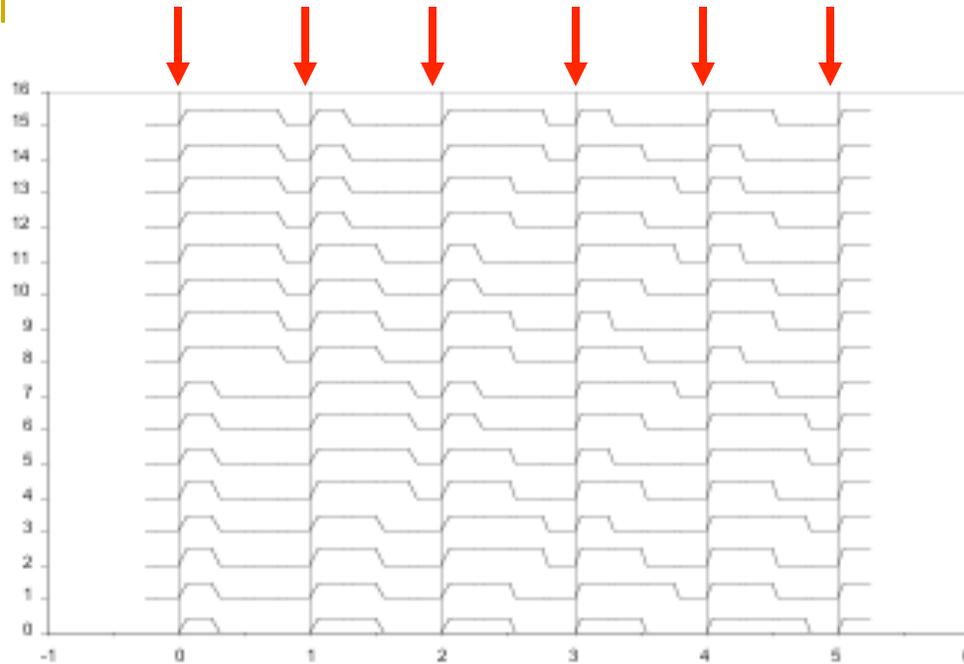
The FM coding



- A bit is transmitted in two unit time intervals, usually in two internal clock cycles at frequency f .
- For bit=1, the output toggles each cycle, i.e., with frequency $(f/2)$ and for bit=0, the output toggles every two cycles, i.e., with frequency $(f/4)$.
- When not transmitting data, the output toggles at frequency $(f/4)$, until seeing the start bit.
- The data stream is naturally DC balanced suitable for AC coupled transmission.
- The polarity of the interconnection doesn't matter.



The Clock-Command Combined Carrier Coding (C5)



- A data train contains 5 pulses and each pulse is transmitted in four unit time intervals, usually in four internal clock cycles at frequency f .
- Information is carried with wide, normal and narrow pulses and the first pulse is always wide or narrow.
- When not transmitting data, all pulses have normal width.
- The data stream is DC balanced over 5 pulses suitable for AC coupled transmission.
- All leading edges are evenly spread so that the pulse train can be used directly drive the receiver side logic or PLL.

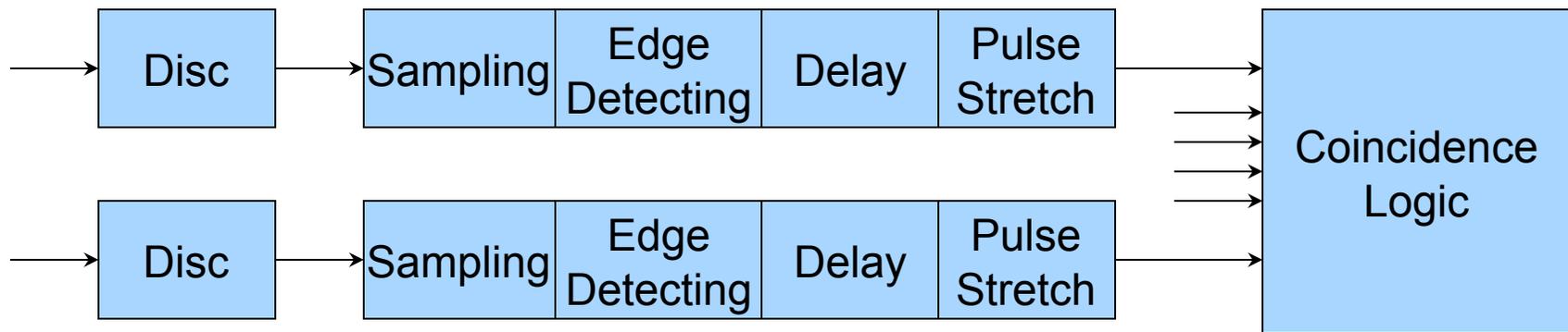
Conclusion

- Clock
- Timing
- Trigger
- Serial Communication

An aerial photograph of a golf course. The course is a large, winding green with several holes and sand traps. In the center-right, there is a clubhouse building with a distinctive white, curved roof. To the left of the clubhouse, a tall, white water tower stands prominently. The surrounding area includes fields, trees, and some residential or commercial buildings in the distance. The text "The End" is overlaid in a blue box in the top left, and "Thanks" is overlaid in a blue box in the middle left.

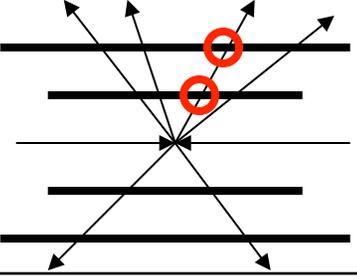
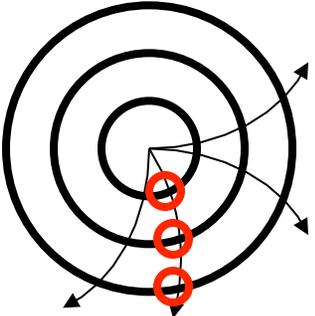
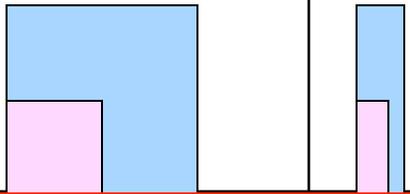
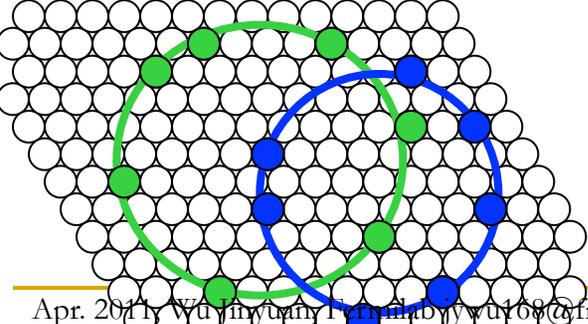
The End

Thanks

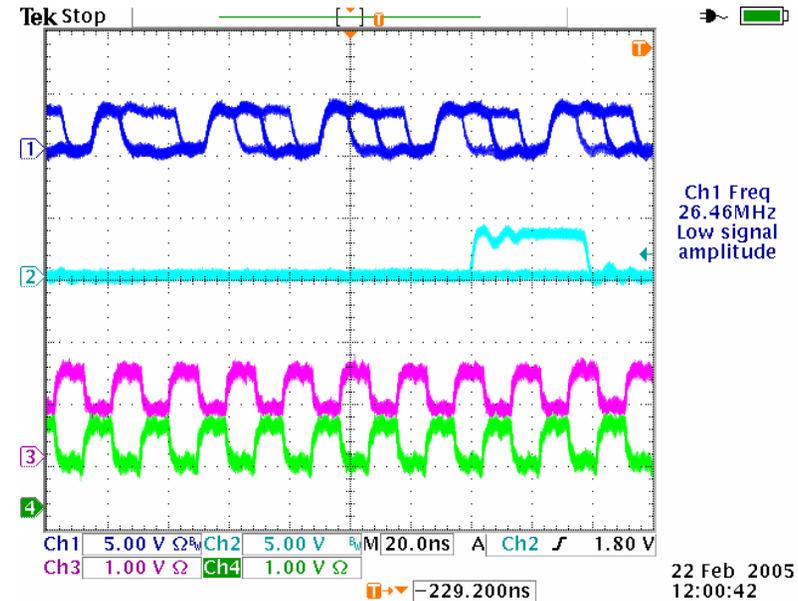
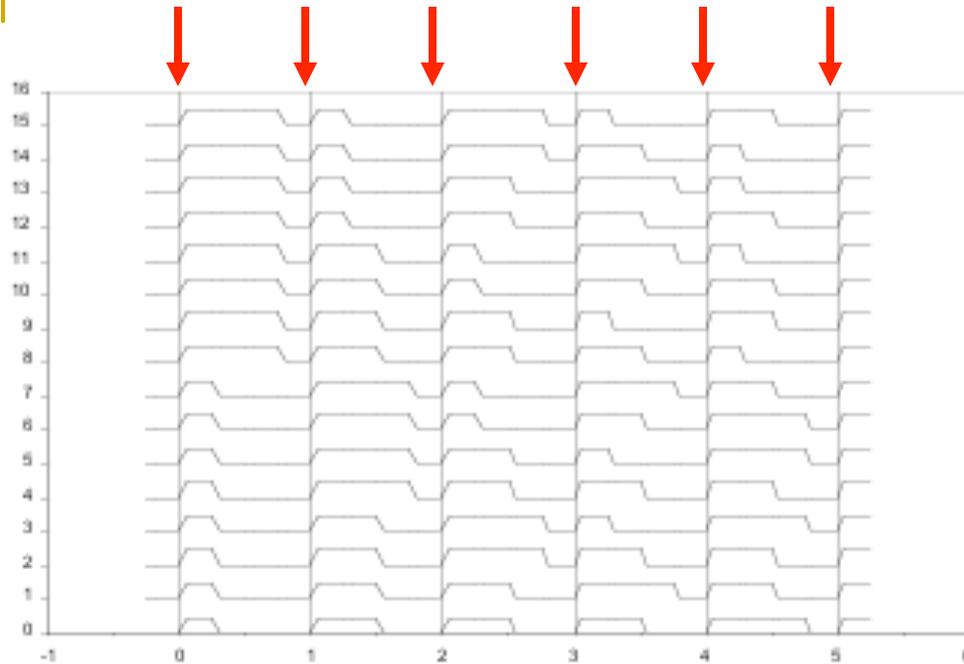


Doublet Finding in Trigger System

Hit Matching

	Software	FPGA Typical	FPGA Resource Saving Approaches
	$O(n^2)$ <pre>for(){ for(){...} }</pre>	$O(n)*O(N)$ Comparator Array	Hash Sorter $O(n)*O(N)$: in RAM
	$O(n^3)$ <pre>for(){ for(){ for(){...} } }</pre>	$O(n)*O(N^2)$ CAM, Hugh Trans. 	Tiny Triplet Finder $O(n)*O(N*\log N)$
	$O(n^4)$ <pre>for(){ for(){ for(){ for() {...} }}} }</pre>		

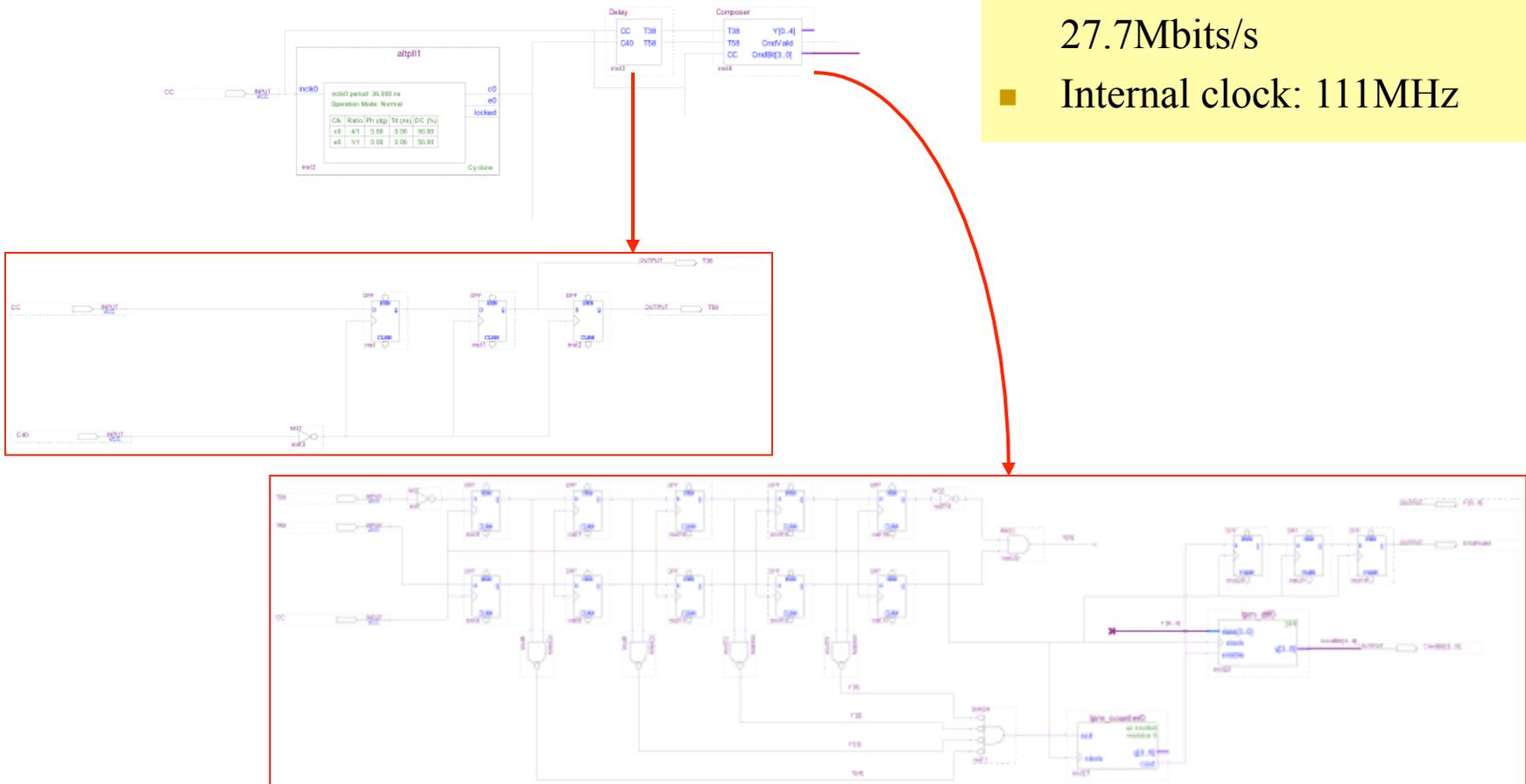
The Clock-Command Combined Carrier Coding (C5)



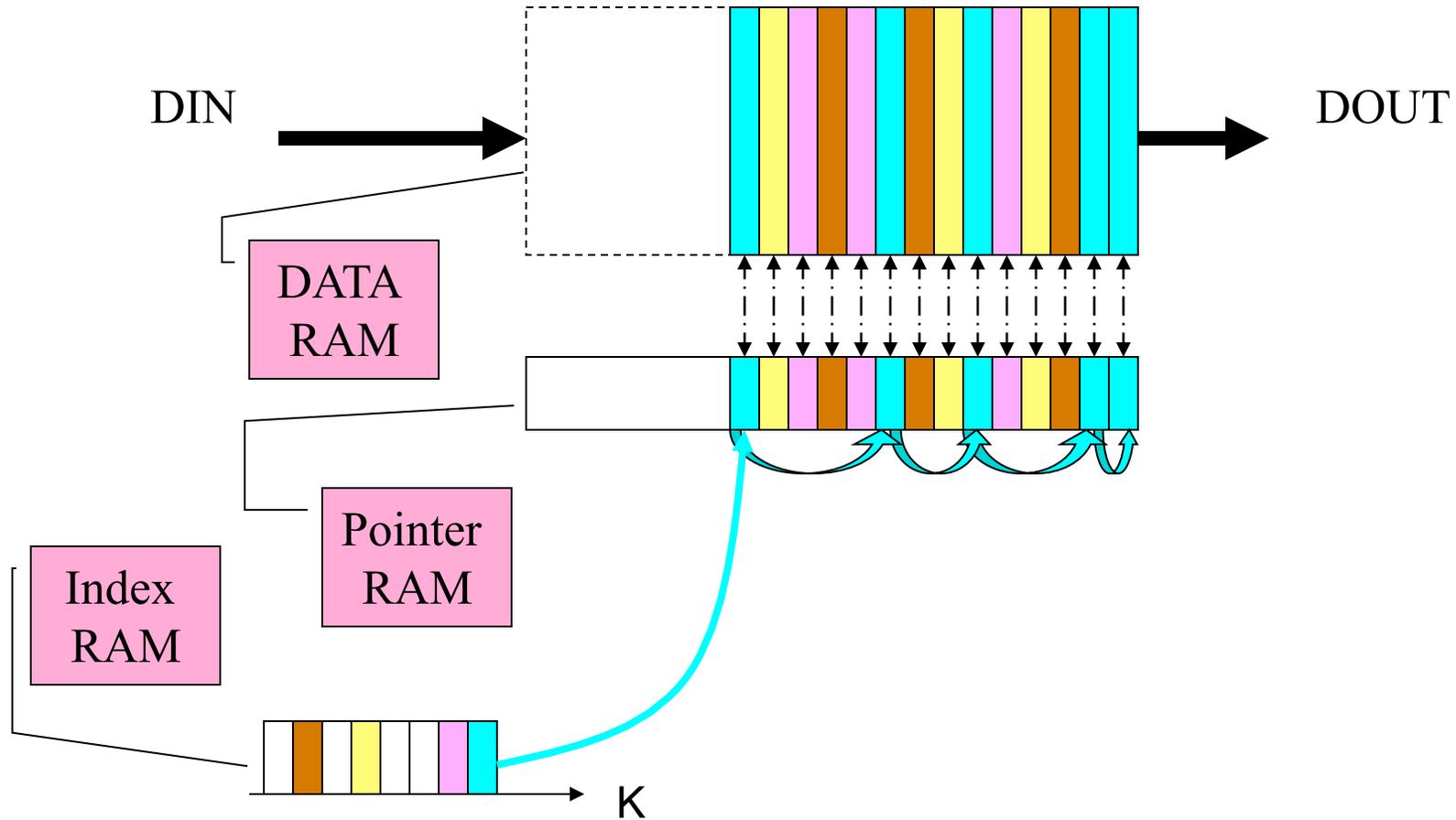
- A data train contains 5 pulses and each pulse is transmitted in four unit time intervals, usually in four internal clock cycles at frequency f .
- Information is carried with wide, normal and narrow pulses and the first pulse is always wide or narrow.
- When not transmitting data, all pulses have normal width.
- The data stream is DC balanced over 5 pulses suitable for AC coupled transmission.
- All leading edges are evenly spread so that the pulse train can be used directly drive the receiver side logic or PLL.

Schematics of C5 Decoder

- Data Rate: 36ns/bit or 27.7Mbits/s
- Internal clock: 111MHz

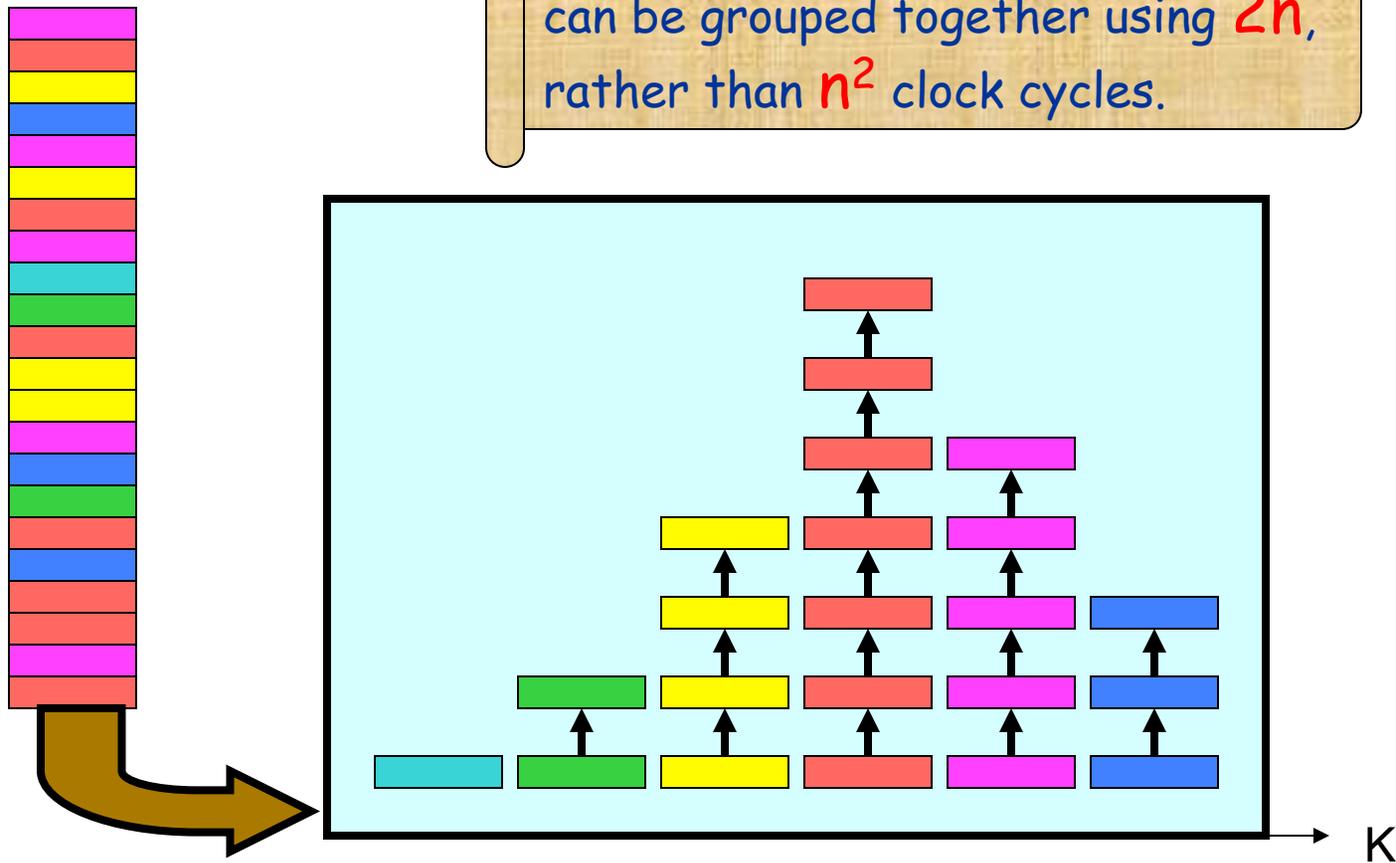


Link List Structure of Hash Sorter



Hash Sorter

Using hash sorter, matching pairs can be grouped together using $2n$, rather than n^2 clock cycles.

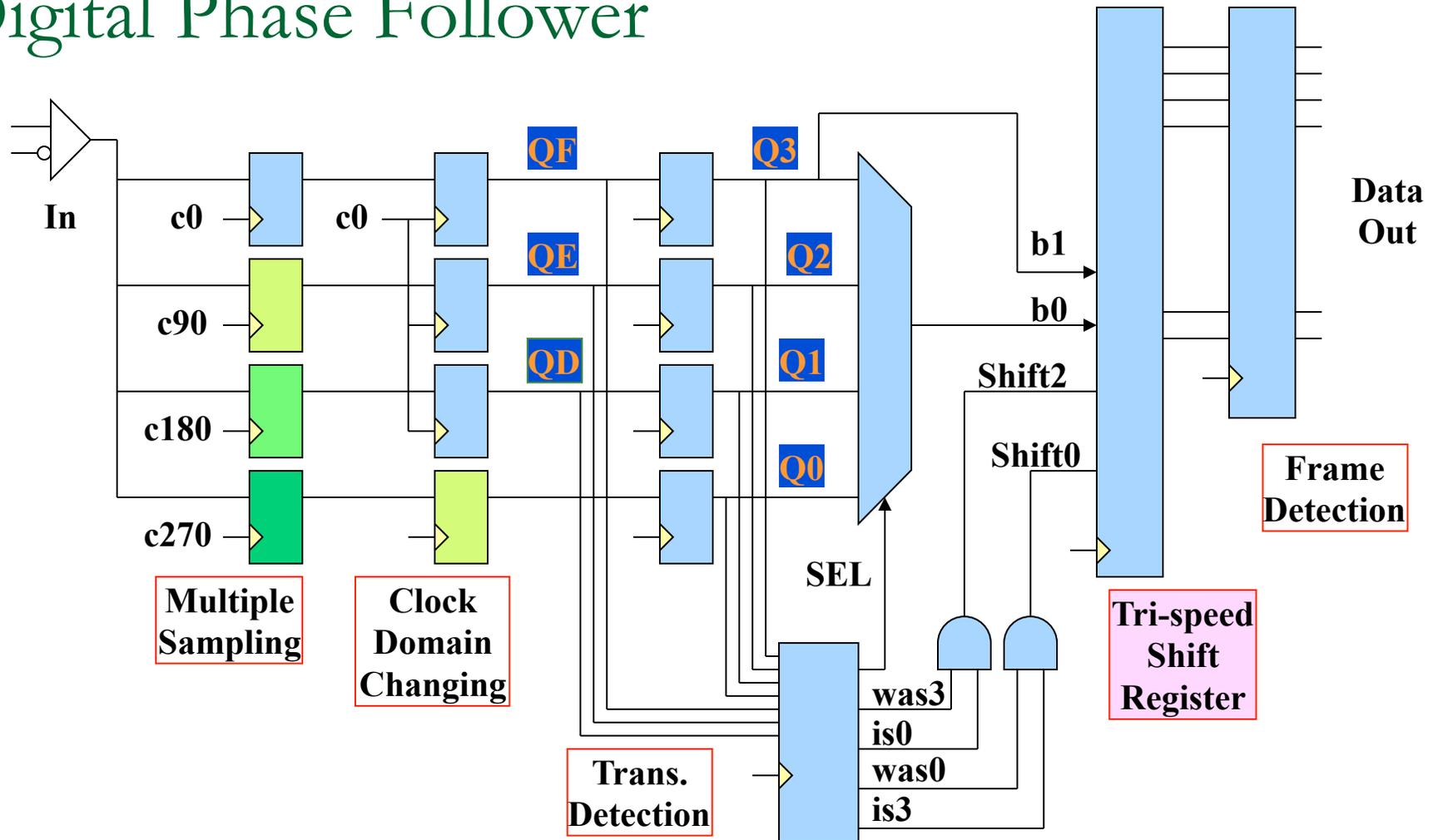


Delay Line Based TDC Architectures

	Delay Hit	Delay CLK	Delay Both
CLK is used as clock			
HIT is used as clock			

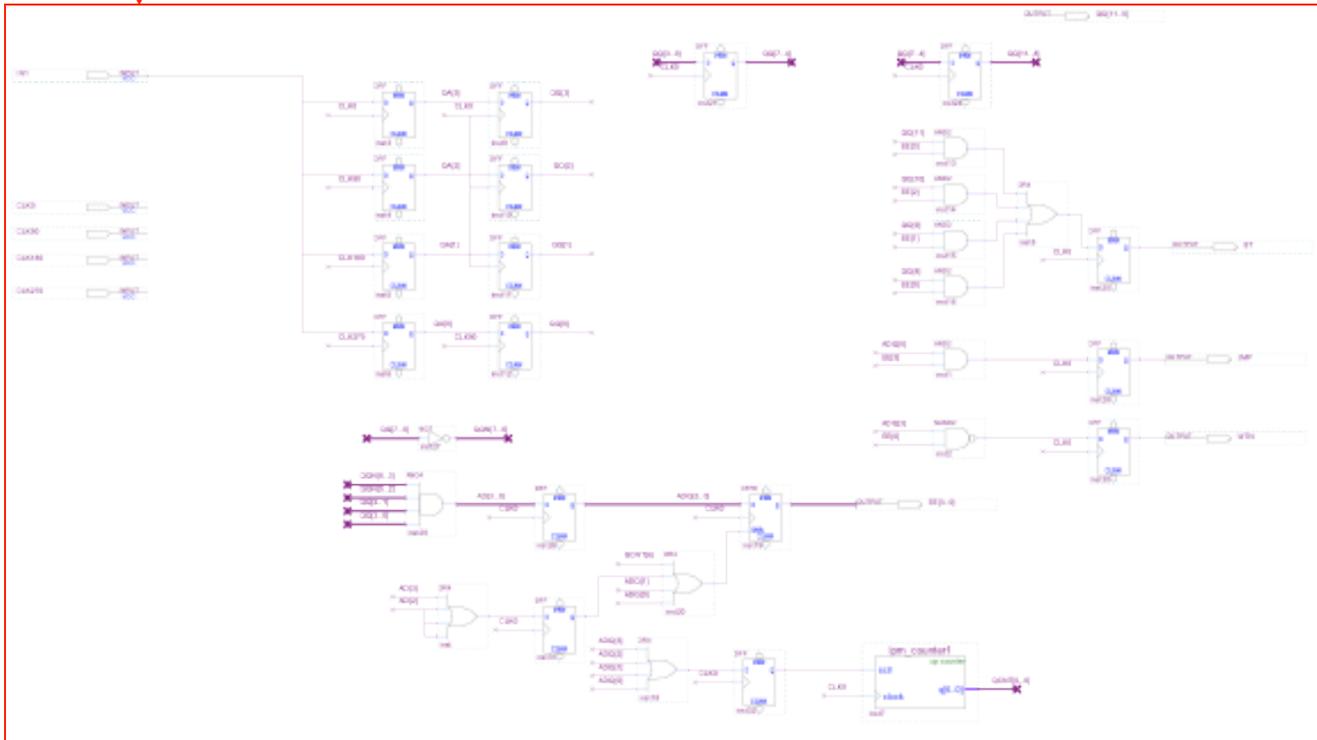
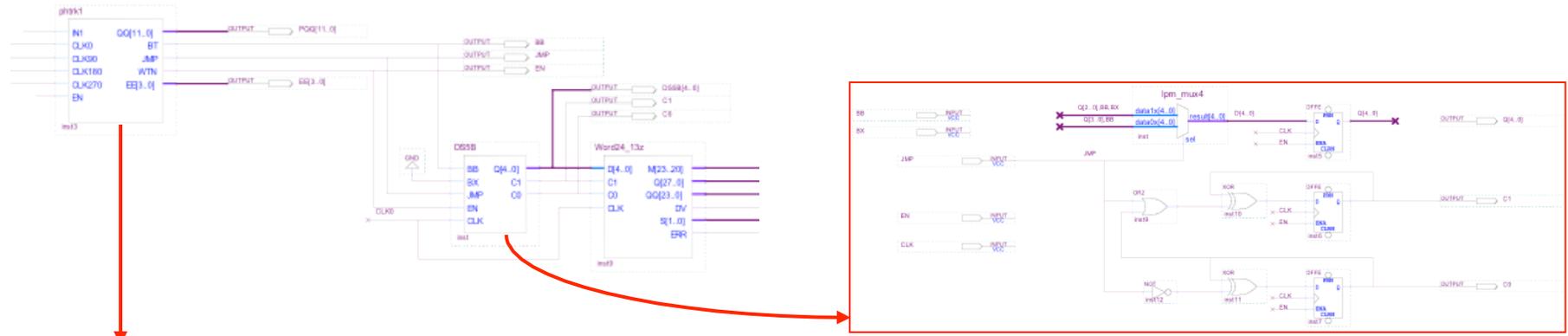
Only this architecture needs dual coarse time counters.

Digital Phase Follower



- The input data rate is 1bit/clock cycle.
- Four clock phases, c0, c90, c180 and c270 are used to detect input transition edge.
- The phase for data sample follows the variation of the transition edge.

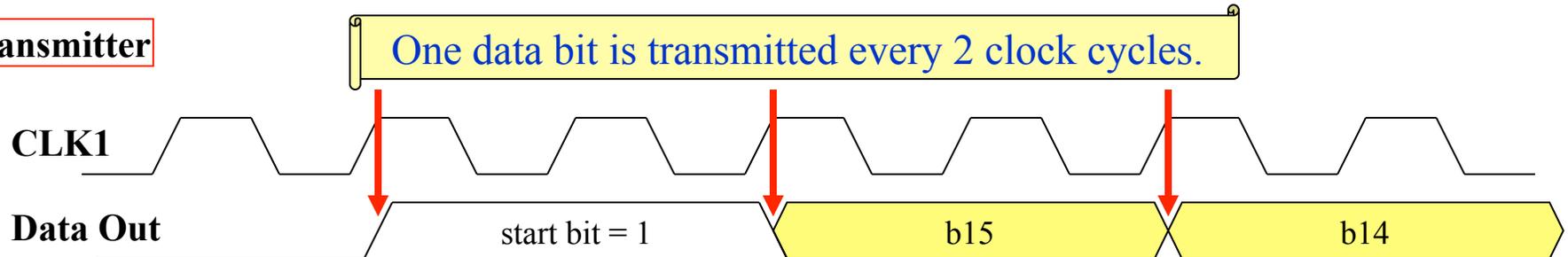
Schematics of Digital Phase Follower



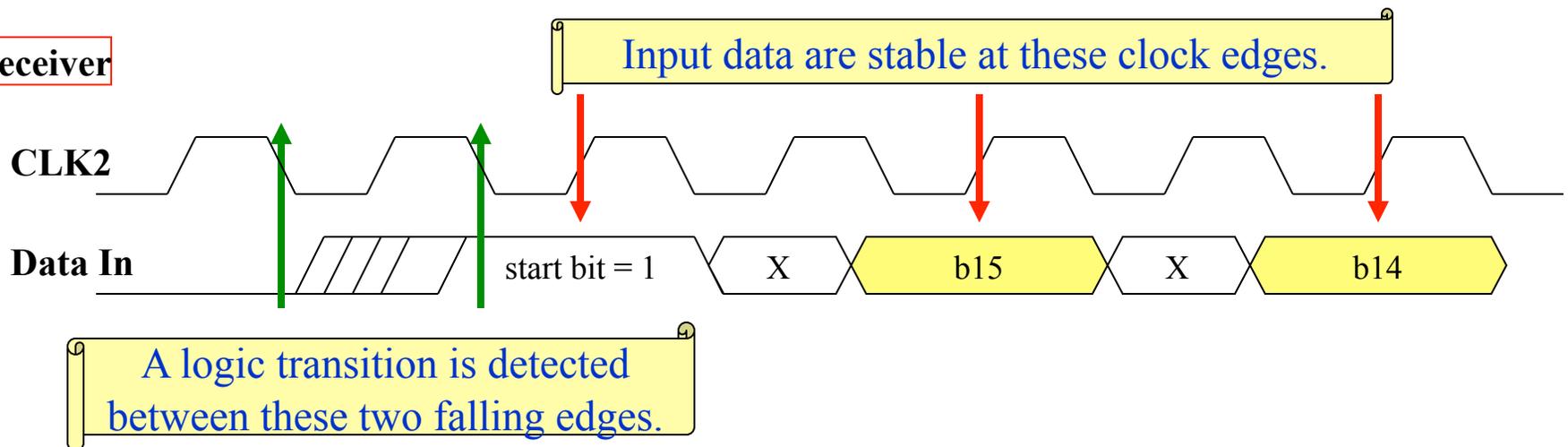
- CLK: 375MHz
- Data Rate: 375Mbits/s

The Two-Cycle Serial IO

Transmitter

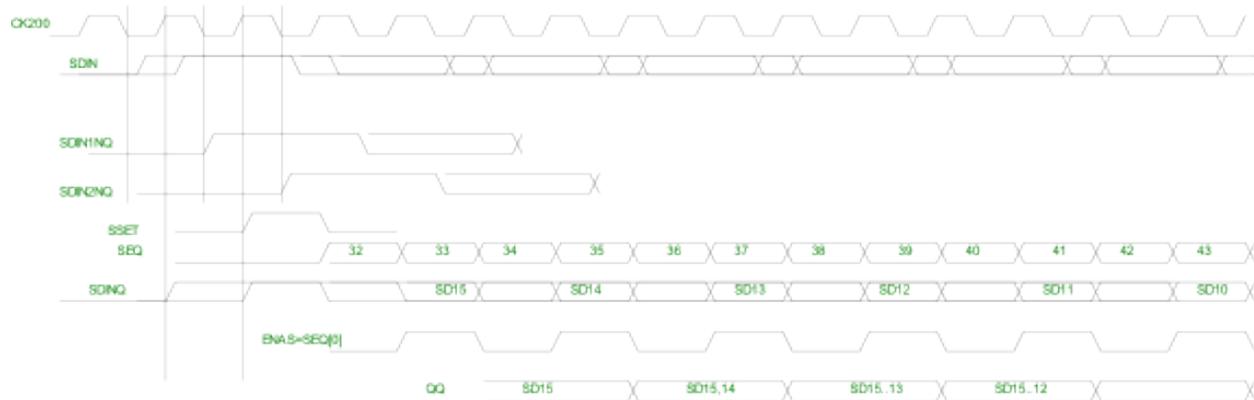
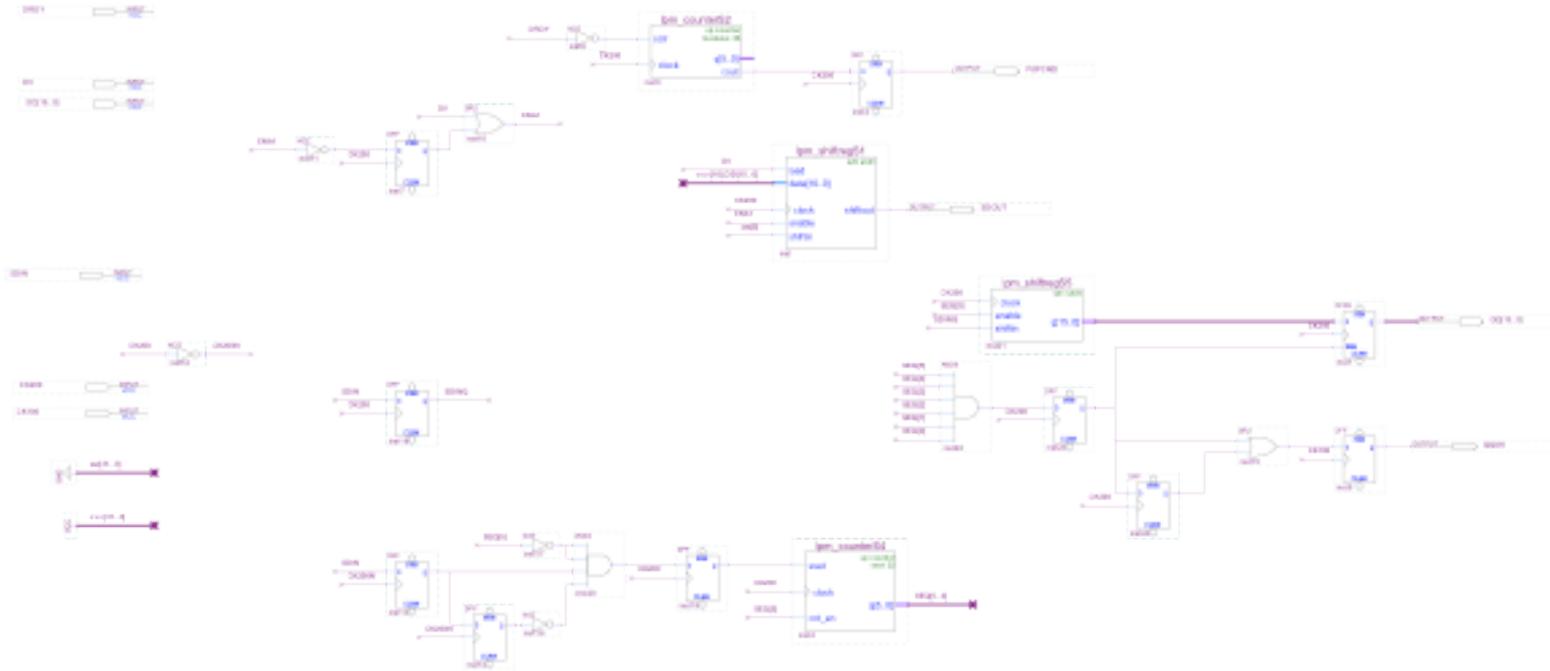


Receiver



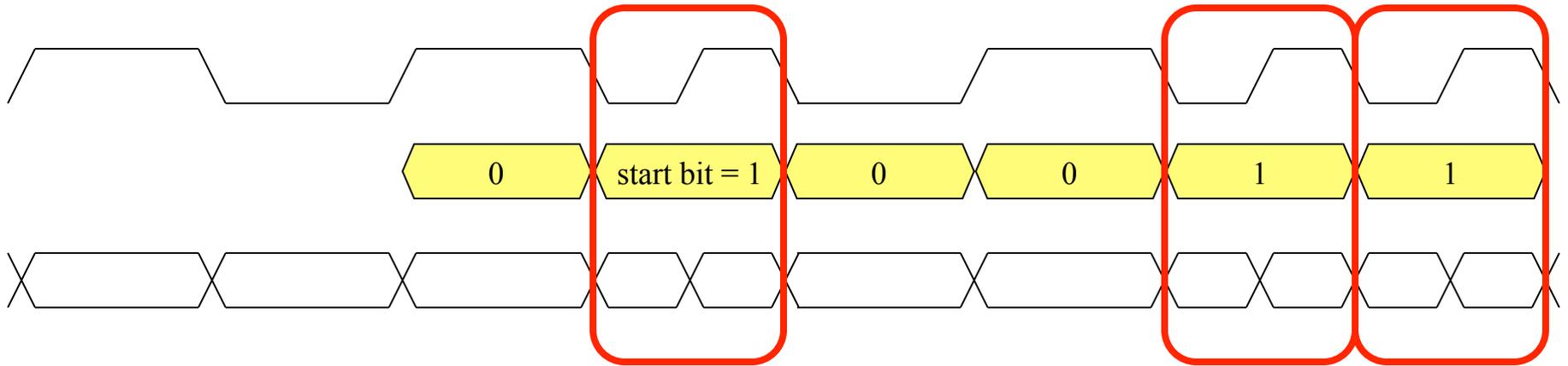
- This scheme is slower than digital phase follower but the logic is simpler.
- The CLK1 and CLK2 can be generated with two free running crystal oscillators.

Schematics of the Two-Cycle Serial IO



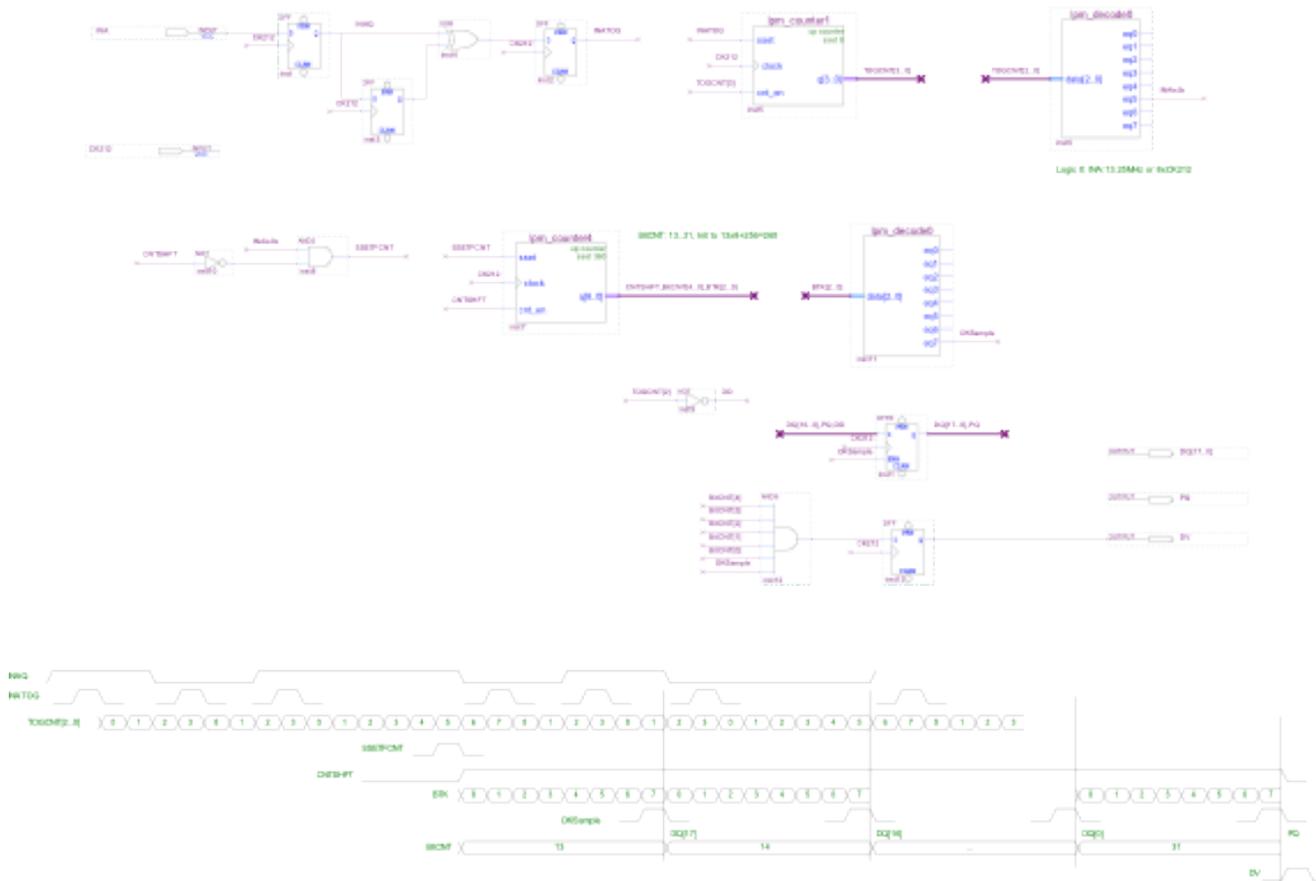
- CLK: 200MHz
- Data Rate: 100Mbits/s

The FM coding



- A bit is transmitted in two unit time intervals, usually in two internal clock cycles at frequency f .
- For bit=1, the output toggles each cycle, i.e., with frequency $(f/2)$ and for bit=0, the output toggles every two cycles, i.e., with frequency $(f/4)$.
- When not transmitting data, the output toggles at frequency $(f/4)$, until seeing the start bit.
- The data stream is naturally DC balanced suitable for AC coupled transmission.
- The polarity of the interconnection doesn't matter.

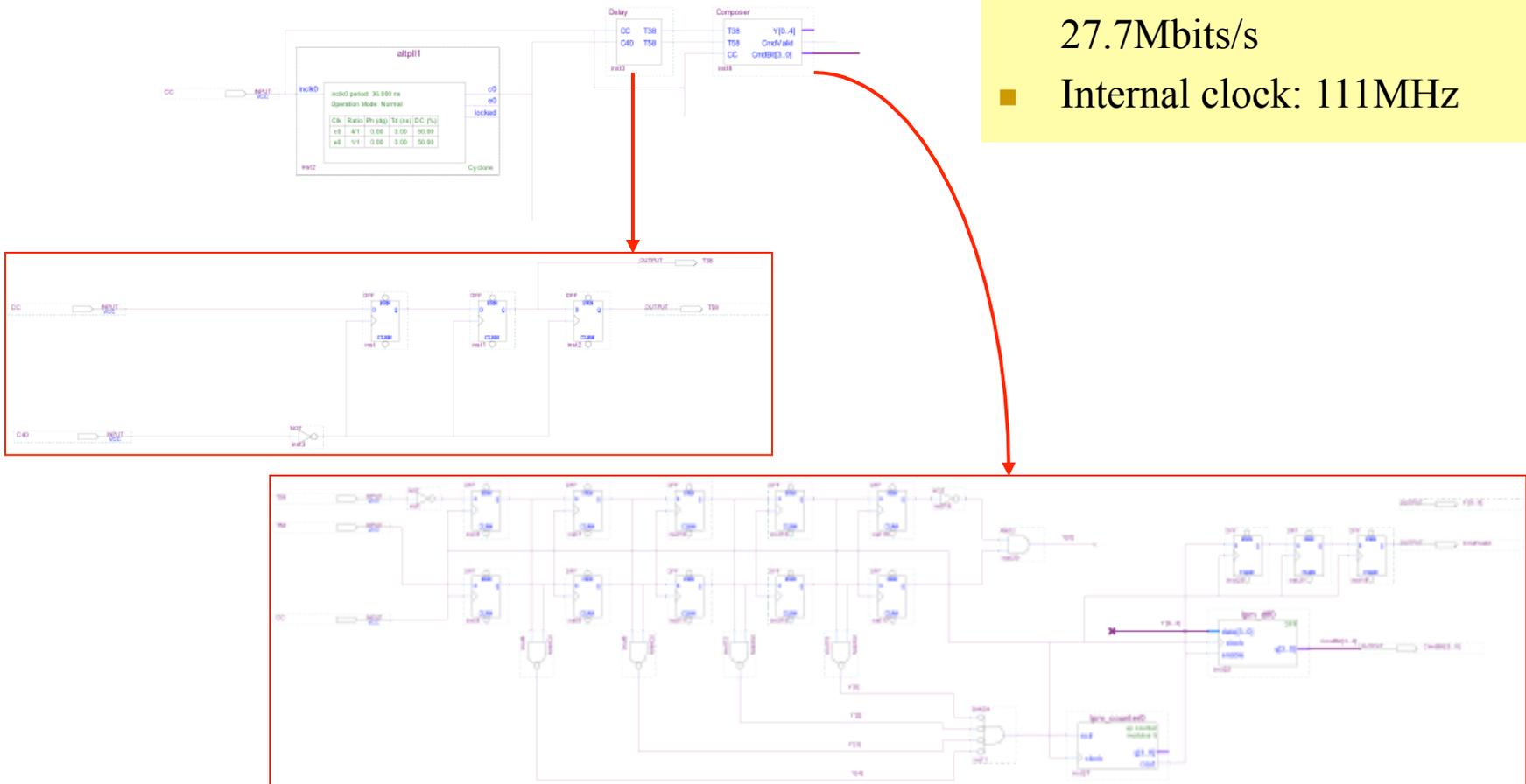
Schematics of FM Decoder



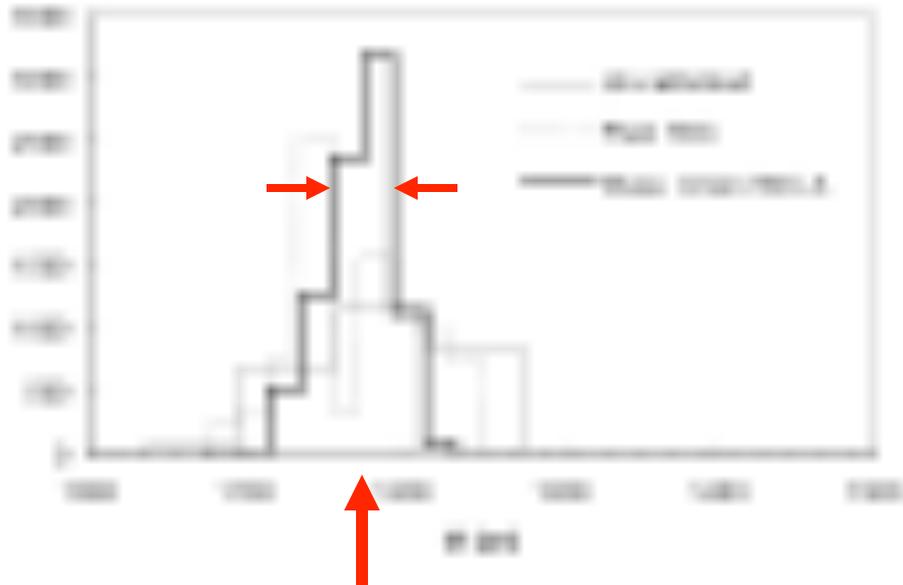
- CLK: 212MHz
- Data Rate: 26.5Mbits/s
- The ratio 8 CLK cycles/bit in this design is not an intrinsic limit.

Schematics of C5 Decoder

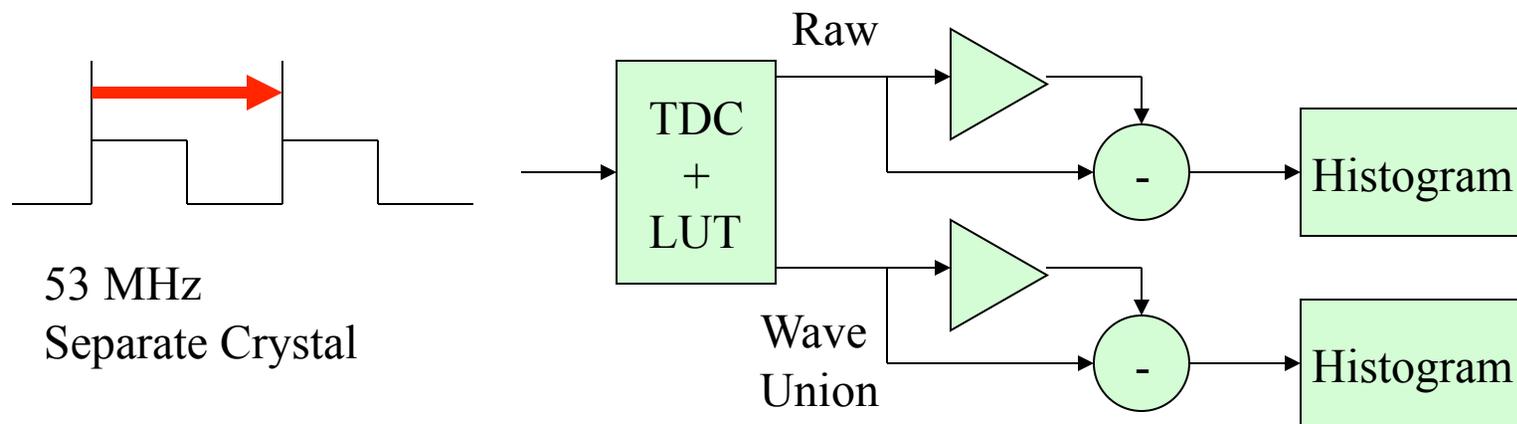
- Data Rate: 36ns/bit or 27.7Mbits/s
- Internal clock: 111MHz



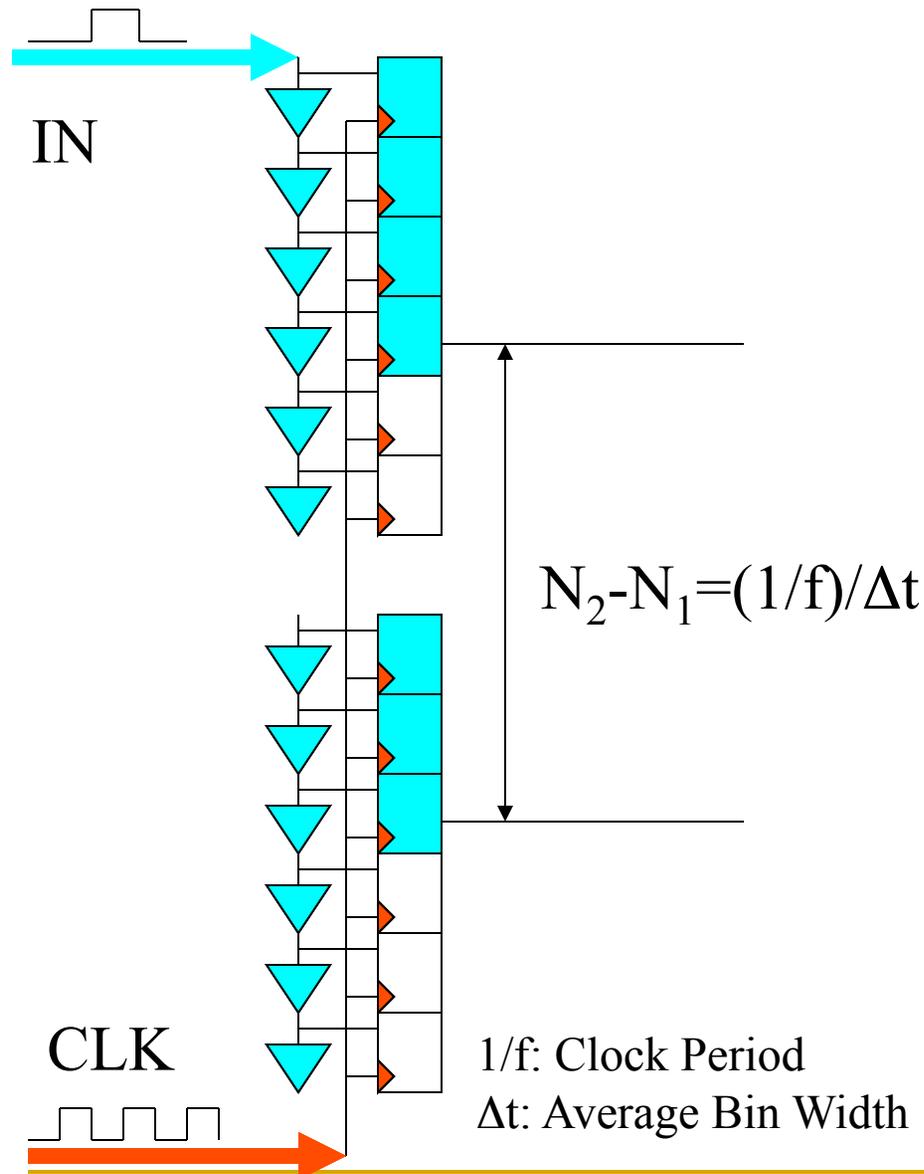
Measurement Result for Wave Union TDC A



- Plain TDC:
 - delta t RMS width: 40 ps.
 - 25 ps single hit.
- Wave Union TDC A:
 - delta t RMS width: 25 ps.
 - 17 ps single hit.



Digital Calibration Using Twice-Recording Method



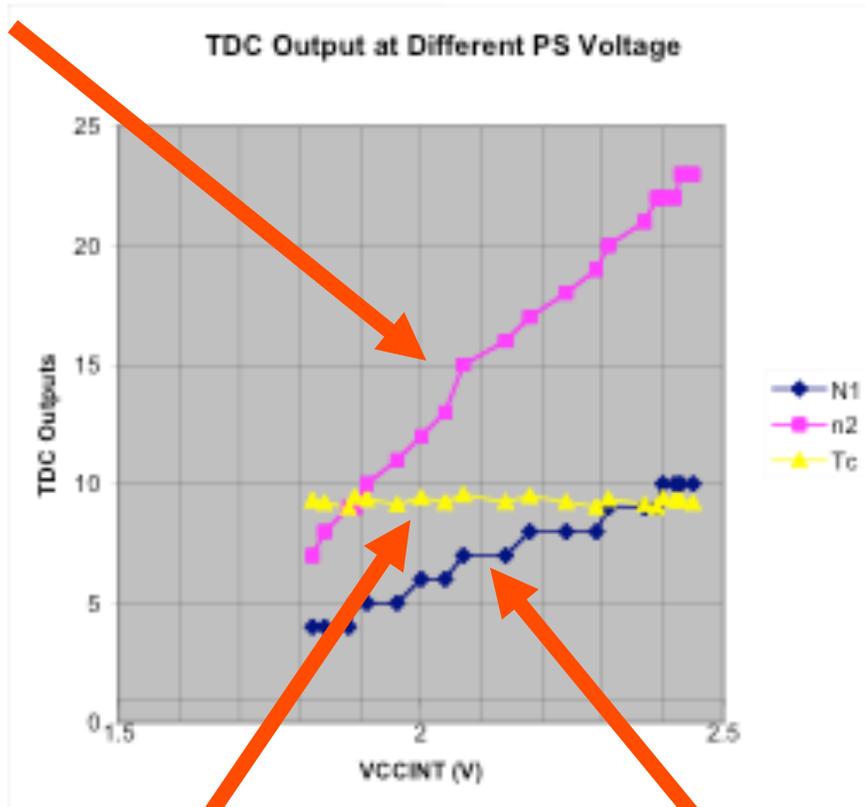
- Use longer delay line.
- Some signals may be registered twice at two consecutive clock edges.

The two measurements can be used:

- to calibrate the delay.
- to reduce digitization errors.

Digital Calibration Result

N_2



Corrected Time

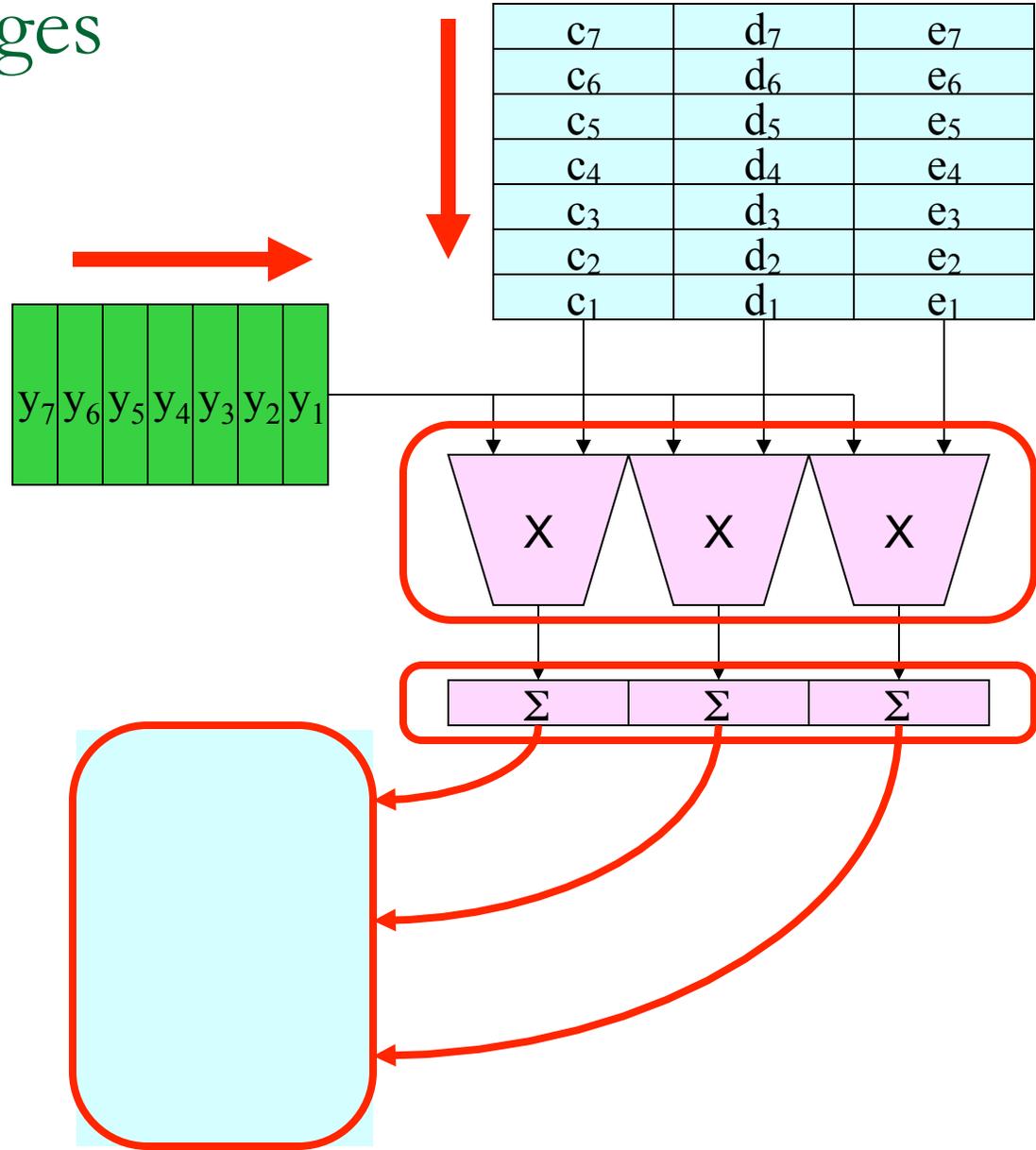
N_1

- Power supply voltage changes from 2.5 V to 1.8 V, (about the same as 100 °C to 0 °C).
- Delay speed changes by 30%.
- The difference of the two TDC numbers reflects delay speed.

■ **Warning: the calibration is based on average bin width, not bin-by-bin widths.**

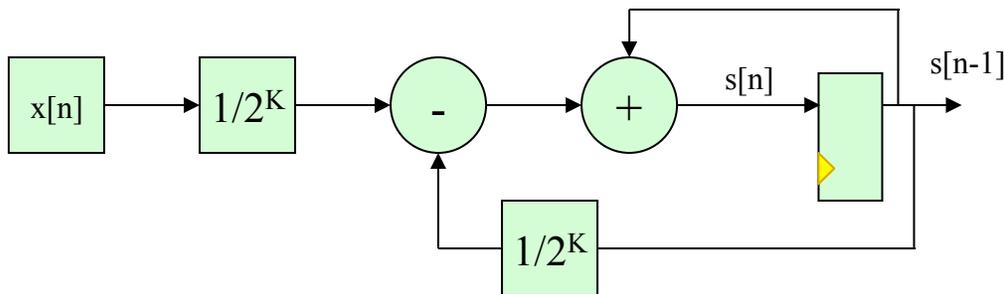
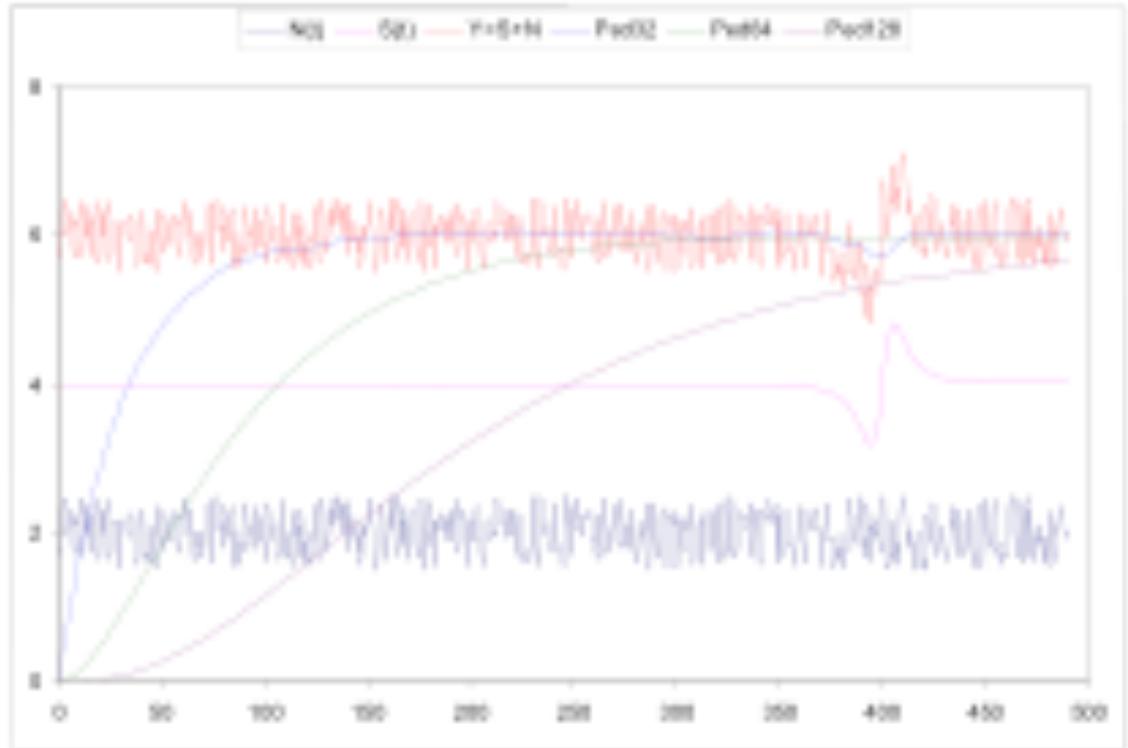
Weighted Averages

- The weighted average is a special case of inner product.
- Multipliers are usually needed.



Exponentially Weighted Average

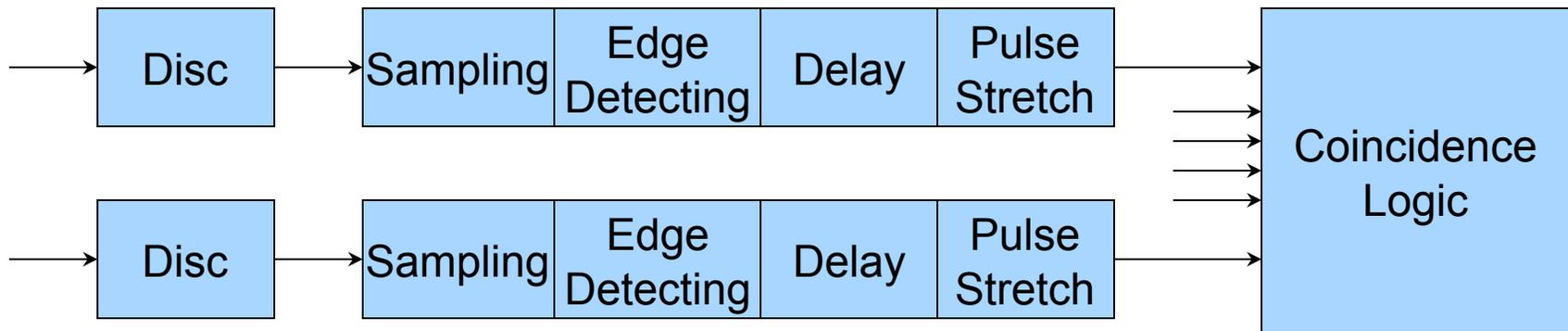
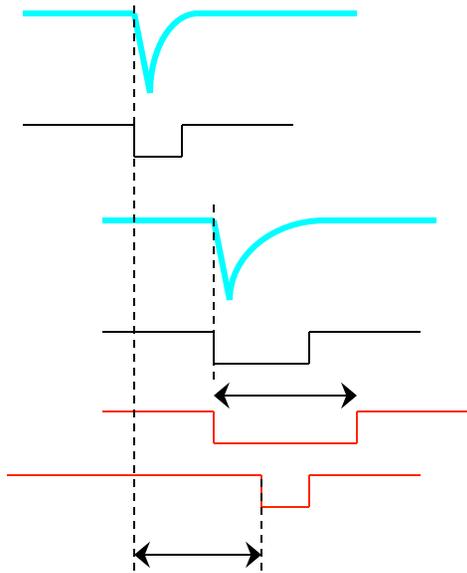
- No multipliers are needed.
- The average is available at any time.
- It can be used to track pedestal of the input signals.



$$s[n] = s[n-1] + (x[n] - s[n-1]) / N$$
$$N = 2, 4, 8, 16, 32, \dots$$

Parameters in Coincidence Finding

Digital Coincidence Finding



Some Details

