An aerial photograph of the Fermilab site. A prominent feature is a large, circular, multi-lane track, likely for horse racing, which is surrounded by green grass and trees. To the right of the track, there are several large, modern buildings, including a distinctive white, curved structure. The surrounding area consists of a mix of green fields, brown patches, and dense forests. The sky is clear and blue.

A Preferable Scheme of Multi-Sampling TDC

Wu, Jinyuan

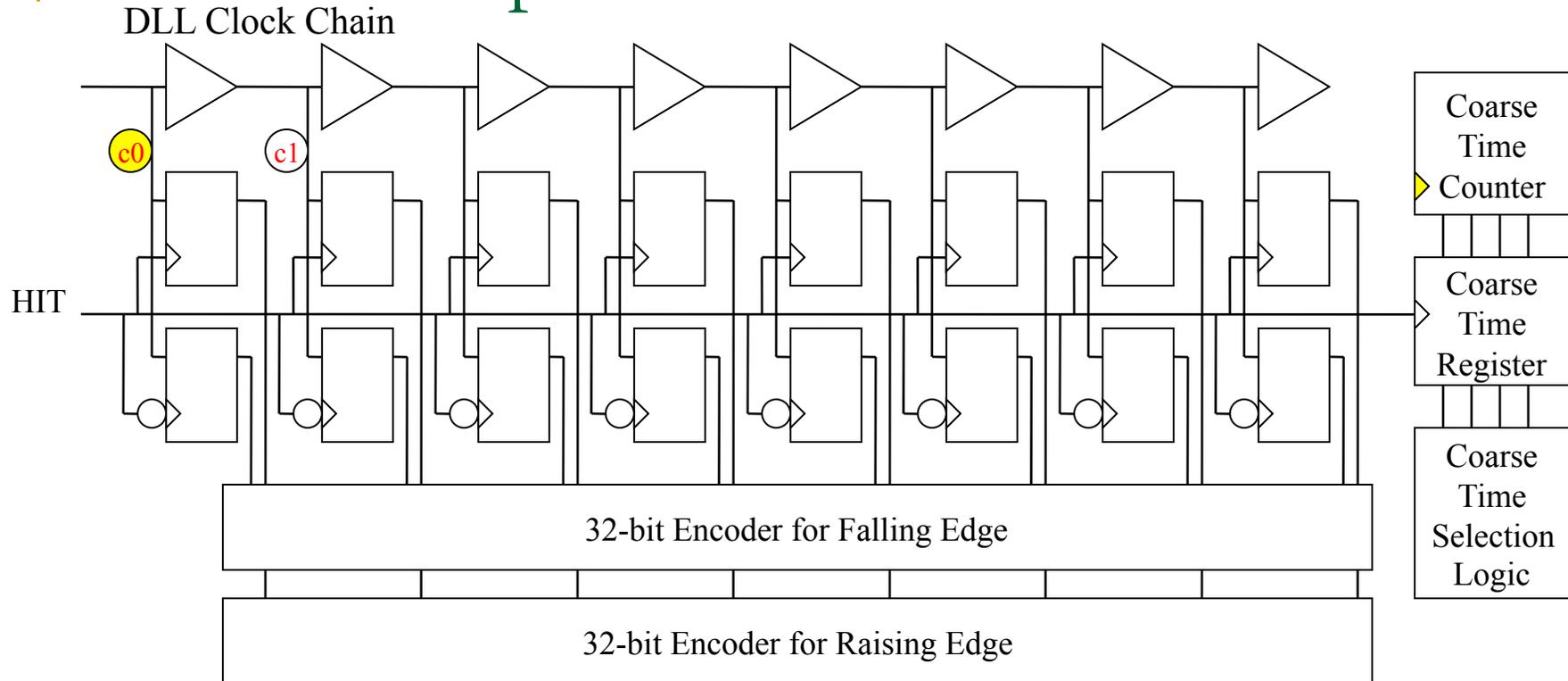
Fermilab

June. 2011

Introduction

- In history, the multi-sample TDC is implemented with HIT feeding into the CK port of the flip-flop of the register array.
- In the HIT->CK scheme, special cares must be taken for coarse time recording.
- A more preferable scheme can be constructed via a simple topology change, i.e., feeding HIT to the D port of the flip-flop.
- The HIT->D scheme simplifies coarse time recording, supporting both leading edge and falling edge digitization with a single set of register array and encoder and allows deadtimeless operation.

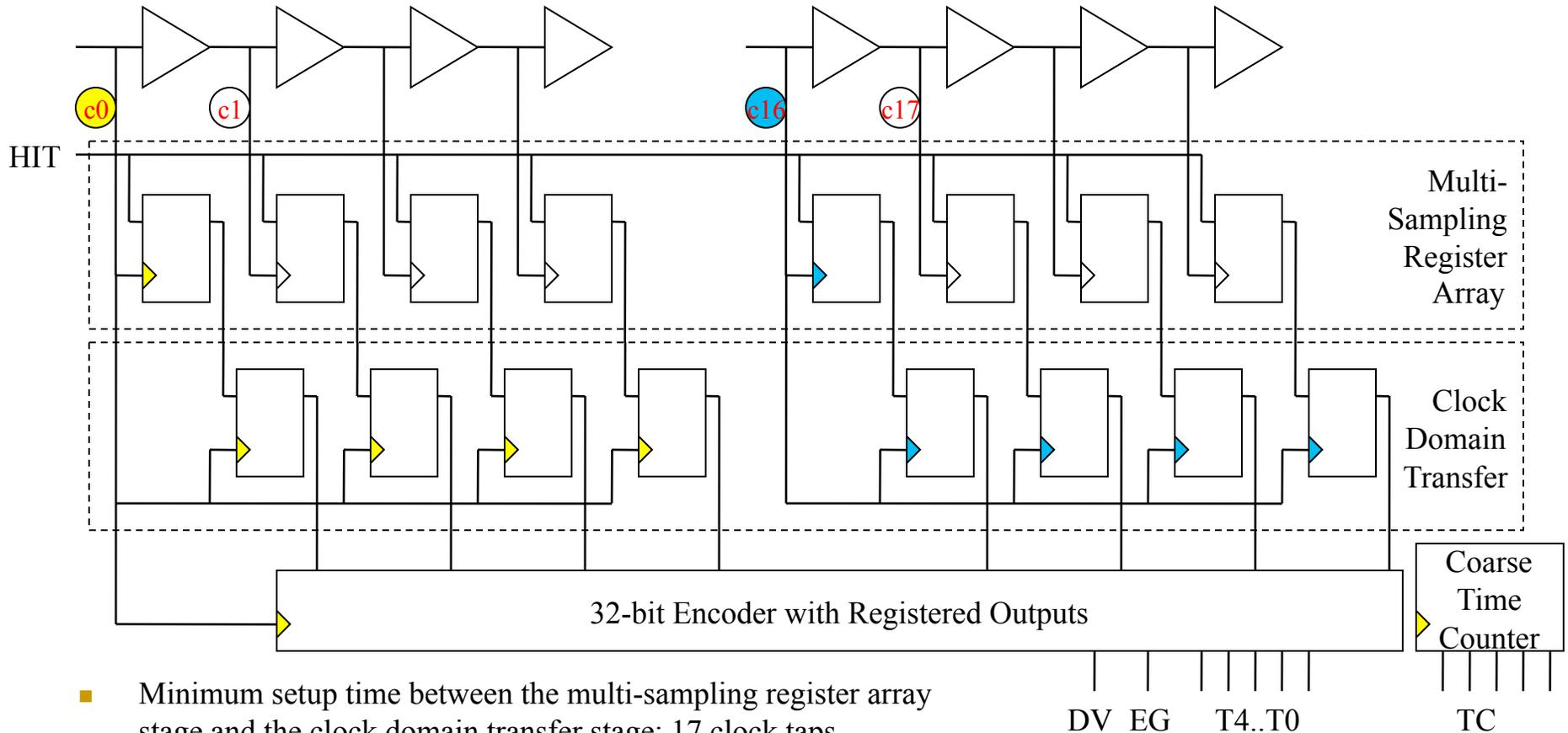
Historical Implementation



- The clock taps c0 to c31 are fed into D and HIT is fed into CK port of the flip-flop.
- Two sets of array and encoder are needed for raising edge and falling edge.
- The HIT is also used as CK of the register to record the coarse time.
- Coarse time selection logic is needed.

A Preferable Scheme

DLL Clock Chain



- Minimum setup time between the multi-sampling register array stage and the clock domain transfer stage: 17 clock taps.
- Setup time between the clock domain transfer stage and the encoder register: 32 or 16 clock taps.
- All outputs including TC are aligned with c_0 .
- Supports both raising and falling edges.

EG: Edge, =1: Raising or =0: Falling.

T4..T0: Time.

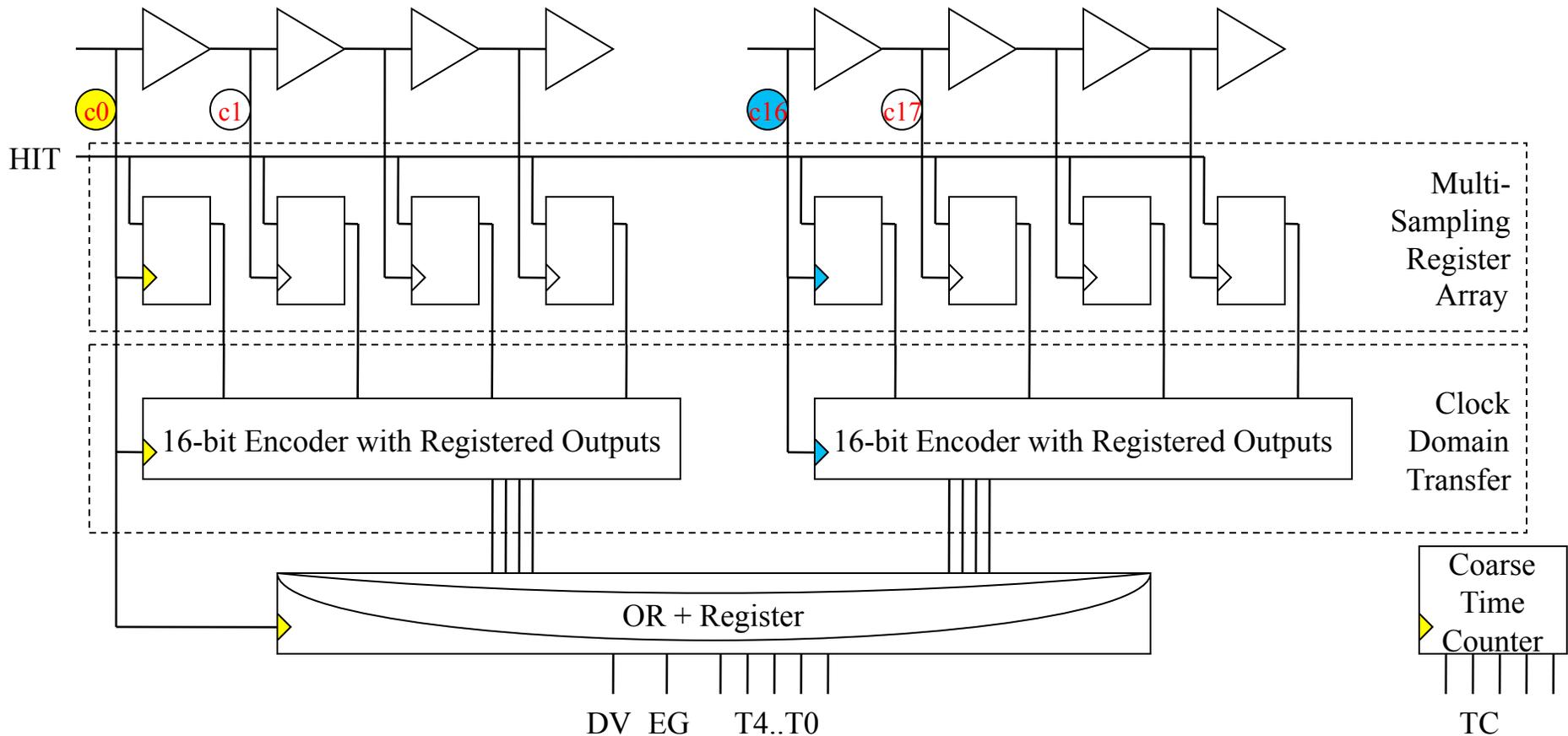
DV: Data Valid, =1 Valid edge detected.

It is used as PUSH signal for FIFO or

Write Enable for other memory buffers.

A Implementation Saving More Silicon Area

DLL Clock Chain



- The clock domain transfer function can be combined with partial encoding functions.
- This scheme saves more silicon area.

Comparison

Historical Scheme: HIT-> CK; (c0..c31)->D;	Preferable Scheme: HIT-> D; (c0..c31)->CK;
Deadtime is unavoidable.	Deadtimeless operation is possible.
Coarse time recording needs special care.	No special care is needed for coarse time.
Two array + encoder sets are needed for raising edge and falling edge.	Both raising and falling edges are digitized with a single array + encoder set.
The register array must be reset for next event.	No resetting is needed for the register array.
The encoder must be re-synchronized with system clock in order to interface with readout stage.	The output is synchronized with the system clock and is ready to interface with readout stage.

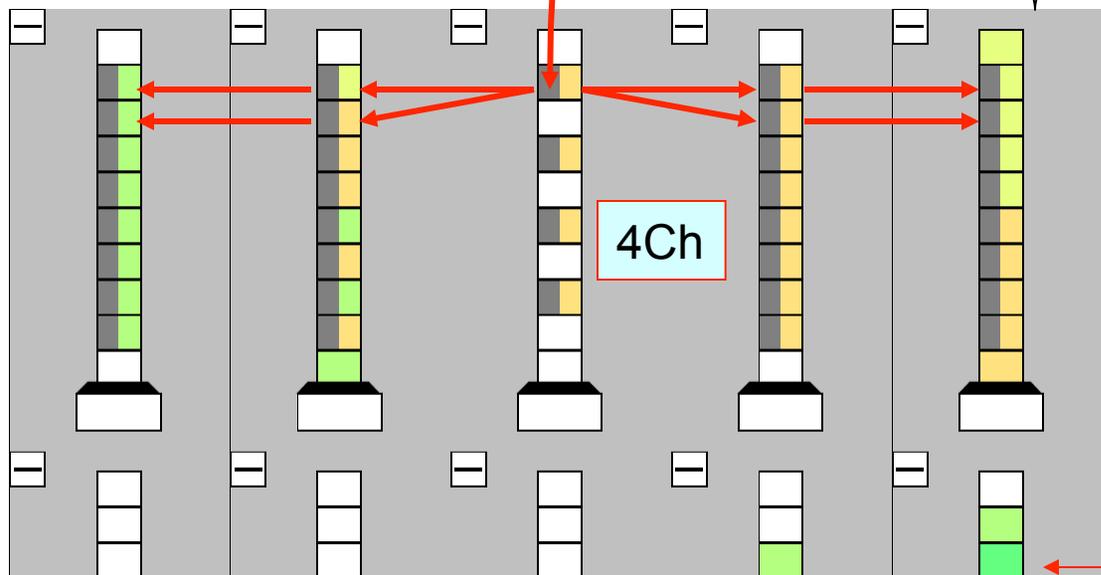
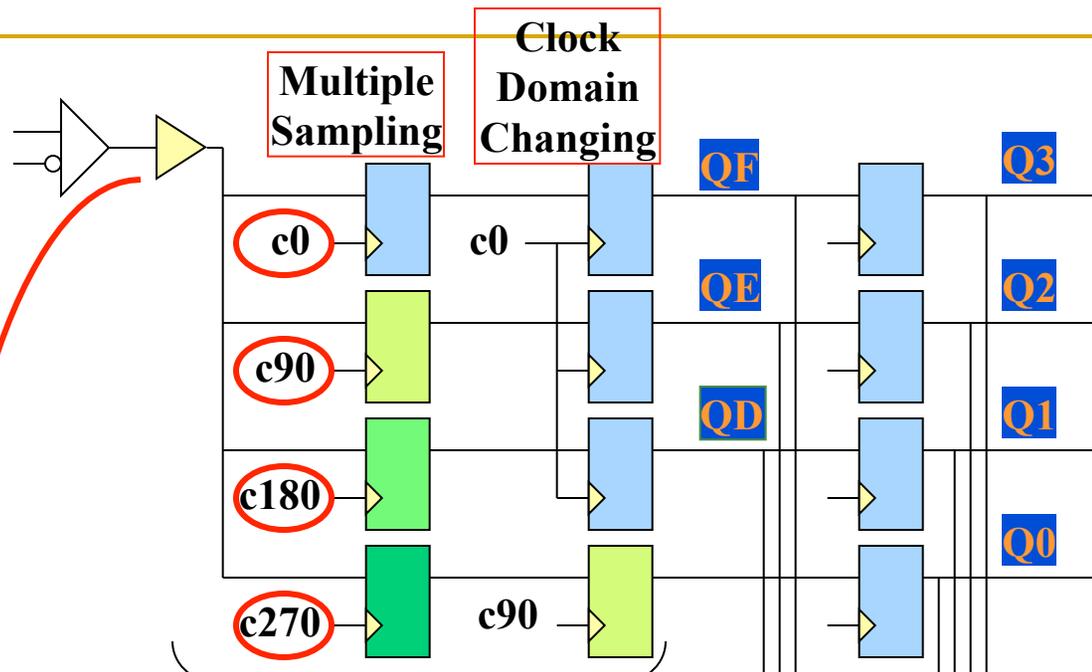
An aerial photograph of a golf course. The course is a large, winding green with several holes and sand traps. In the center-right, there is a clubhouse building with a distinctive white, curved roof. To the left of the clubhouse, a tall, white water tower stands prominently. The surrounding area includes fields, trees, and some residential or commercial buildings in the distance. The image is framed by a thin yellow border.

The End

Thanks

The Multi-Sampling Block

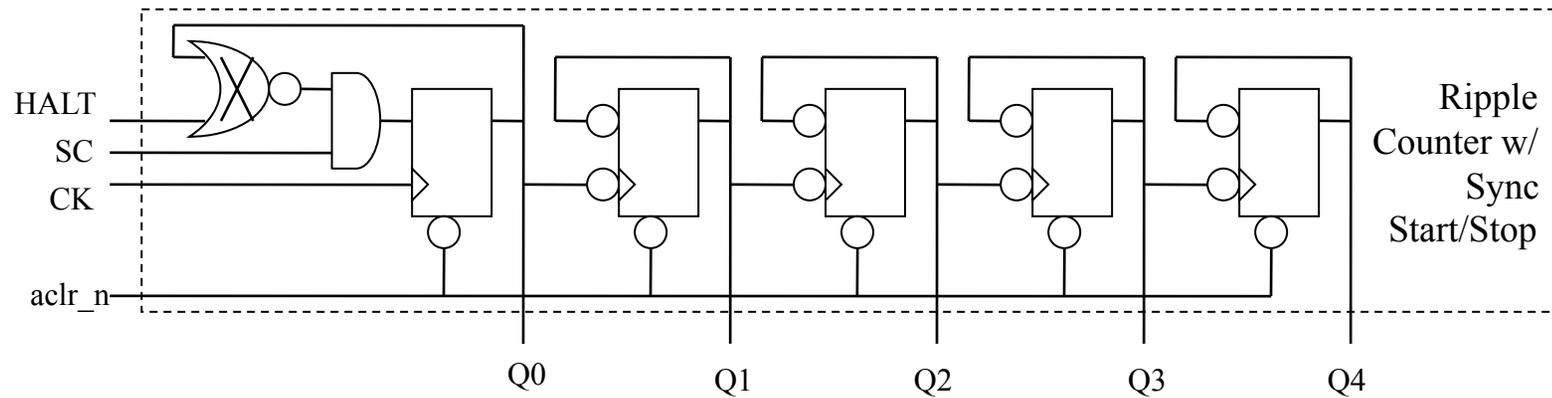
- Sampling rate: 250 MHz
x4 phases = 1 GHz.
- LSB = 1 ns.



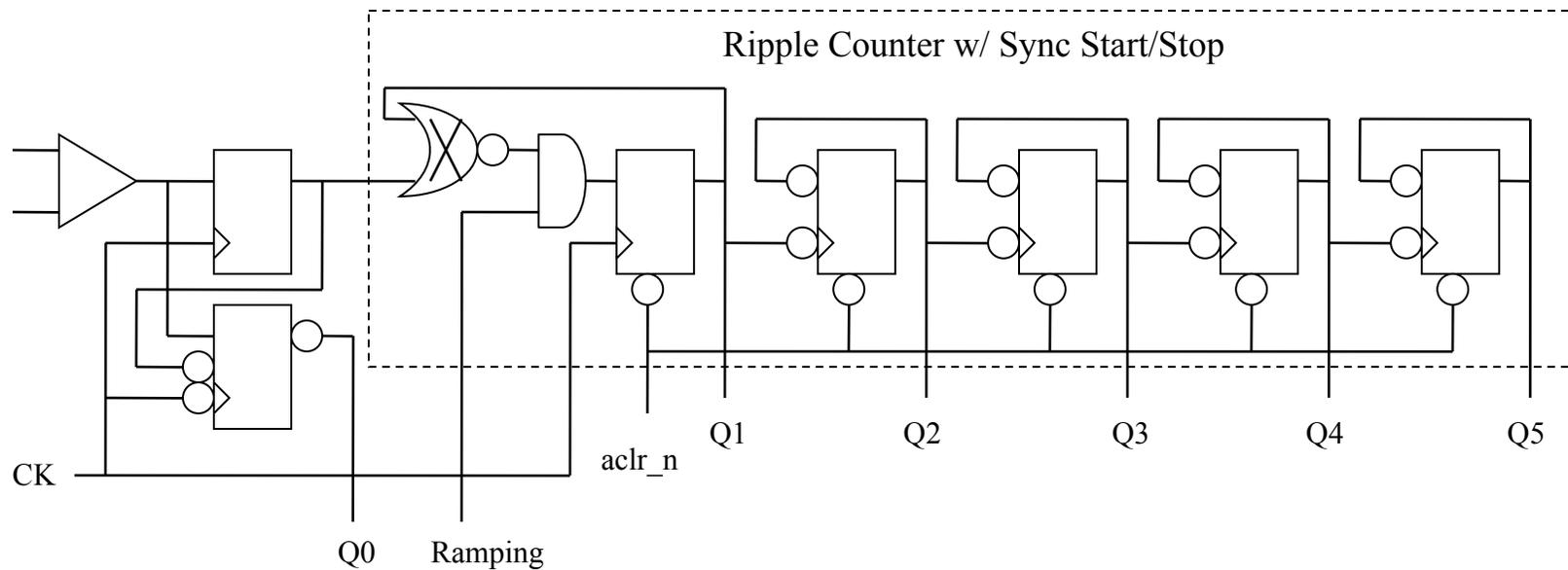
This picture represent a placement in Cyclone FPGA

Logic elements with non-critical timing are freely placed by the filter of the compiler.

The Ripple Counter w/ Sync Start Stop



Single Slope ADC Supporting Half Cycle



The Multi-Sampling Structure

