

# QIE Electronics for JLab Test

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# Goals for QIE Board

- To evaluate the capabilities of the CMS charge integrating encoder (QIE8) family of chips.
- To test the effects of delaying the input phase by varying input cable lengths.
- To test readout capabilities of PCI-based scheme.
- To provide NIM-level clock signals for clock fanout cards.
- To start development of readout boards for future QIE releases.

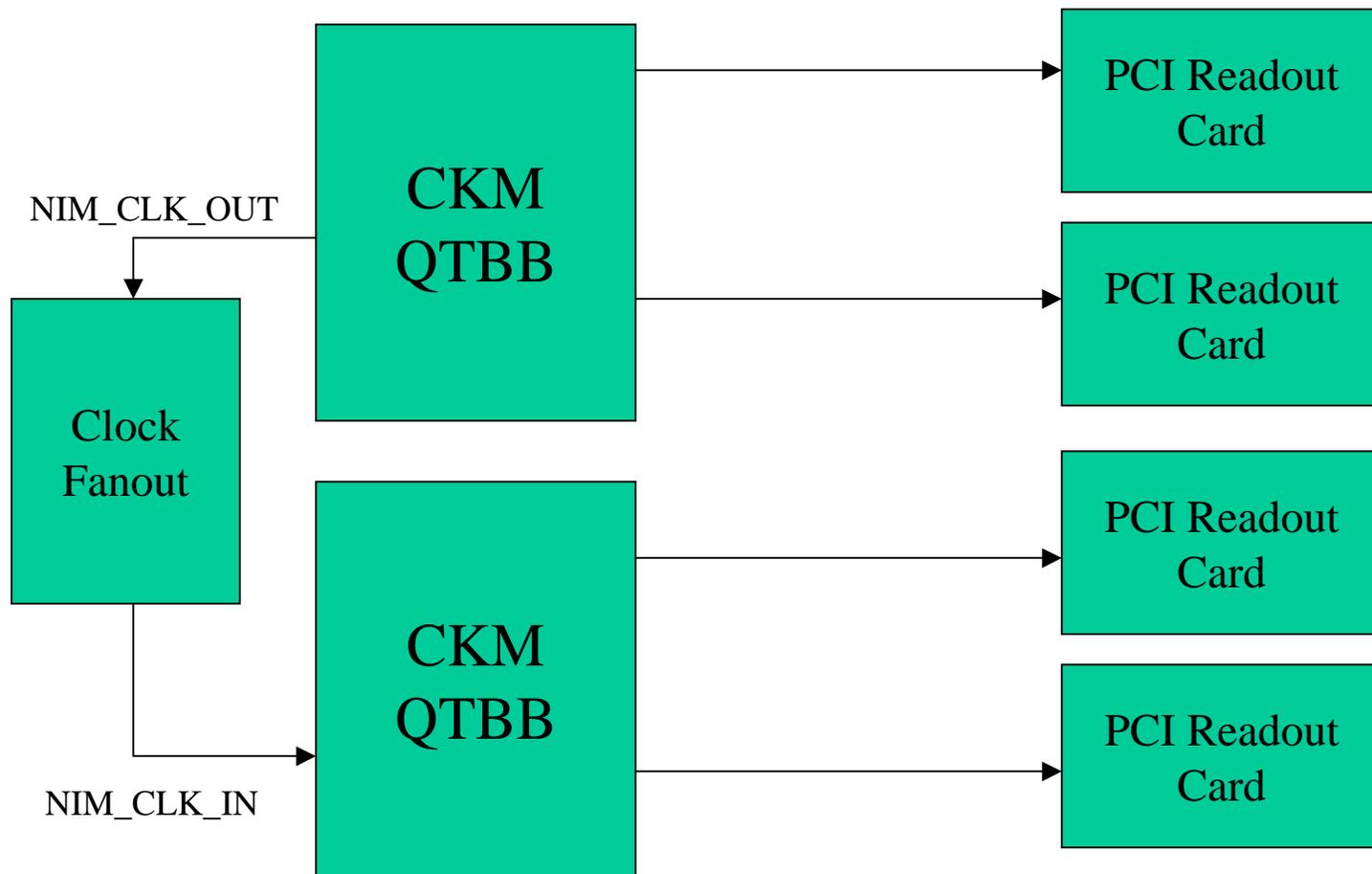
# CMS QIE8 Specifications

## QIE Performance

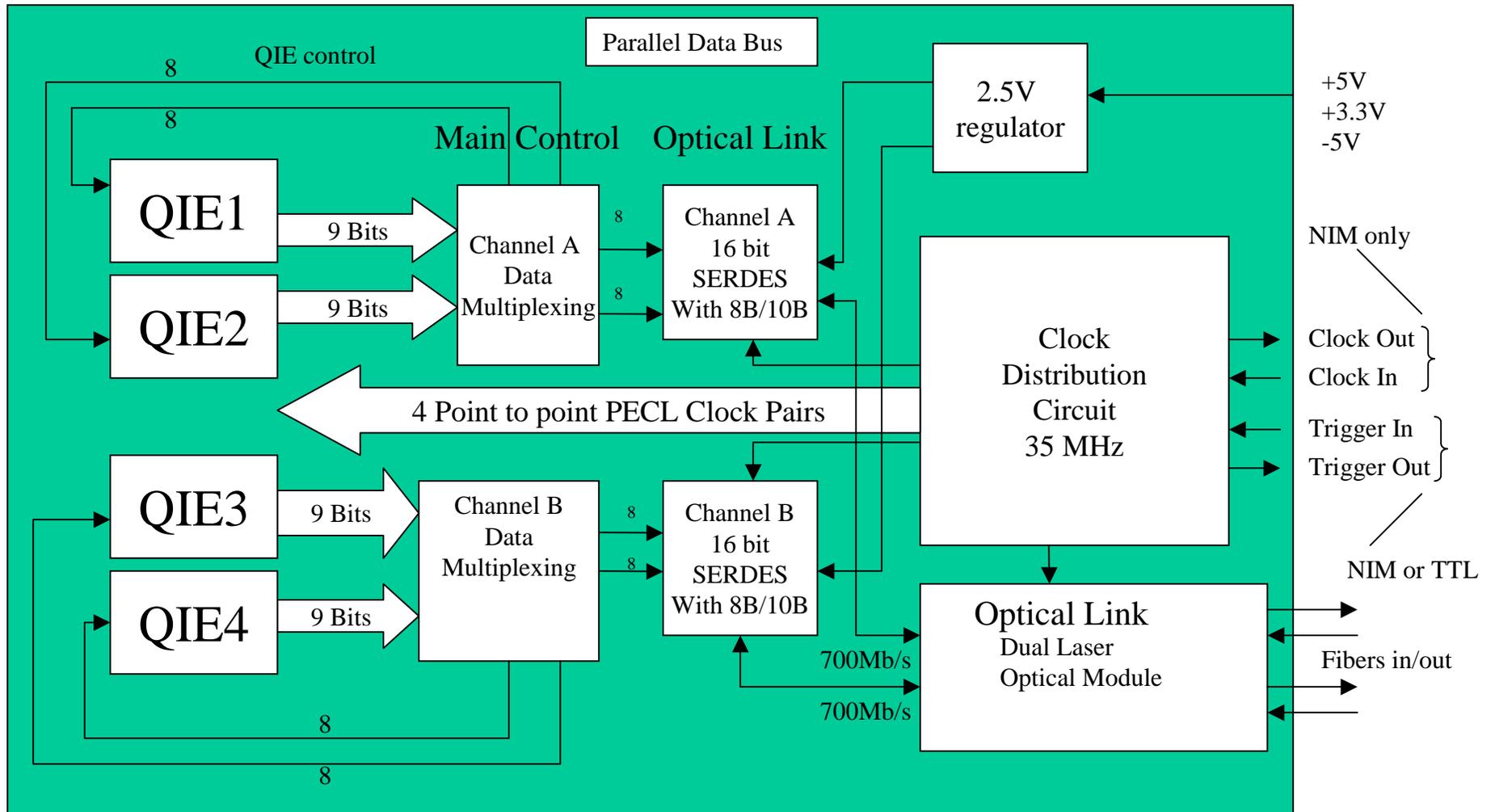
## CKM Specifications

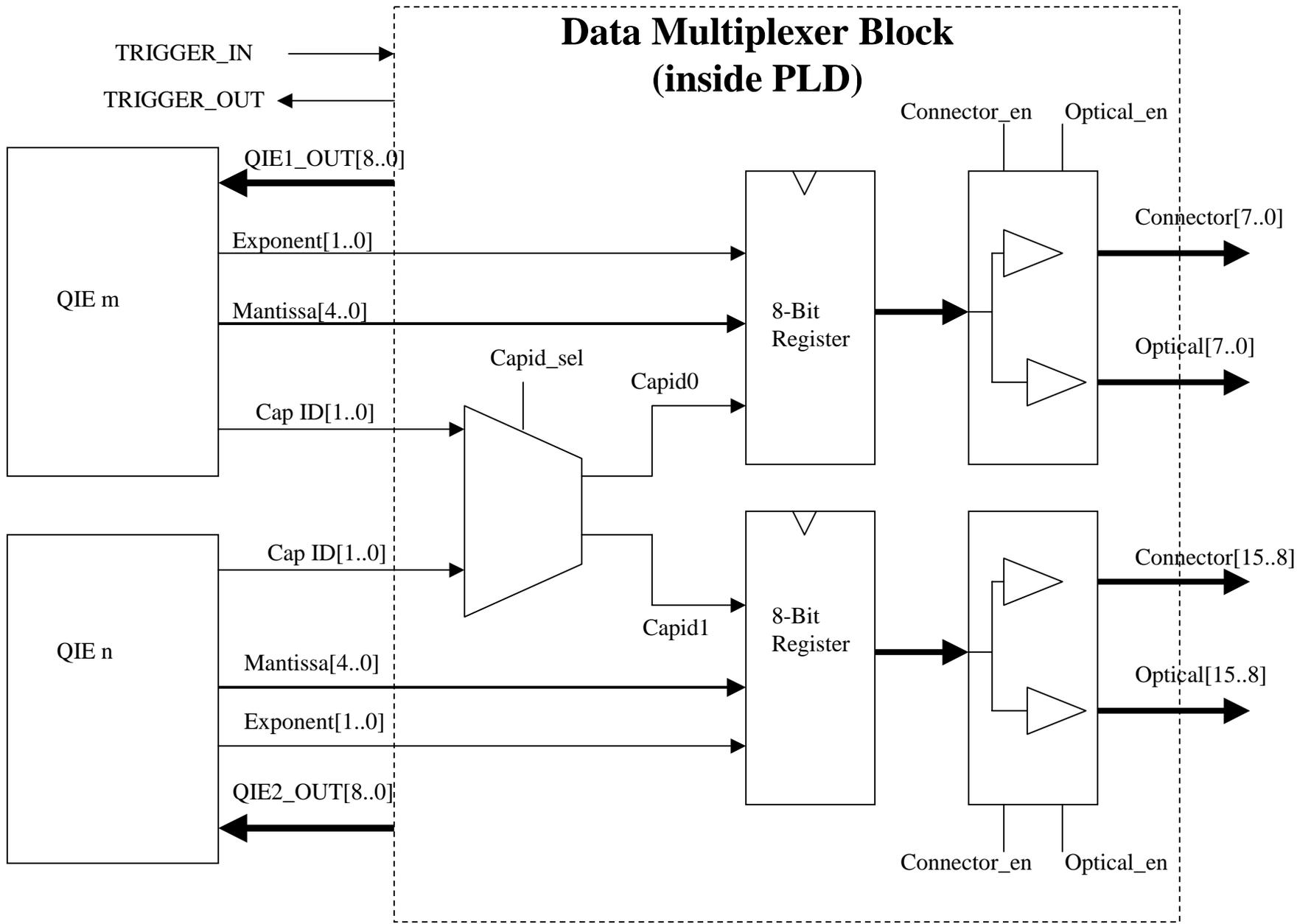
|                     |                  |                           |
|---------------------|------------------|---------------------------|
| Minimum Charge      | 2.7 fC           | VVS: 40 fC<br>FVS: 10 fC  |
| Maximum Charge      | 27 pC            | VVS: 320 pC<br>FVS: 75 pC |
| Operating frequency | 35 MHz           | 80-100 MHz                |
| Precision           | 5-bit -> 3%      | FVS: 2%<br>VVS: 8%        |
| Dynamic range       | 13 bits          | VVS: 13 bits              |
| Noise               | 2 fC w/ 3m cable | -                         |

# JLab Test Beam System Block Diagram



# CKM QIE Test Beam Board (QTBB) Block Diagram

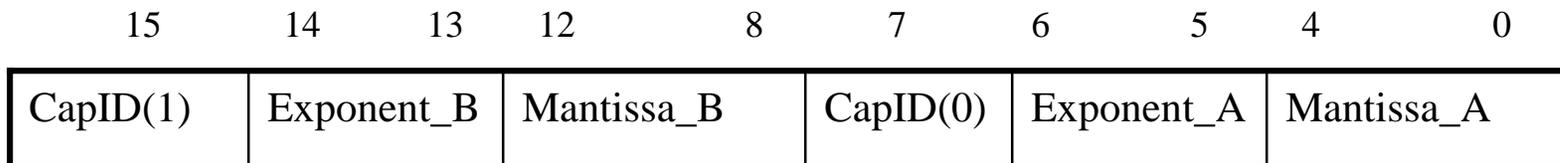




# Optical Link Information

- Data out rate: 2 fibers out at 700Mbits/s
- Data in rate: 2 fibers in at 700Mbits/s

Data Word Format:



# Upgrade Path

- The CKM QTBB in its current state would require layout changes to accommodate the higher speed QIE device.
- However, the core logic of the design is verified for 80MHz+ operation
- The current board utilizes a databus that may be modified to receive trigger data back from the readout card via the optical link. This may prove useful by eliminating TTL and NIM level inputs. The clock signal might also be extracted from the optical link.
- The current board utilizes a small portion of the maximum logic blocks in the selected PLD devices, so the current QTBB would allow some simple trigger functionality.
- The optical link would be able to operate at upwards of 2.5Gbps by selecting a pin-compatible replacement SERDES device and a new laser module (possibly pin-compatible as well).
- The major holdback from using the current QTBB for 80MHz+ operation is the some layout signal integrity issues and the change in QIE pinout for future QIEs. However, the board could prove useful as a development tool.