Current Knowledge on CKM Front-end Electronics

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Since 2nd Edition of Proposal

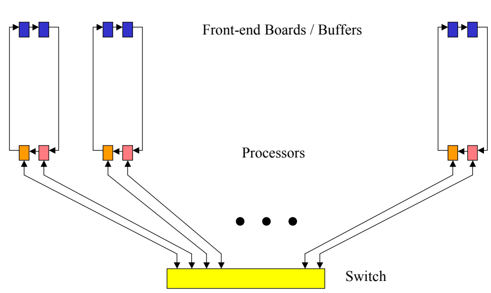
- The front-end electronics, as the data source, need to match the global picture change – software trigger scheme.
- Large amount of new knowledge, test design, simulation, prototype, etc.
- Possible inherits (cost saving): HV (LRS 1440) and crates, PS, racks, etc.

Possible Inherits

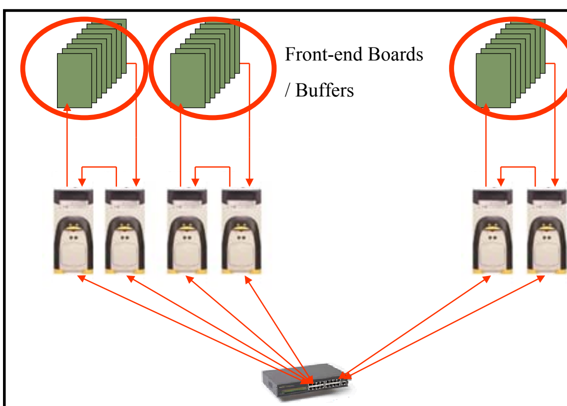
- High voltage: LRS 1440 from KTeV.
  - What's the best use of this? FVS? VVS?
  - What about CW development?
  - Work request for experts to study on this.
- Crates, PS, racks, etc: from other experiments.
  - Inventory, quality?
  - Work request for experts to study on this.

CKM FE General Information

- Total channel count: 33K.
  - TDC only channels: 27K.
    - Chambers: UMS, KEAT and DMS.
    - PMT: KRICH, PRICH, BTSM, ETP and CVP.
  - TDC + ADC channels: 6K.
    - PMT: from veto detectors VVS, FVS, BIVS, MVS and HVS.
- Pipeline structure, no DAQ dead time.
- Zero-suppression is needed before sending data through DAQ switch.

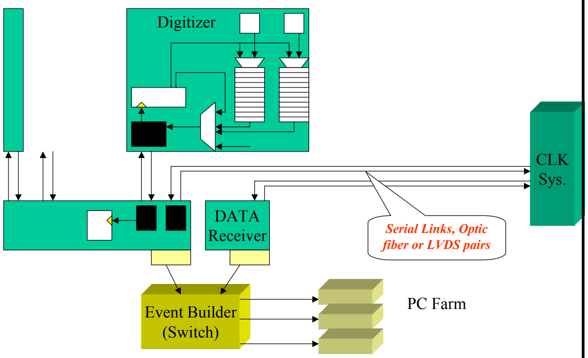


Switch-based DAQ Architecture

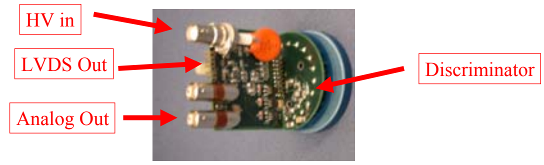


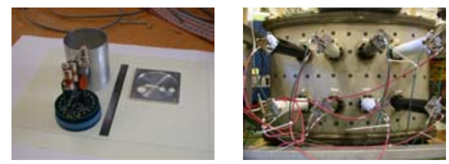
Switch-based DAQ Architecture, Commercial

Details of Front-end Sub-systems

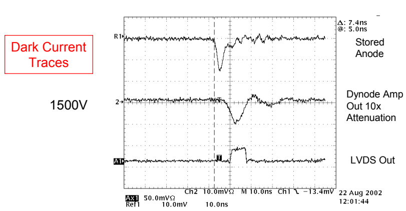


Jlab VVS Prototype PMT Base

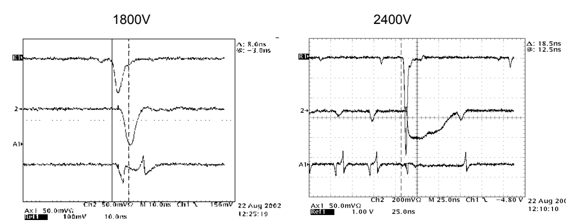




Jlab VVS Prototype PMT Base



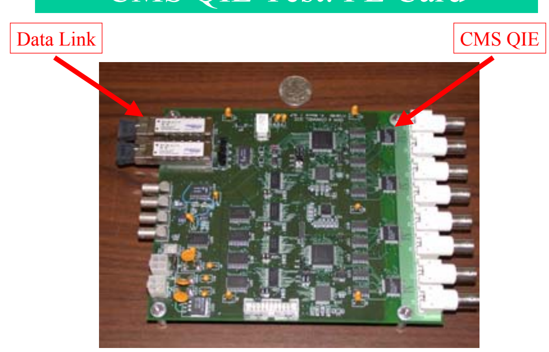
Jlab VVS Prototype PMT Base



Jlab VVS Prototype PMT Base

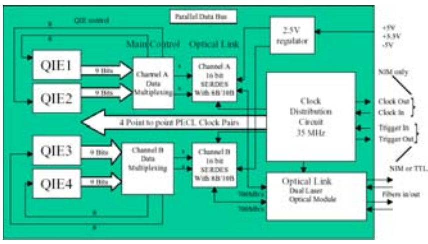
- PMT base for VVS prototype were used in Jlab test beam.
- The VVS base with integrated discriminator achieves threshold of 1 MeV.
- Electronics noise is negligible.

CMS QIE Test: FE Card



CMS QIE Test: FE Card

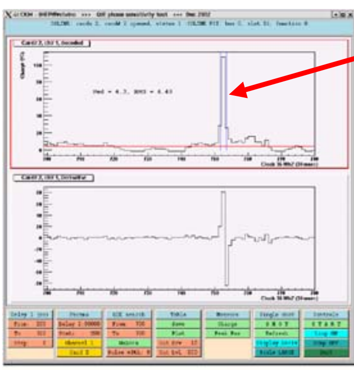
Block Diagram



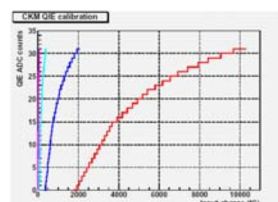
CMS QIE Test: Readout Card

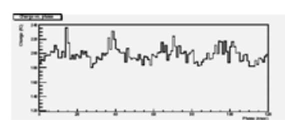
- QIE readout card is a modified CoLink card.

CMS QIE Test: Software Interface



CMS QIE Test: Results

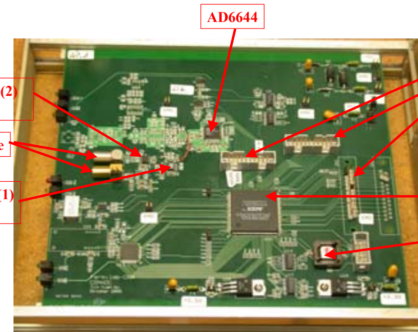




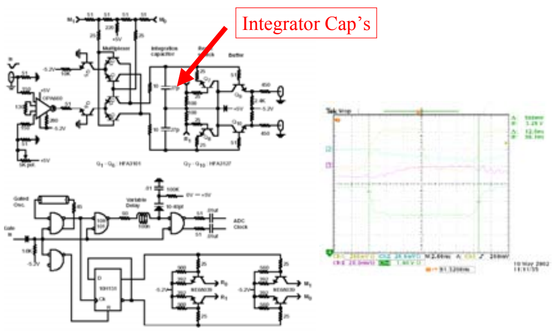
CMS QIE Test: Results

- CMS QIE with 10 m cable has good noise performance with our nominal VVS gain of $1x10^5$ and FVS gain $5x10^3$.
- CMS QIE clock phase sensitivity is under control.
- CMS QIE part now runs at 75 MHz, path to 100 MHz and 6-bit mantissa looks clear.

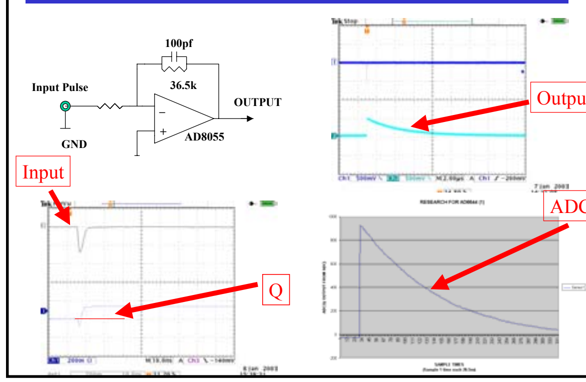
Commercial ADC: The Circuit Board



COMADC: 2-phase Integrator

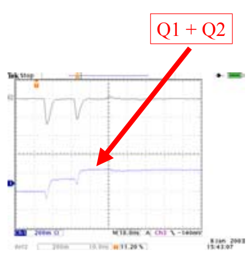


COMADC: Bleeding Integrator



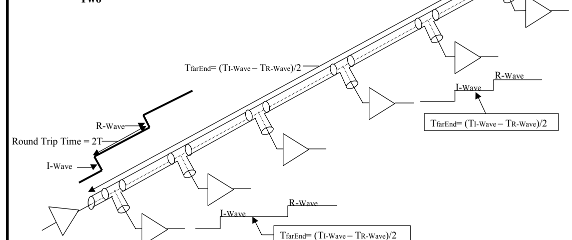
COMADC: Current Findings:

- Noise level is under control. (RMS 1.01 to 1.8 LSB or 0.25MeV at 4GeV full scale).
- There is no phase sensitivity issue (for bleeding integrator).
- Linear response provides good multi-pulse detection.



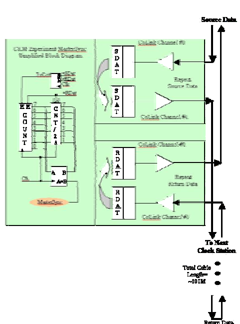
Timing Distribution System (TDS)

- Timing (or Clock) Distribution System (TDS)
  - **The Far-End of the Cable is a Common Reference for all Receivers**
  - **Reference can be Determined by: T = (Round Trip Time)/2 Or**
  - **The Time from Incident Wave to the Reflected Wave Divided by Two**

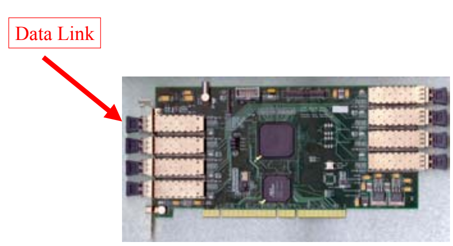


TDS: Block Diagram

- Data patterns are sent through the bi-directional communication links.
- Media delay is sensed by recovered clocks or digital patterns of the data flow.
- Compensated clock is generated with digital method.



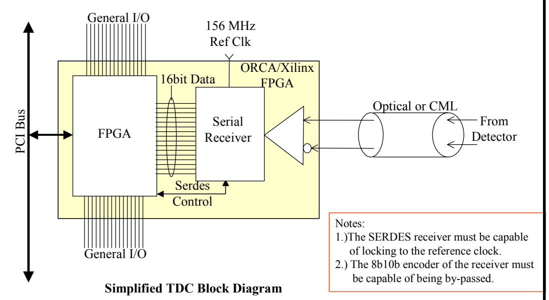
TDS: Building Block



Timing Distribution System (TDS) & Emergence Service System (ESS)

- Timing distribution system uses digital method to distribute precise timing information over the CKM detector.
- Media delay temperature coefficient is compensated with digital process.
- TDS needs bi-directional communication links -- emergency service system can use the same physical system, just add firm-wares.

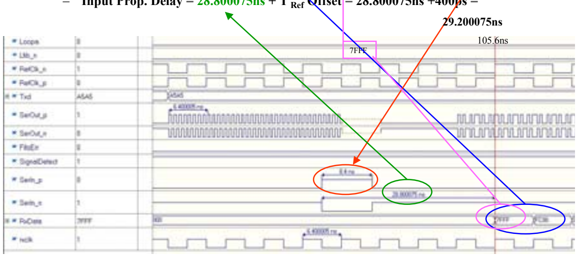
TDC, DESER Based:



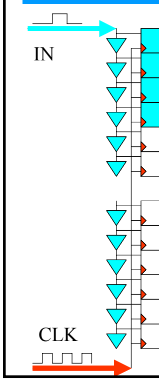
Simplified TDC Block Diagram

TDC, DESER Based: Simulation

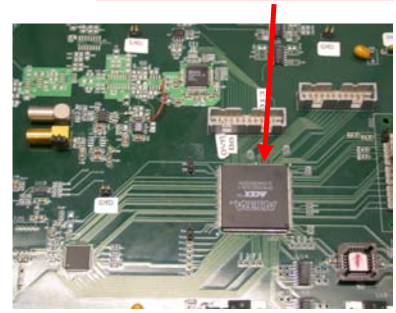
- TDC w/ 400ps Resolution
  - Input Pulse Width = 7FFF FC00 0000-> 21bits x 6.4ns/16 = 21 x 400ps = 8.4ns
  - Reference Counter Time = T_{Ref} = 105.6ns
  - T_{Ref} Offset = # of 0 bits from T_{Ref} x 400ps = 1 x 400ps = 400ps
  - Input Prop. Delay = 28.800075ns + T_{Ref} Offset = 28.800075ns +400ps = 29.200075ns



TDC, Chain Delay Based:



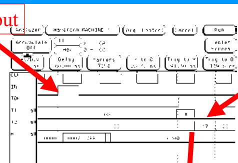
Same FPGA for ADC data handling

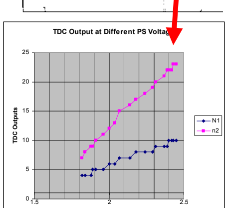


TDC, Chain Delay Based: Test

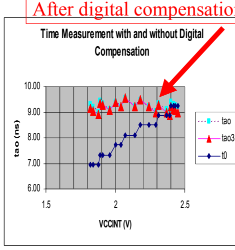
Input

TDC



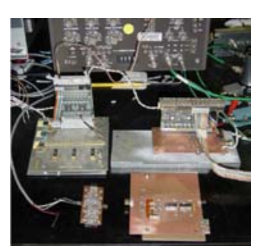


After digital compensation

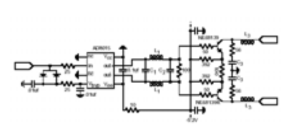


- Power supply voltage changed to create variation of the delay.
- V = 2.5 to 1.8V: the change is very big.
- 30% cell delay variation is seen.
- Digital Compensation Works.

UMS Pre-amplifier



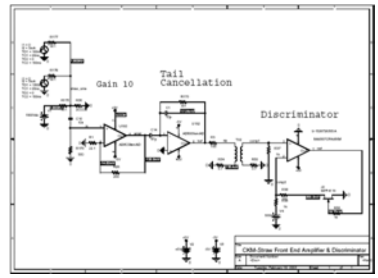
- Both UPENN-ASDQ and commercial-part-based ASD are tested.
- Left: test setup.
- Bottom: COM-ASD circuit schematics.



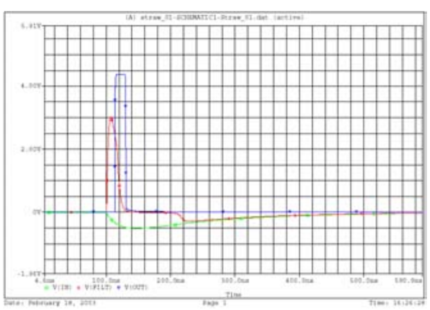
UMS Pre-amplifier

- Measured:
  - Equivalent noise charge (ENC) at input.
  - T_r
- COM-ASD works as good as UPENN-ASDQ.

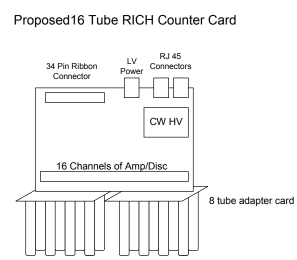
DMS Pre-amplifier: Schematics



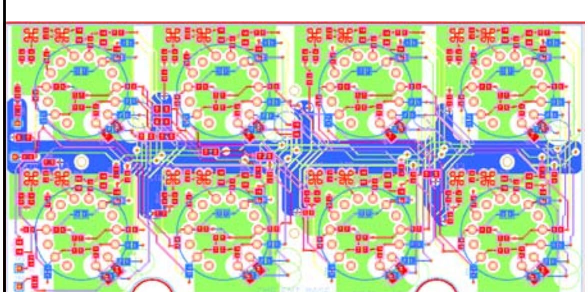
DMS Pre-amplifier: Simulation



RICH PMT Base: Structure



RICH PMT Base: Adapter Card



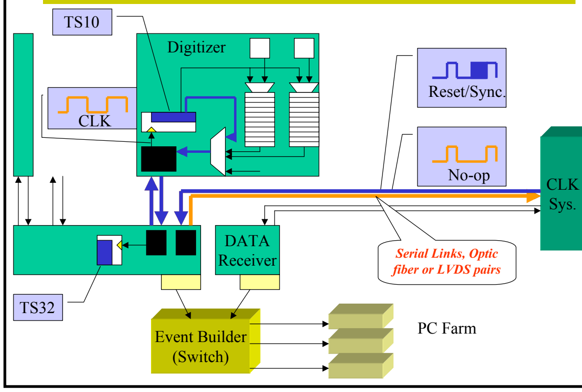
Data Structure Study

- Data sparsification is necessary in FE hardware.
- A scheme of possible data structure is provided for software trigger simulation based current knowledge on hardware.

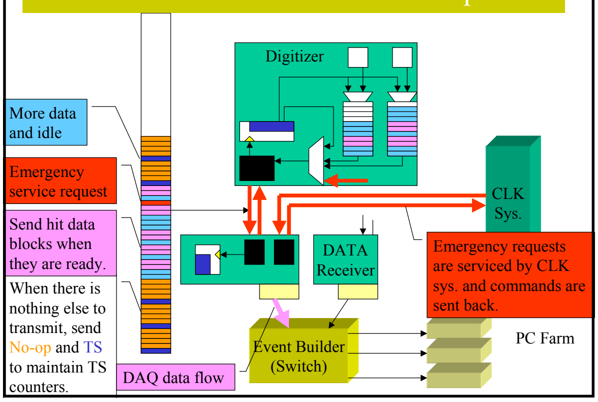
Data Structure

Group						
Centenary 255	1	1	0	1		Check sum of past centenary
	0	E	D	TS[7:0]		Time (1ns/bin)
	1	1	0	0	TS[9:6]	Ch. #
	1	1	0	0		Centenary ID = TS[15:8]
Centenary 0	1	1	0	1		Check sum of past centenary
	0	E	D	TS[7:0]		Time (1ns/bin)
	0	E	D	TS[7:0]		Time (1ns/bin)
	1	1	0	0	TS[9:6]	Ch. #
Centenary ID word: Inserted while forming Millenary	1	1	0	0		Centenary ID = TS[15:8]
Millenary Header	1	1	1	1	Millenary Check Sum [11:0]	
	1	1	1	1	Millenary Word Count [23:12]	
	1	1	1	1	Millenary Word Count [11:0]	
	1	1	1	1	Unified Channel Number [23:12]	
	1	1	1	1	Unified Channel Number [11:0]	
	1	1	1	1	Reset ID [3:0]	Millenary ID [31:24]
	1	1	1	1	Millenary ID [23:12]	
	1	1	1	0	Millenary ID [11:0]	

Data Structure: TS Establish Assumption



Data Structure: Data Flow Assumption



The End

Thanks