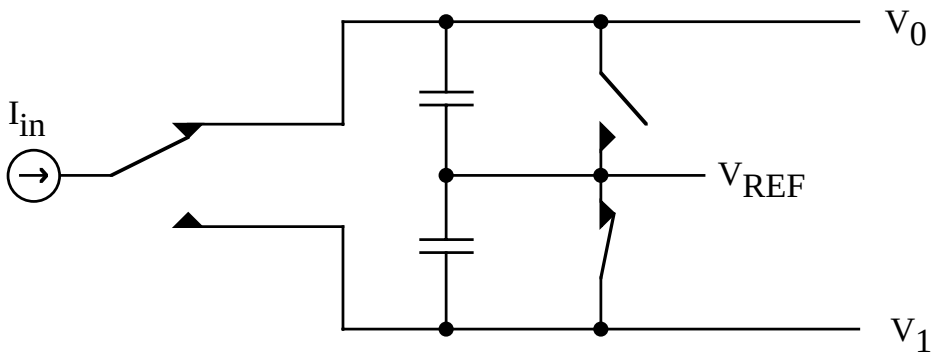
A Two-Phase Integrator for a QIE using Commercial Components



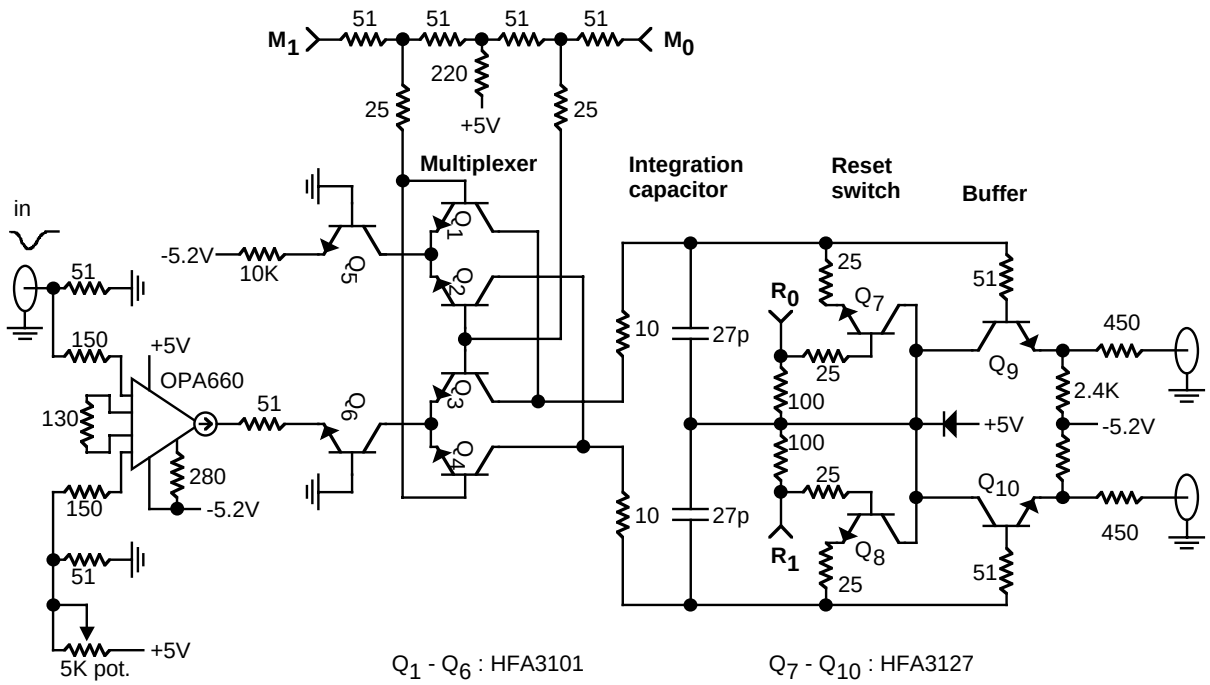
- One capacitor integrates while the other is reset.
- The ADC samples the difference

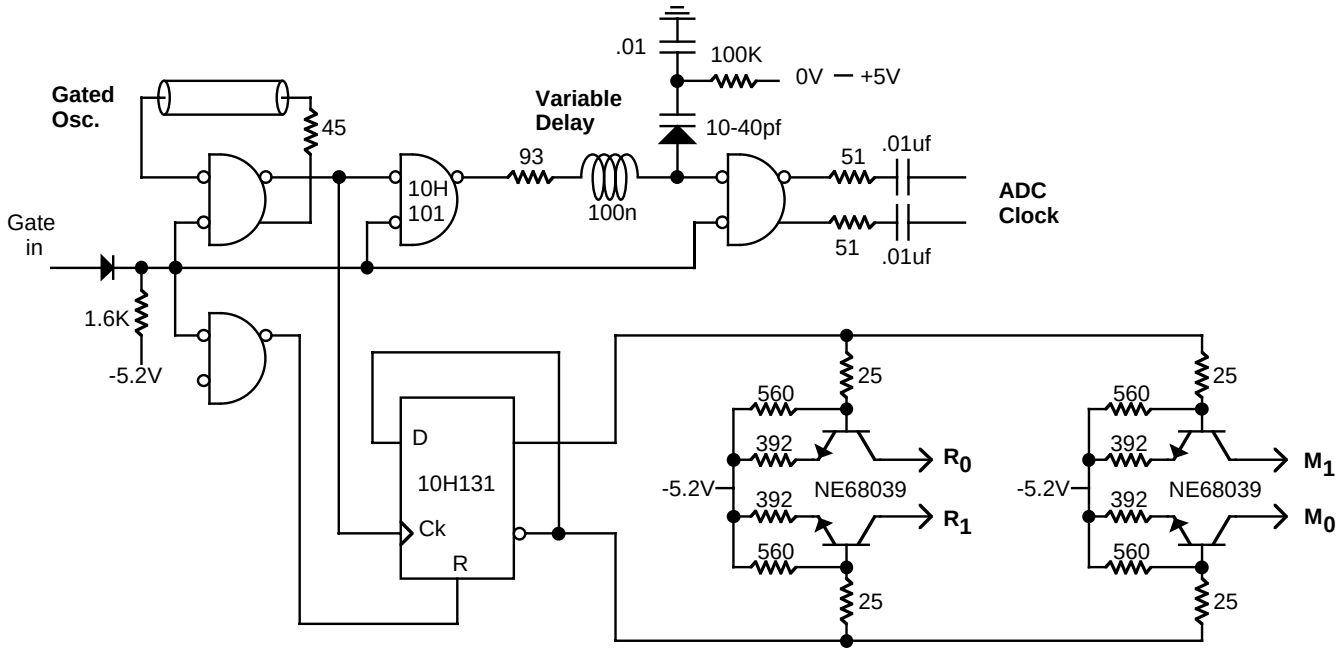
$$V_0 - V_1 = \frac{1}{C}\int I_{in}dt - V_{\mathrm{REF}}.$$

- Sign bit identifies even or odd period.

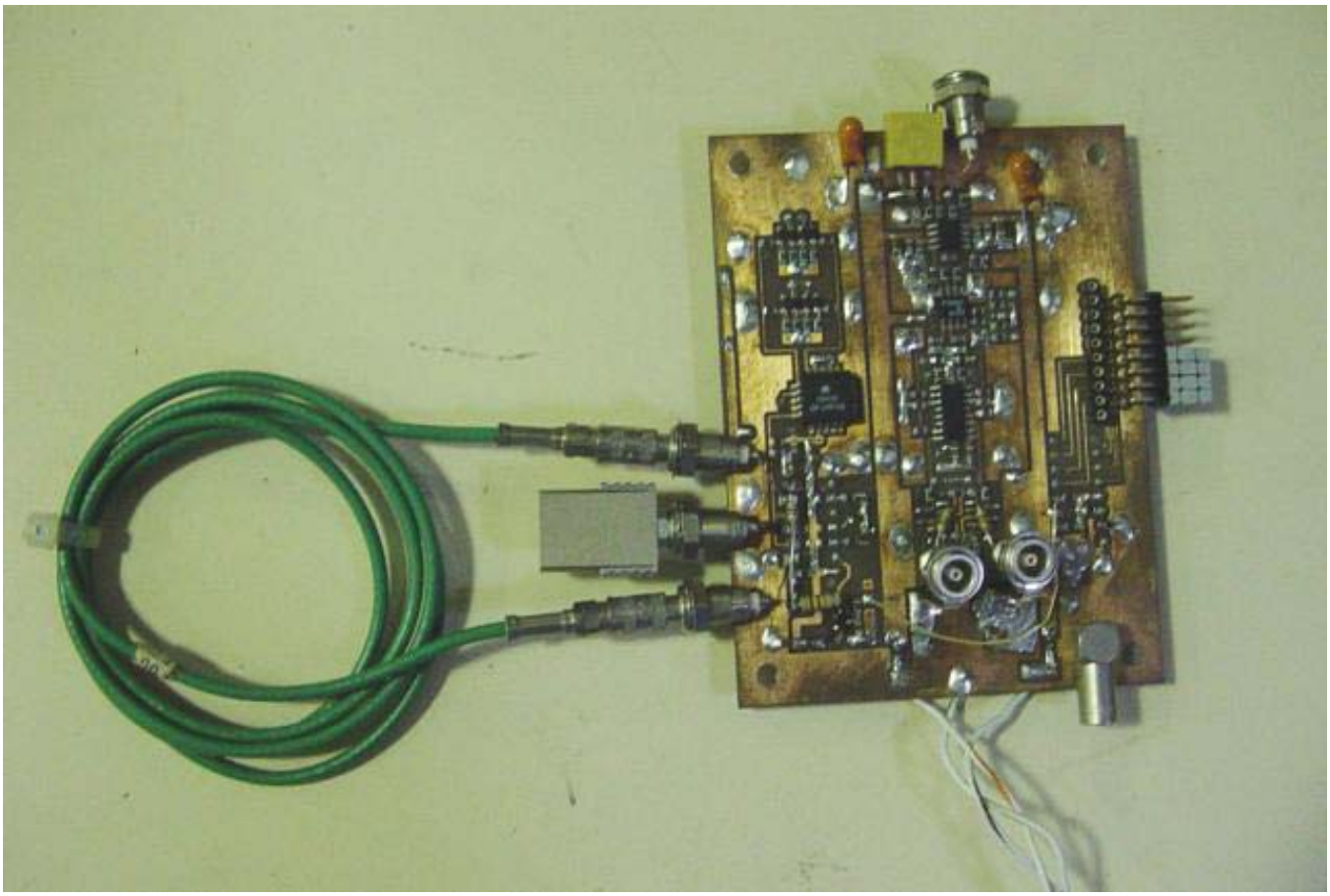
Goals: 80MHz clock, 13 bit dynamic range

After solving some problems in the original design the current circuit is;





prototype on simple two layer board



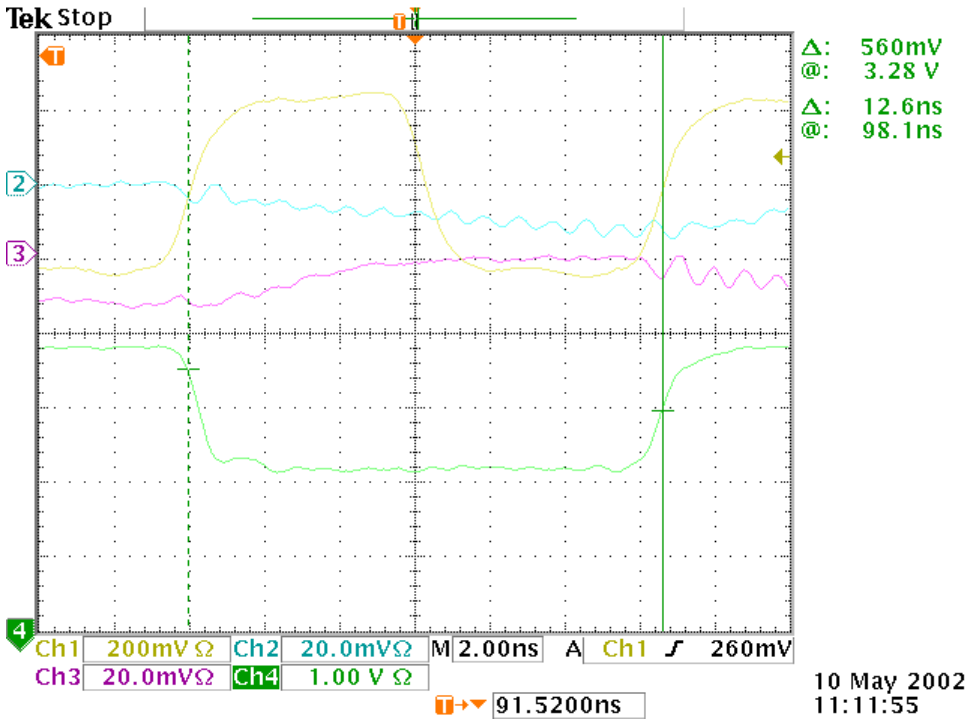
Grounded input, Phase 0:

ch 1: 80MHz Clock

ch 2: Capacitor 0 integrating quiescent current

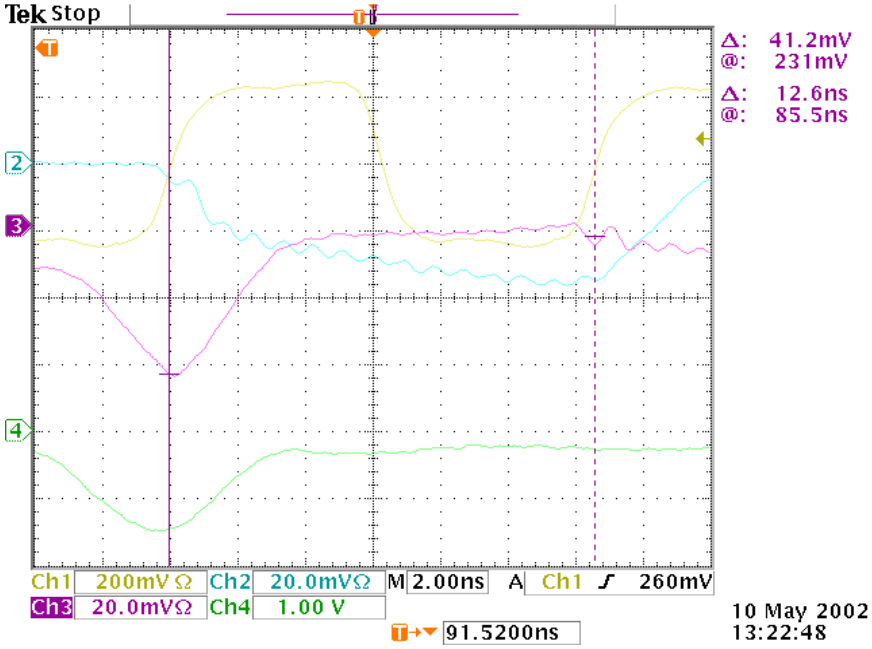
ch 3: Capacitor 1 reset to VREF

ch 4: R0

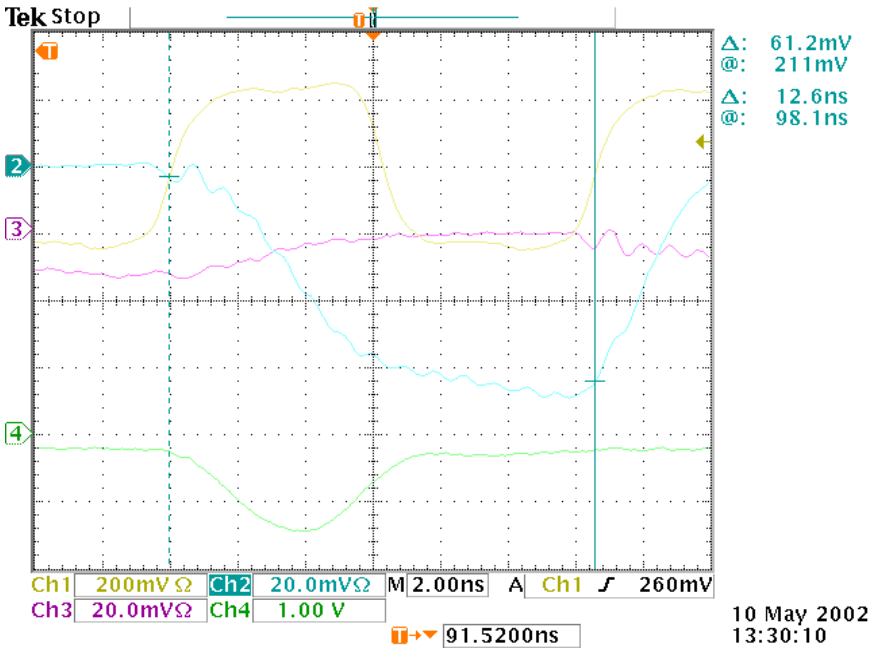


Note: cursors mark measurement points.

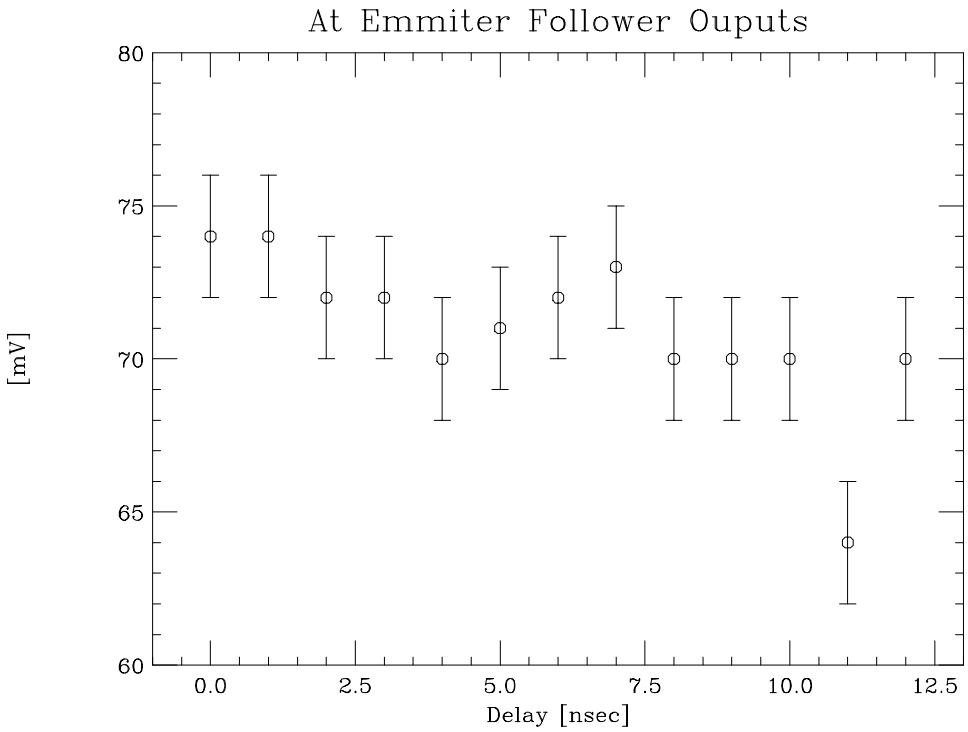
8ns pulse split between two phases



8ns pulse contained in one phase



Measure two-bucket integral by difference between successive periods



Future Plans

Some concerns: switching transients; phase matching between ADC clock, M and R; CMRR of ADC input...

M. Larwill *et al* developing a simulation of integrator to be used as guide for improvements.

Need to combine integrator with ADC, FPGA *etc* on a single board. Same interface as QIE board.
$\Rightarrow$ Wu has nearly completed layout.

Will subject this board to the same tests as QIE

Expect several iterations to get it right.