Silicon Pixel p-Spray Sensors for BTeV

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1. Introduction

In this paper we describe the design of a group of prototype silicon pixel sensors for the BTeV experiment at Fermilab [1], which is designed to cover the "forward" region of proton-antiproton interaction point at a luminosity of $2*10^{32}$ $cm^{-2}s^{-1}$. Because of the high radiation environment the pixel detector requirements are extremely challenging. All components have to be radiation hard up to a fluence of $10^{14}cm^{-2}year^{-1}$ in the most critical region at 6mm distance from the beam.

The ATLAS pixel collaboration successfully developed for LHC a radiation hard sensor [2], which is expected to also meet the requirements for BTeV pixel detector. The design of our silicon sensor is guided by the necessity to operate the device at many hundred volts without the risk of junction breakdown or micro-discharge. For this purpose a multiple guard ring structure is used. Also, a bias grid is implemented to test the sensors under full bias before assembly. About half of the ordered devices test the hardening of the silicon itself following the ROSE collaboration results, which developed the DOFZ type low resistivity silicon with increased oxygen by diffusion [3]. Some test sensors for future developments are also included.

2. Pixel sensor design overview

The BTeV silicon pixel sensor is based on rectangular 50µm x 400µm pixel elements, and it is connected via bump bonds to a read out FPIX chip, developed also at Fermilab. The pixel is n^+-diffusion on an n-type substrate having p^+-diffusion on the other side. This structure allows pixel operation under partial depletion after substrate type inversion, thus increasing the detector's lifetime. However, a special isolation technique between pixels must be used in order to avoid electrical shorting of n^+/n pixels due to the electron accumulation layer induced by the oxide charge. We are testing the so-called moderated p-spray isolation technique, developed by ATLAS [2] that improves the high voltage stability of the device. Here the nitride layer is opened only in the middle of the gap between two pixel implants, leading to a step in effective p-spray dose along the gap since the nitride layer shadows the region beneath during the p-spray implantation.

The sensors are made on 4 inch diameter, 250µm thickness, <111> orientation, n-type, double side polished, 1-2.5KΩcm resistivity silicon wafers. At least 25% and up to 50% of the wafers' batch should be oxygenated. The TESLA manufacturing company in the Czech Republic, who produced similar sensors for ATLAS, restricted the available area on the wafer as seen in Figure 1. Before irradiation, the pixels' leakage current must be less than 50nA/cm^2 at the operating voltage, which is 200V or 1.3 times the full depletion voltage, whichever is greater and the breakdown voltage must be larger than 300V or 1.5 times the full depletion voltage, whichever is greater.

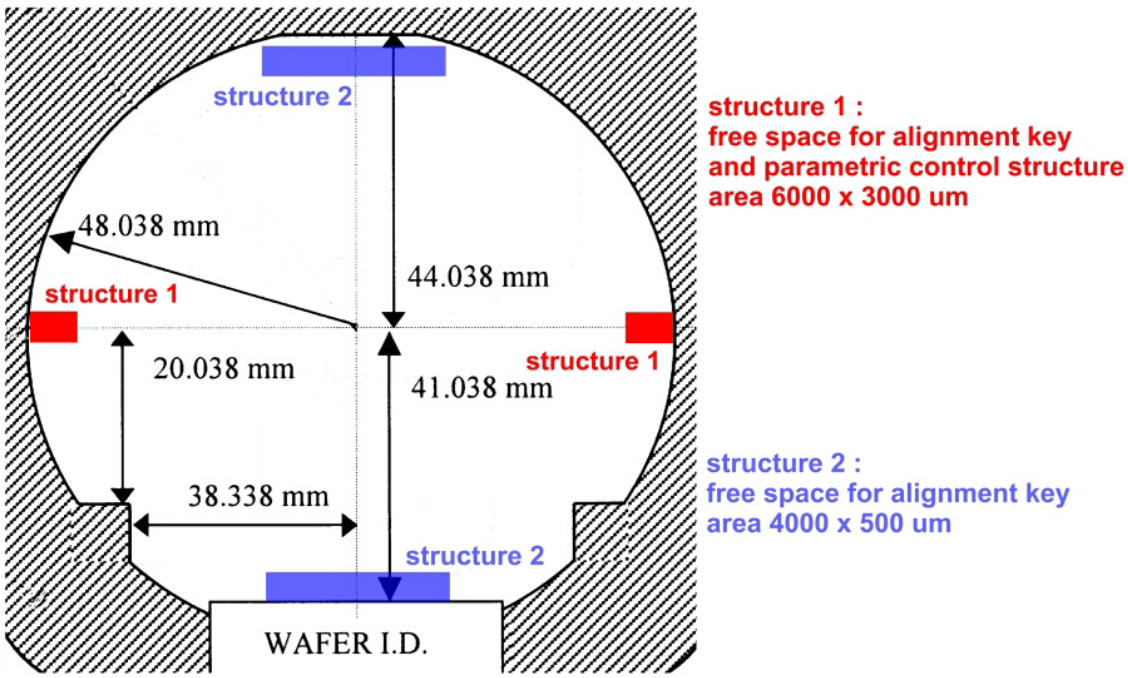

Figure 1

Considering BTeV pixel detector mechanical requirements, pixels are organized in grid tiles, which are multiples of 1, 4, 5, 6 and 8. The basic unit contains an array of 128 x 22 pixels that matches the bump pads of one FPIX readout chip. Our wafer design (see Figure 2) also contains miscellaneous test structures that will be described later in this paper.

Table 1

Parameter	Tile 1	Tile 4	Tile 5	Tile 6	Tile 8
Pixel area (µm^2)	9,205x6,410 =59,004,050	36,805x6,410 =235,920,050	46,005x6,410 =294,892,050	55,205x6,410 =353,864,050	73,605x6,410 =471,808,050
Total area (µm^2)	11,395x8,600 =97,997,000	38,995x8,600 =335,357,000	48,195x8,600 =414,477,000	57,395x8,600 =493,597,000	75,795x8,600 =651,837,000
Pixel area (%)	56.13	70.35	71.15	71.69	72.38
No. of pixels/tile	2,816	11,262	14,080	16,896	19,712
No. of tiles/wafer	5	1	3	3	2

Table 1 lists some general features of each tile. The pixel area parameter contains the length and width of each tile's active pixels array (as measured on the nitride layer). The length (or width) of the total area occupied by a tile is composed of the active pixel's length (or width) plus two times a constant 1040µm silicon region from the active area to the scribe line plus one scribe line width (110µm). The 1040µm region includes the bias and guard rings on the pixel-side and the multi guard ring structure on the junction-side of the wafer. The total number of pixels on a wafer is 157,694.

As mentioned, the sensors are processed in the so-called moderated p-spray technology using a Si_3N_4 mask that is not completely opaque to boron ion implantation. Our design provides a nitride mask for the junction side too, although in principal this is not necessary. No polysilicon is required and one metal layer on each side is sufficient. Alignment precision should be better than 2µm within the same side and 10µm between front side and backside. Our agreement with the manufacturer is to use the same technological processes as for ATLAS sensor that our design is following closely.

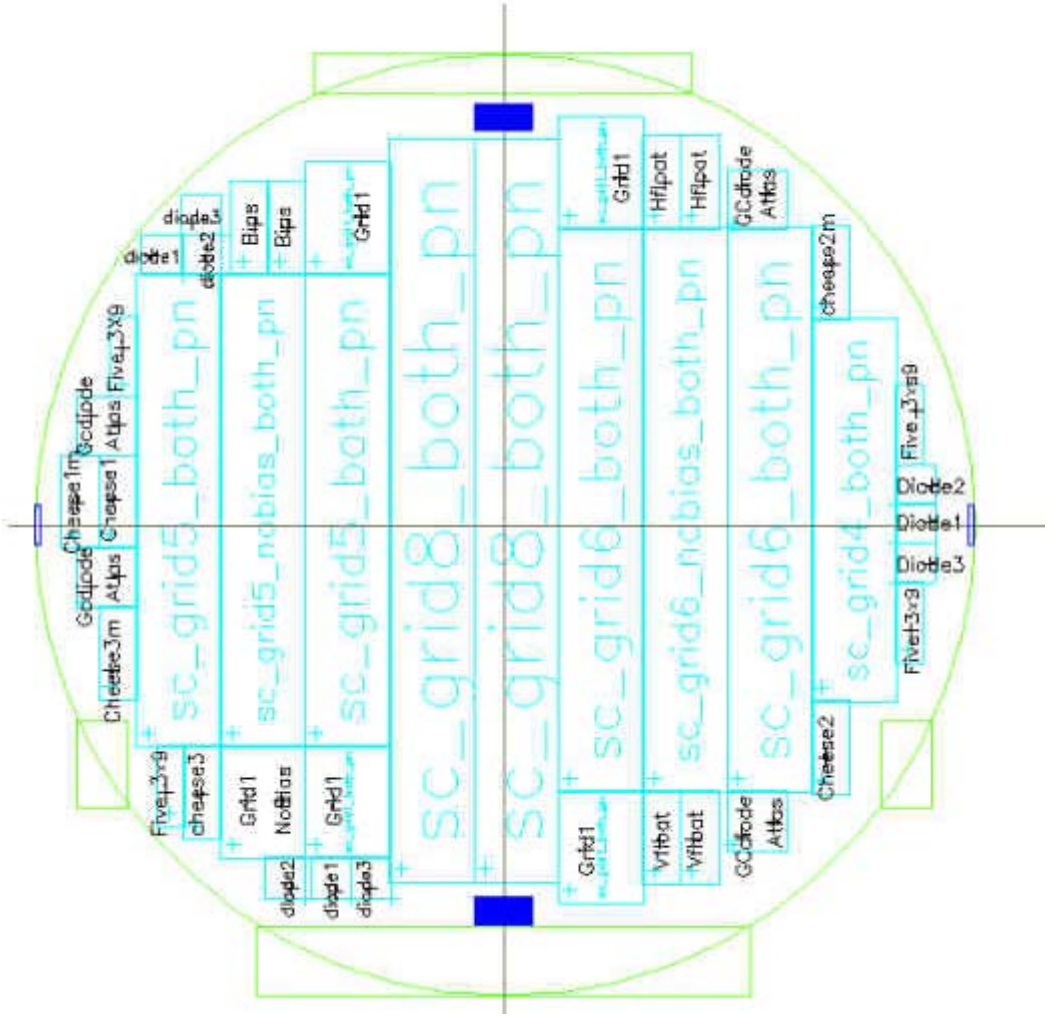

Figure 2

The following masks (layers) are used:

On the n-side (or pixel-side)	On the p-side or junction-side
M1 = n^+ pixel definition	M1 = p^+ junction definition
M2 = contact holes in the oxide	M2 = contact holes in the oxide
M3 = (contact) holes in the nitride	M3 = (contact) holes in the nitride (optional)
M4 = metal	M4 = metal
M5 = passivation opening	M5 = passivation opening

3. BTeV pixel tiles description

All tiles contain uniform arrays of rectangular 50µm x 400µm pixel elements. Considering the readout chip dimensions, each group of pixels that is read out by one FPIX chip has the 'first' and 'last' columns with longer pixels (600µm instead of 400µm length) as can be seen in Figure 3. The bump pad, normally at one end of the pixel, is 12µm in diameter. The pixel can be biased using the punch through mechanism in a geometry layout called 'bias dot' at the opposite end.

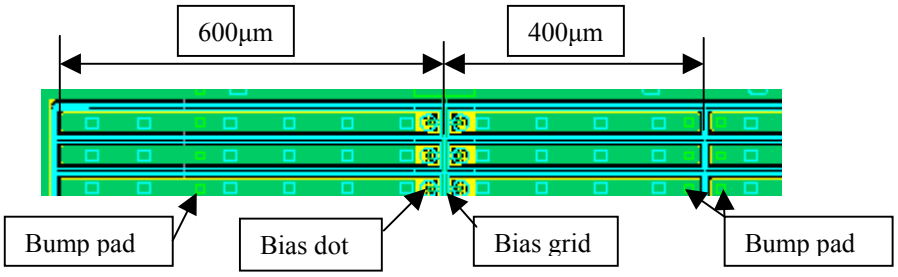

Figure 3

The dot diameter is 10µm and the punch through distance around it is 5µm making the 'hole' diameter inside the pixel n^+ active area of 20µm. The bias voltage is brought to the bias dot through a metal bias grid, which is connected to an outside bias ring, common for all the pixels in a tile. This biasing scheme has the advantage that it allows sensor testing under full bias conditions before assembling the tile with the readout chips, minimizing also the bias differences between pixels. Once the sensor has been bump bonded to its readout chip, the pixel is biased via the electronics and the grid becomes unused. Also, because the bias dot is occupying a fraction of the pixel's active area, there is a small signal loss. For this reason and considering our experience with previous sensors, we decided to provide also some Tiles that do not have this bias grid option. This is implemented for each of Tile 1, Tile 5 and Tile 6 sensors.

The pixel cells have an n^+ diffusion width of 30µm, with a distance between diffusions of 20µm. Half of this distance is p-implanted in addition, for better pixel isolation purposes, using a 10µm opening in the nitride mask. This is the so-called moderated implant feature of the design. Since this p implantation has a gap of 5µm to the n^+ pixel, the breakdown voltage of pixel's junction is not decreased too much by the p-type implantation. Each pixel has four n^+-metal contacts and the metal covers basically the full pixel's diffusion area, up to a distance of 2µm from its edge. An 83µm bias ring

surrounds all pixels inside a tile, with pad openings for external bias (see Figure 4). On the outside of the bias ring a large n^+ guard ring is extended to the tile's scribe line. Both bias and guard rings have pad openings for external bias and bump pads for eventual bias through the readout chip. In the 15µm isolation gap between these rings there is also a 5µm wide opening in the nitride layer for moderated p-spray implantation.

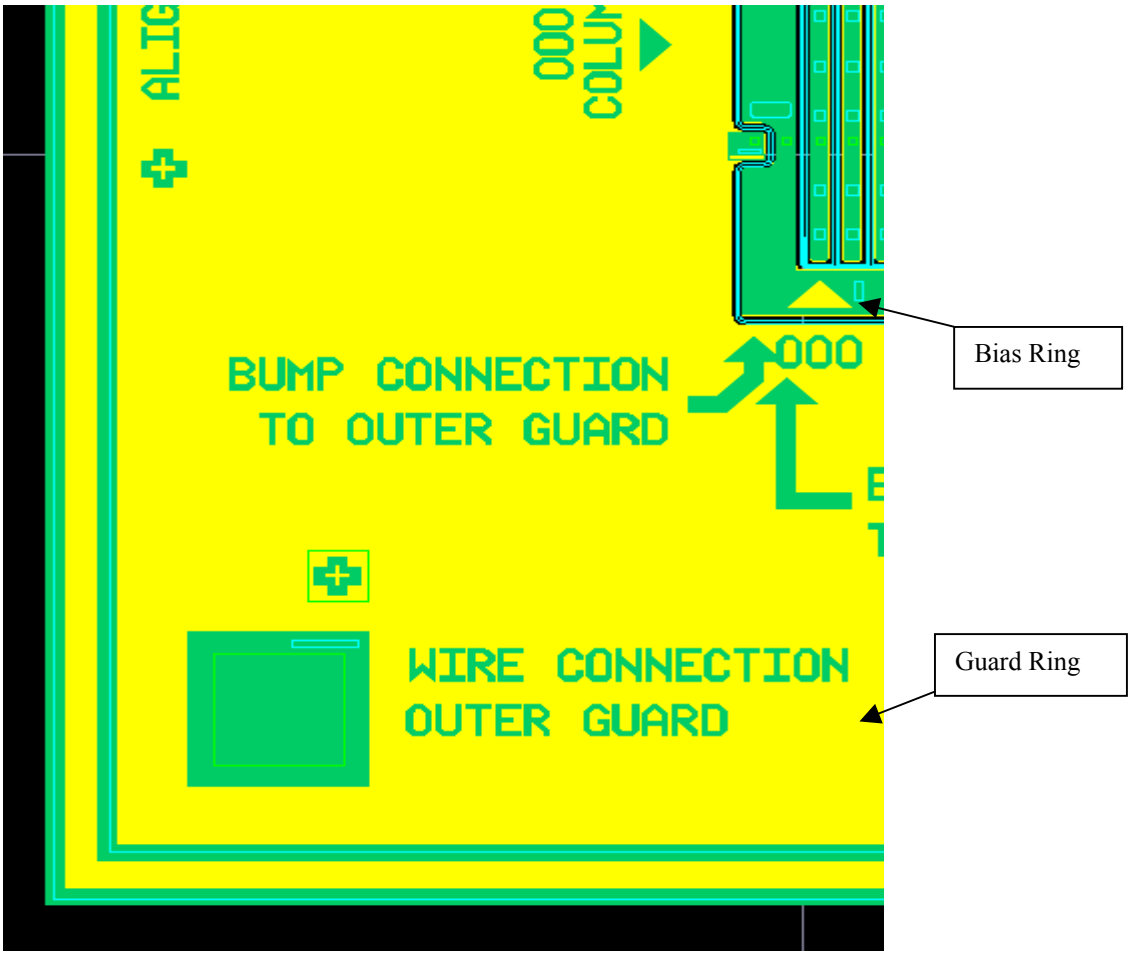

Figure 4

The p-side or junction-side of the sensor (see Figure 5) basically consists of one large p^+-diffusion aligned with the full matrix of pixels from the other side. A p^+-metal contact ring at the periphery is used and the metal is covering all the p^+-diffusion area. Laser shining holes aligned with pixels are provided for testing purposes. For high voltage and module assembly reasons, each tile has one large-opening square pad for external bias, located in the center of the first corresponding readout chip. This HV pad has an area of 3 x 3mm^2 and will be electrically connected with tile's HDI cable using a conductive epoxy.

In order to increase the breakdown voltage of the sensor and also to minimize the danger of sparks from the edge of p-side to the pixel side, a structure containing 16 guard rings surrounds the p^+ junction. The width of all rings is 10µm. For the first 11 guard

rings, the gap increases from 10.5µm to 15µm in increments of 0.5µm. The last 5 guard rings have gaps from 41.5µm to 49.5µm in steps of 2µm. The metal line on top of all these rings is wider than the diffusion width and extends more toward the inside of the structure. The full guard ring structure can thus be modeled as a chain of PMOS transistors with the metal gate shorted to source with no overlap over the drain. The breakdown voltage of the bias p^+ junction is thus the sum of the drain-source punch through breakdown voltage of each PMOS transistor in the chain.

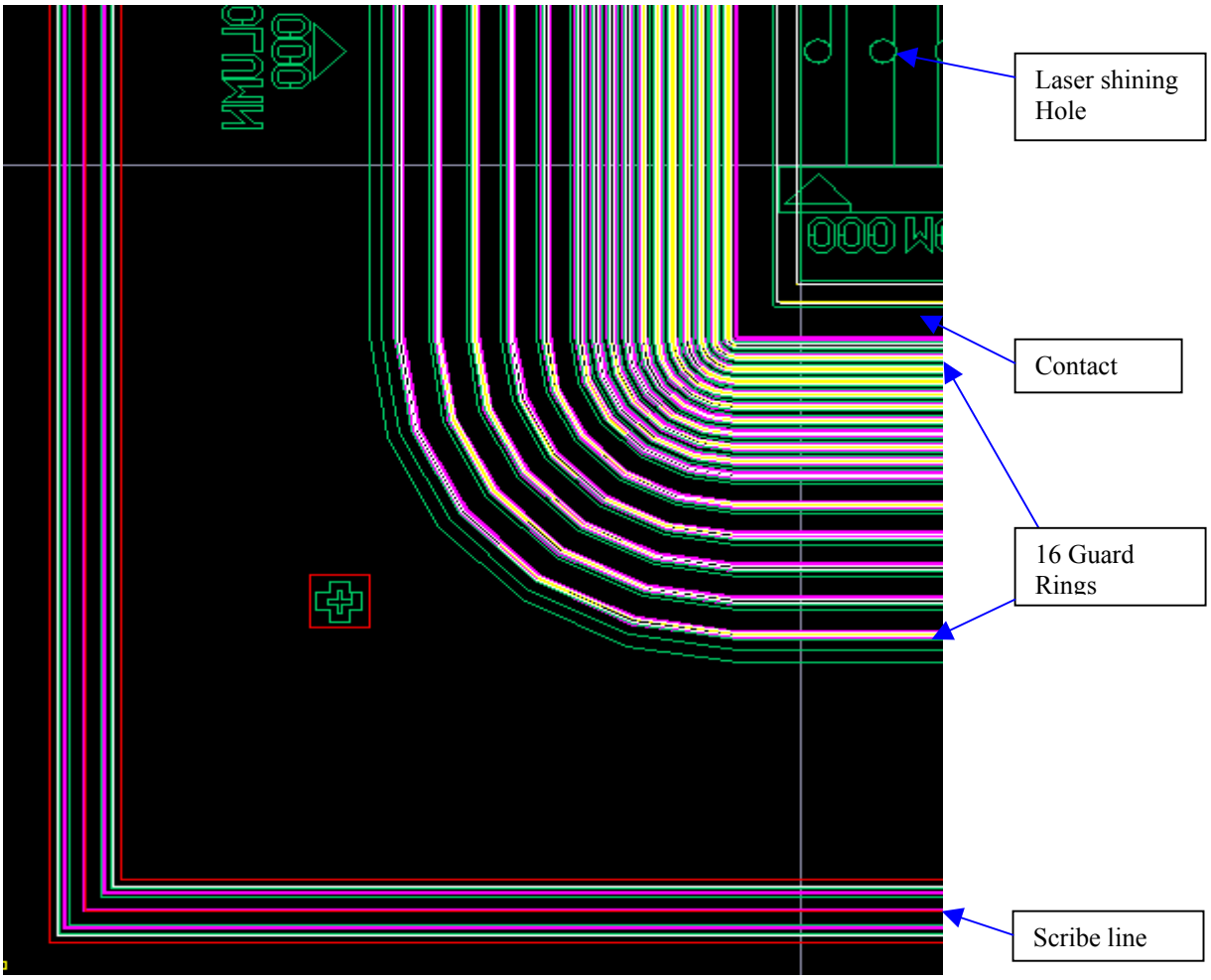

Figure 5

4. Test sensors

The test sensors have no direct use in BTeV silicon detector system, but are used to investigate new ideas for future development. We have a total of nine types of test sensors, which are all designed to have compatible readout bump pads with the 32 x 18 preFPIX2 chip. These are different flavors of the basic Tile1 unit in which only the core pixel matrix is modified and the bias and guard rings are left unchanged, as well as the full p-side.

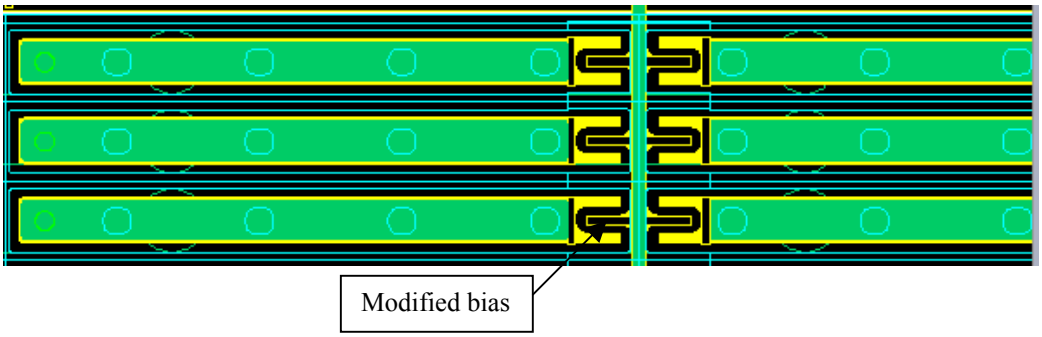

Figure 6

A first test sensor is shown in Figure 6. Here we changed the bias configuration layout: instead of the bias dot, we designed a meander-comb type bias structure. It has the same punch through length of 5µm but the total width of the punch through region (82µm) is about two times the mean circumference of the bias dot (47µm) for the same occupied area. Good experimental results on this test sensor will allow us to decrease the area occupied by the bias grid structure.

Another idea inspired by the charge division mechanism was to split a pixel in smaller floating pixels (without readout) with benefits in smaller leakage current and input capacitance per pixel but mainly in increasing the spatial resolution without increasing the number of readout channels. We implemented two versions.

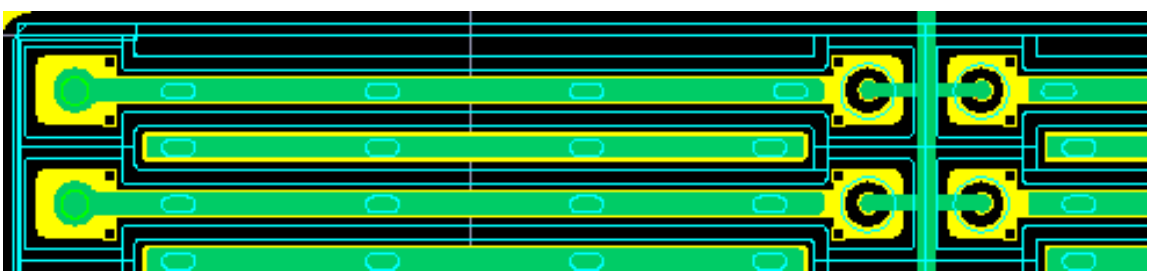

Figure 7

In a first version of floating pixel, presented in Figure 7, the 400µm pixel's length is preserved and the pixel width is reduced from 50µm to 25µm. The floating pixel has no bias grid due to space limitations. In a first order approximation, the microstrip capacitance formulas are still valid for pixels. We then obtain the same capacitance ratio:

$$\frac{C_{backplane}}{C_{intepixel}} = \frac{\ln(p/w)}{\ln(4t^2/pw)} = 0.093 \qquad \text{for } w = 13\mu\text{m},\ p = 25\mu\text{m or } w = 30\mu\text{m},\ p = 50\mu\text{m}.$$

For a pixel area of 400 x 50µm^2 we expect a $C_{backplane} = 7\,fF$ and $C_{interpixel} = 75\,fF$.

The second version of floating pixels is presented in Figure 8. Here the 50µm width is preserved and the 400µm length is divided into three pixels. A new bias grid line was introduced in this case (for this configuration we have the necessary space). One drawback of this floating pixels structure, which can not be avoided due to the readout chip we have to use, is the fact that the readout pixels are not evenly distributed within the floating pixels. Thus the charge division is unbalanced with two consecutive readout channels followed by four (without readout) floating channels.

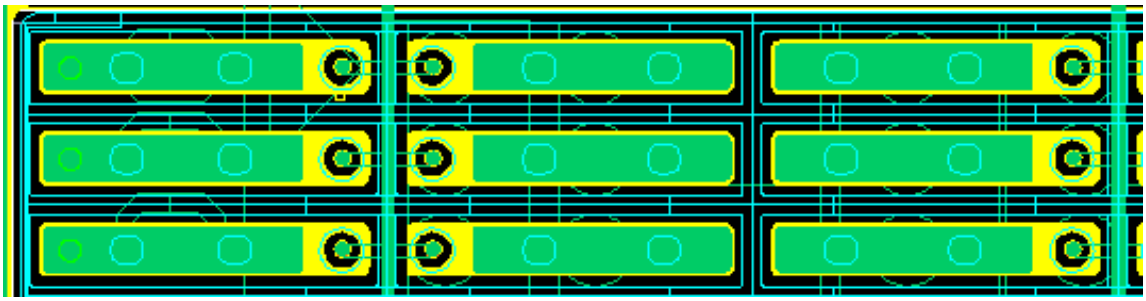

Figure 8

The next group of test sensors addresses another aspect of pixel geometry, i.e. the occupied silicon area and the ratio area over perimeter of the n^+ diffusion. These parameters affect the spatial resolution, leakage current, capacitance and noise. Starting again with the standard pixel layout, the basic idea is to decrease as much as possible the n^+ diffusion area as suggested in Figures 9 to 11.

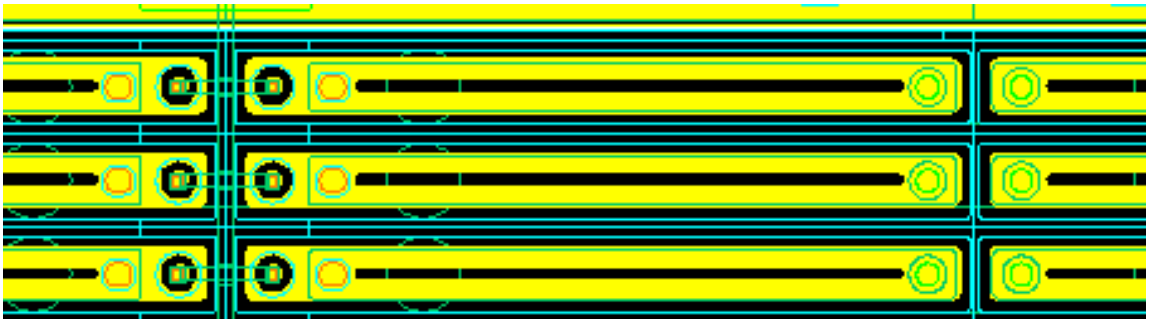

Figure 9

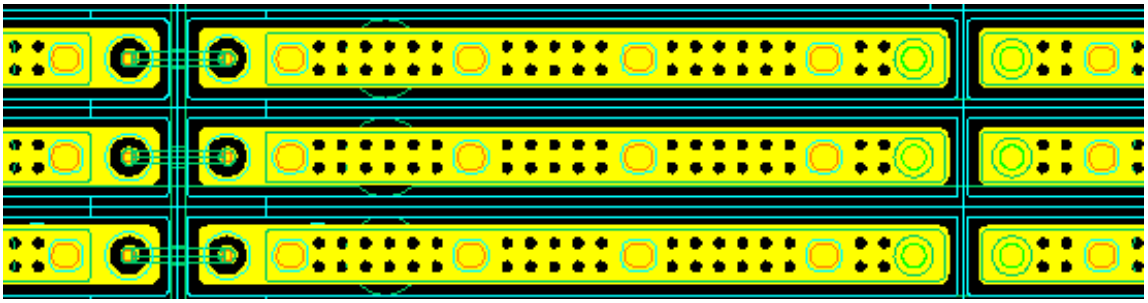

Figure 10

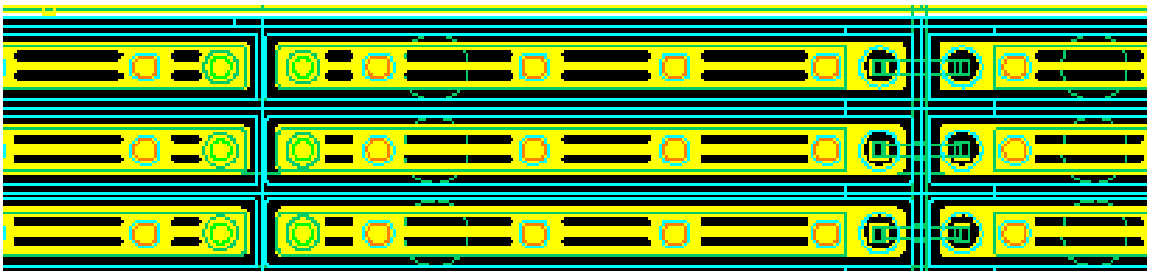

Figure 11

These layout configurations, while decreasing the pixel's n^+ area, increase the pixel n^+ perimeter and, depending on the ratio of surface over volume components of the reverse current, the total leakage current will increase or decrease consequently. Hole diameters (or width) are 6µm and the holes area as a percentage of n^+ standard pixel's area (10500µm^2) is 16.72%, 10.22% and 22.72% while holes perimeter as a percentage of n^+ standard pixel's perimeter (760µm) is 79.87%, 94.2% and 78% respectively. The top pixel metal configuration is like the Tile 1 case, covering all pixel's n^+ diffusion, and thus it is subject to adding a parasitic capacitance with the substrate when it's passing over diffusion holes. To avoid this, a second set of similar test sensors but with the metal surrounding the pixel holes is presented in Figures 12 to 14.

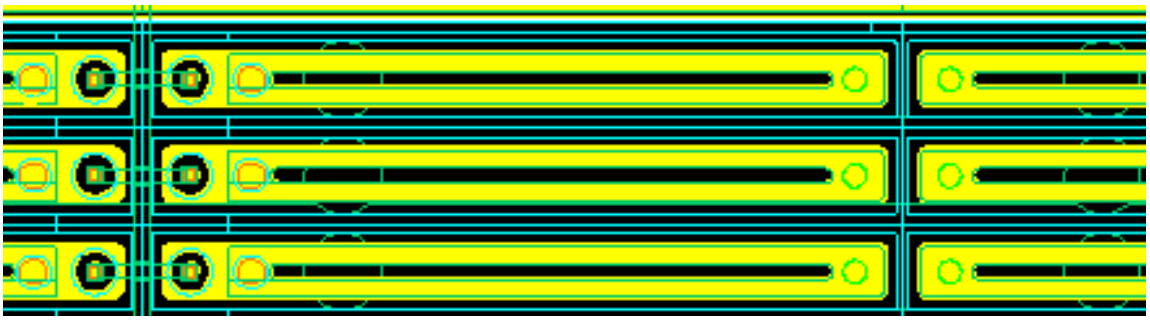

Figure 12

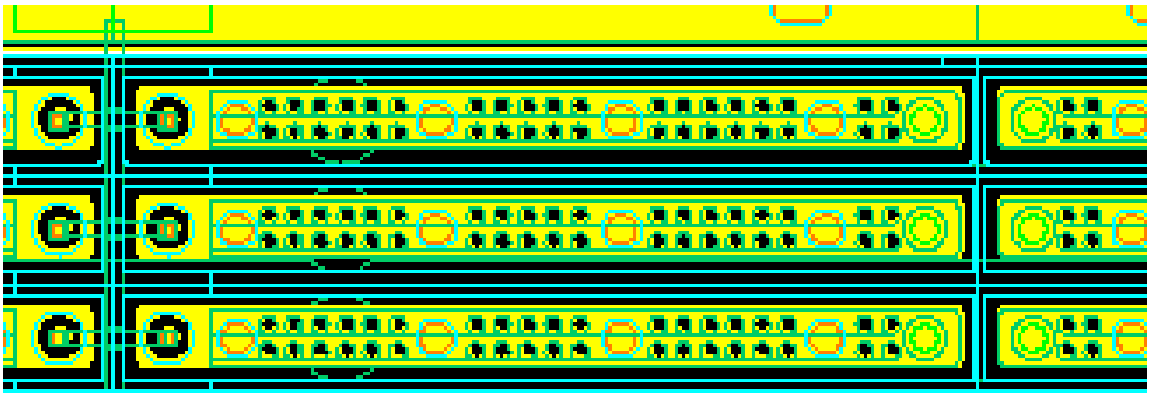

Figure 13

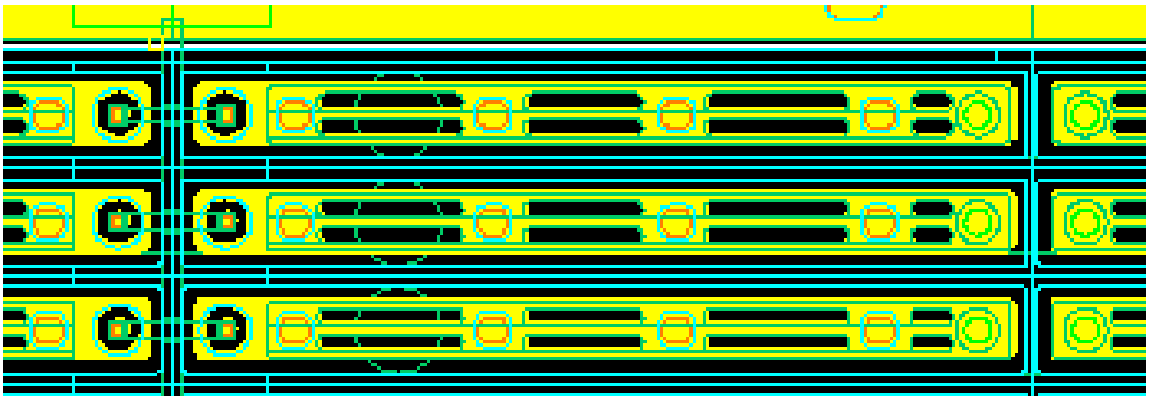

Figure 14

A last test sensor structure that we designed, which is intended to be used only for electrical measurements, contains five small arrays of pixels using pixels with the modified bias, the two floating pixels, the standard Tile 1 type and the Tile 1 type with no bias grid. The standard bias and guard rings surround the entire structure. Each small array is comprised of 3 by 9 pixels in which all pixels are short-circuited by a metal line, except the central pixel [4]. This particular configuration is useful for pixel and inter-pixel capacitance measurements. A detail of one small array is presented in Figure 15.

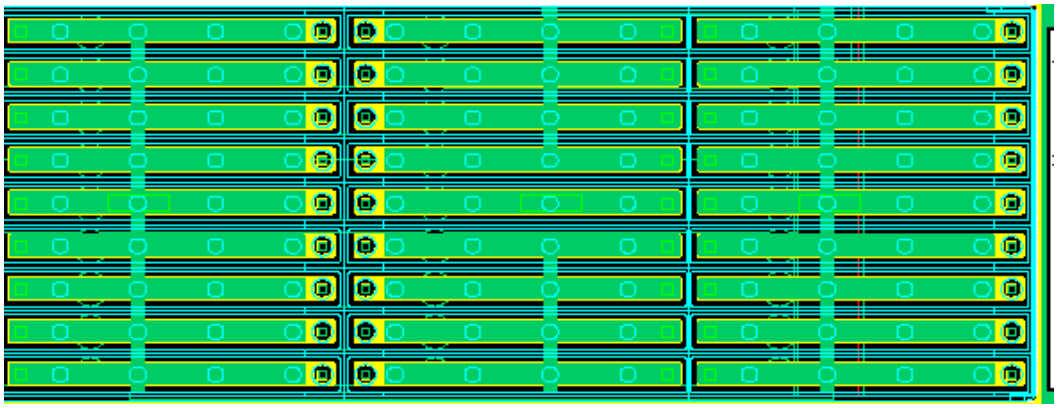

Figure 15

5. Diodes and MOS capacitors

The BTeV wafer design contains also three types of diodes with different area and perimeter, two types of gate controlled diodes, and two types of MOS capacitors.

The diode presented in Figure 16 is a square p^+-type on n substrate diode with an area of 2 x 2mm^2 and a perimeter of 8mm. The guard ring structure is identical with the one used on Tiles. On the n-side, a large n^+ diffusion is used for good ohmic contact. Two versions of this diode having different ratio of area/perimeter are also used. The structure

in Figure 17 contains a matrix of 75 x 75 holes in the p^+ diffusion. The hole diameters are 12µm with a pitch of 24µm which means a 15.9% reduction in junction area and a 26.5 times increase in perimeter, with respect to the diode in Figure 16.

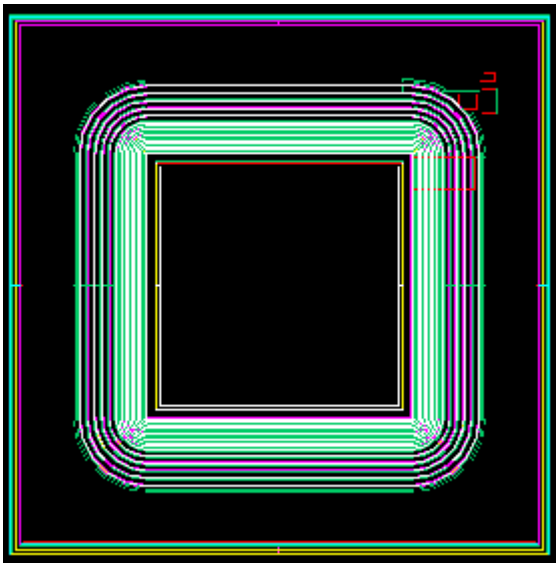

Figure 16

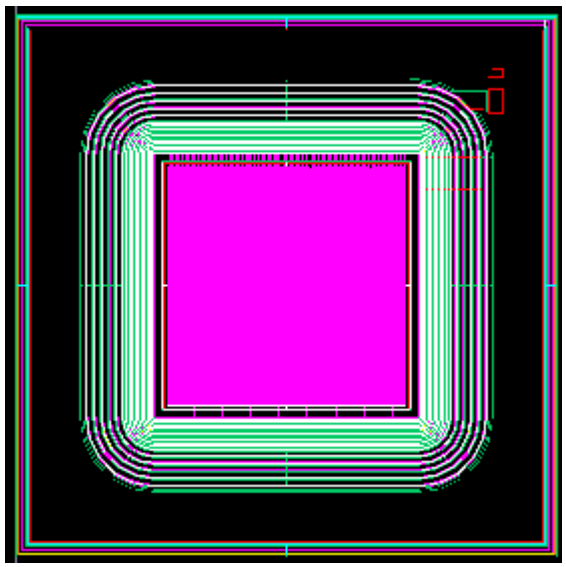

Figure 17

Similarly, the structure in Figure 18 contains a matrix of 1 x 75 longitudinal holes in the p^+ diffusion. The hole widths are again 12µm with a pitch of 24µm which means a 40.17% reduction in junction area and a 33.65 times increase in perimeter.

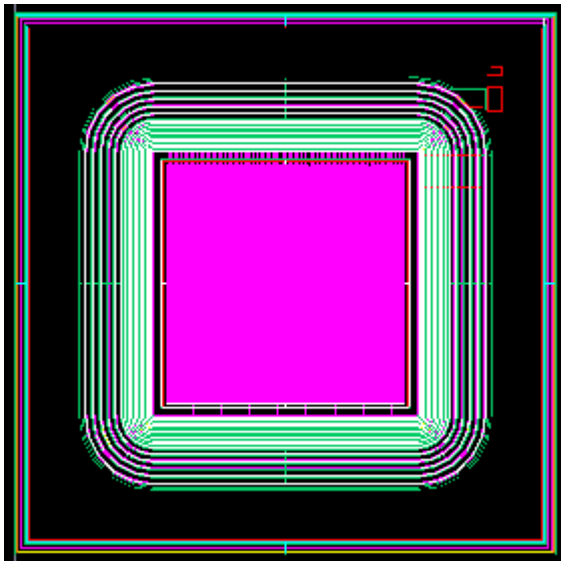

Figure 18

We have also two types of gate controlled diodes and MOS capacitor structures [5]. The structure in Figure 19 contains the active devices on the n-side or pixel–side of

the wafer while the structure in Figure 20 contains the active devices on the p-side or junction–side of the wafer. Each structure contains a gate controlled diode and a MOS capacitor with or without the nitride dielectric layer. The n-side structure (Figure 19) is an n^+/n diode with five gate controlled rings and on the p-side it has a large p^+ diffusion with a three p^+ guard ring structure. This configuration is intended to be measured after irradiation, when silicon type-inversion occurs. The p-side structure (Figure 20) is a p^+/n diode with five gates. On the n-side it has just a large n^+ diffusion for contact. This configuration is intended to be measured before irradiation.

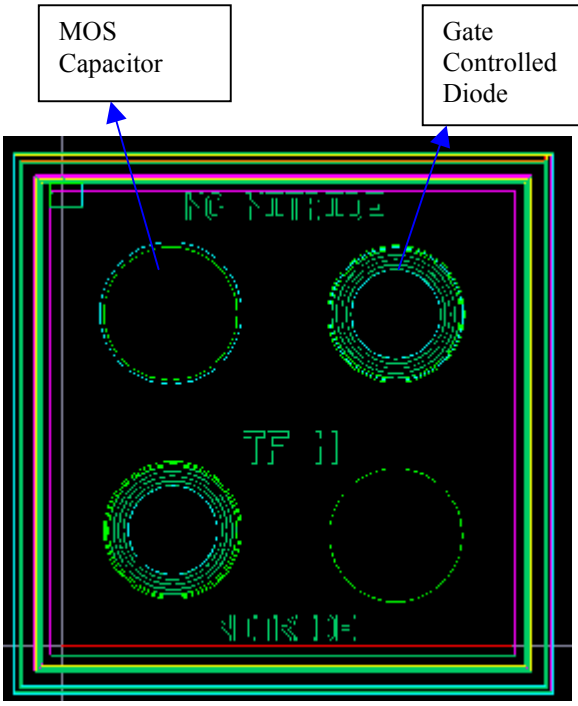

Figure 19

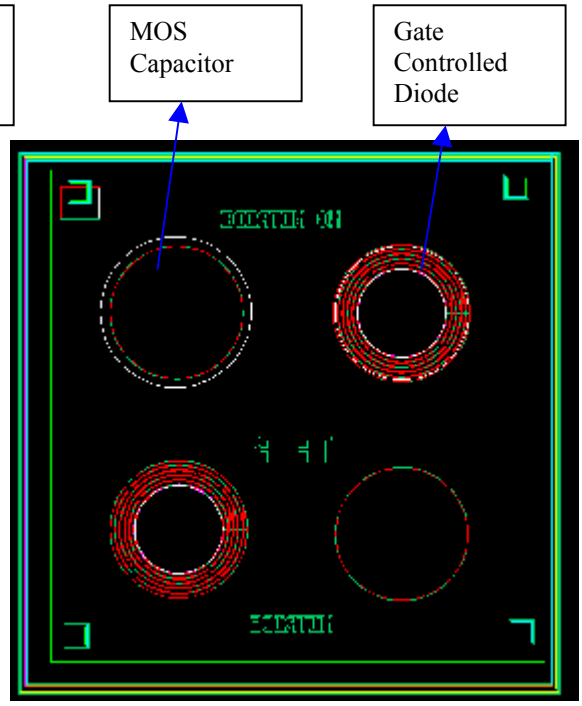

Figure 20

The circular MOS capacitors have a gate area of $17.7*10^{-3}cm^2$ (0.75mm radius). The gate controlled diode is formed by a circular diode (0.5mm radius, $7.9*10^{-3}cm^2$ area) surrounded by 5 individual gate rings, each 50µm wide with a gap of 5µm. There are several advantages to having more than one gate ring. It is possible to define the lateral extension of the gate depletion region by keeping the outer gates in accumulation. Also, several gates may be connected together to build a larger gate depletion region.

6. Other test structures

The BTeV wafer design also contains some test structures for technological process monitoring. These are organized in a “2 by N type” test pad configuration. Pad dimensions are 80µm by 80µm with another 80µm distance between pads.

Figure 21 presents the Van der Pauw structure. There are two types, one for the n^+ diffusion on the n-side and one for the p^+ diffusion on the p-side. Diffusion width, as designed, is W=16µm. For diffusion effective-width measurements, two reference distances are provided: L_{ref1}=180µm and L_{ref2}=110µm

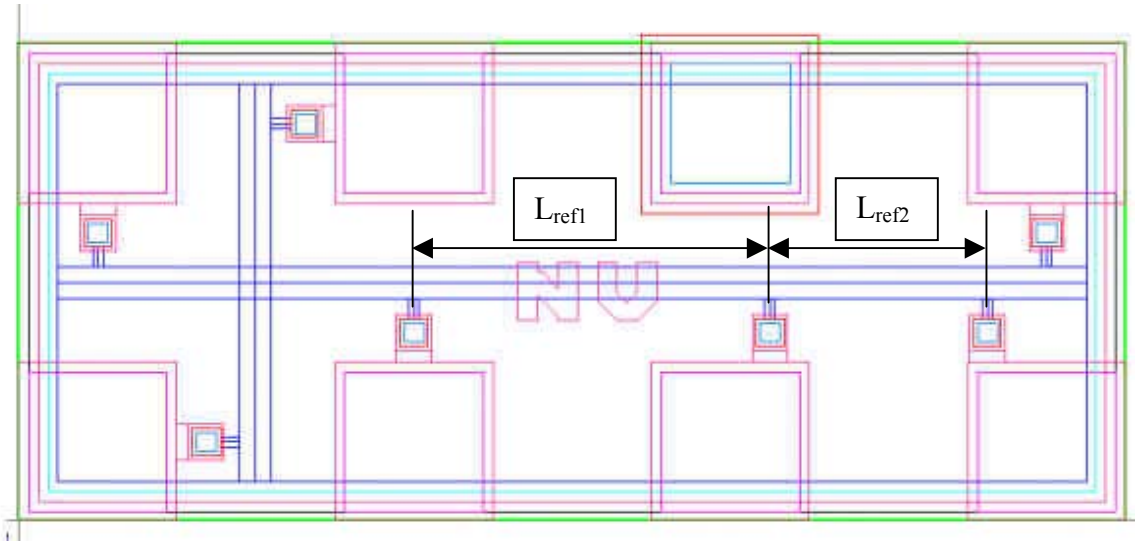

Figure 21

Figure 22 presents a structure designed to measure the electrical resistance of the contact metal-diffusion. Again, there are two types, one for the n^+ diffusion on the n-side and one for the p^+ diffusion on the p-side. The contact areas, as designed, are 4 x 4 μm^2 and 10 x 10 μm^2.

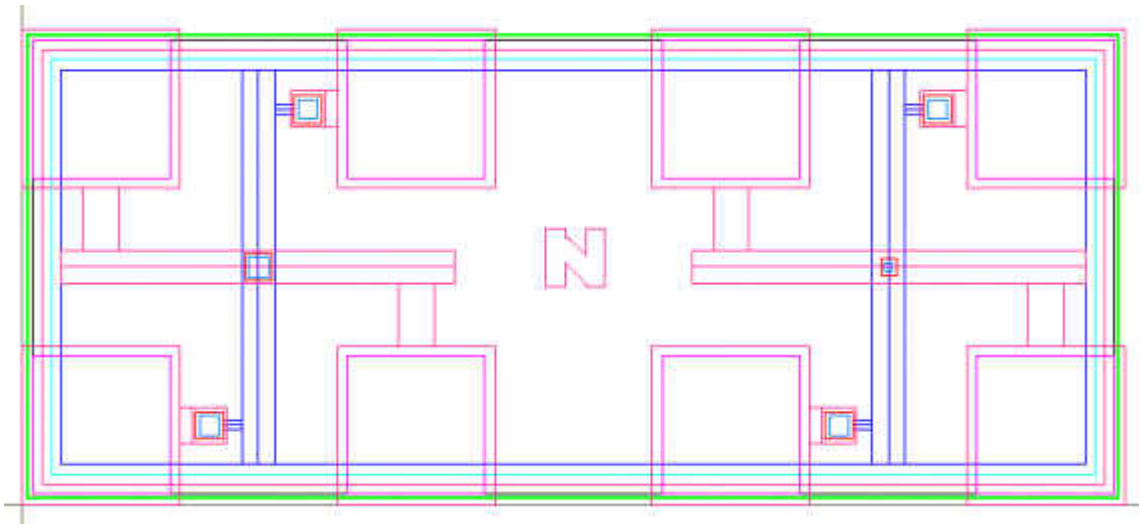

Figure 22

Finally, a chain of MOS transistors, with common source, common gate, constant channel width (W=50µm) and different channel lengths (L=25µm, 18µm, 12µm and 6µm) are presented in Figure 23. We have four structures with similar geometry: two with PMOS transistors on the junction-side of the wafer and two with NMOS transistors

on the pixel-side of the wafer. In one of the two structures, the gate insulator is the sandwich of SiO_2-Si_3N_4, and on the other one, the gate insulator is just SiO_2. The four transistors are channel-stop isolated from each other.

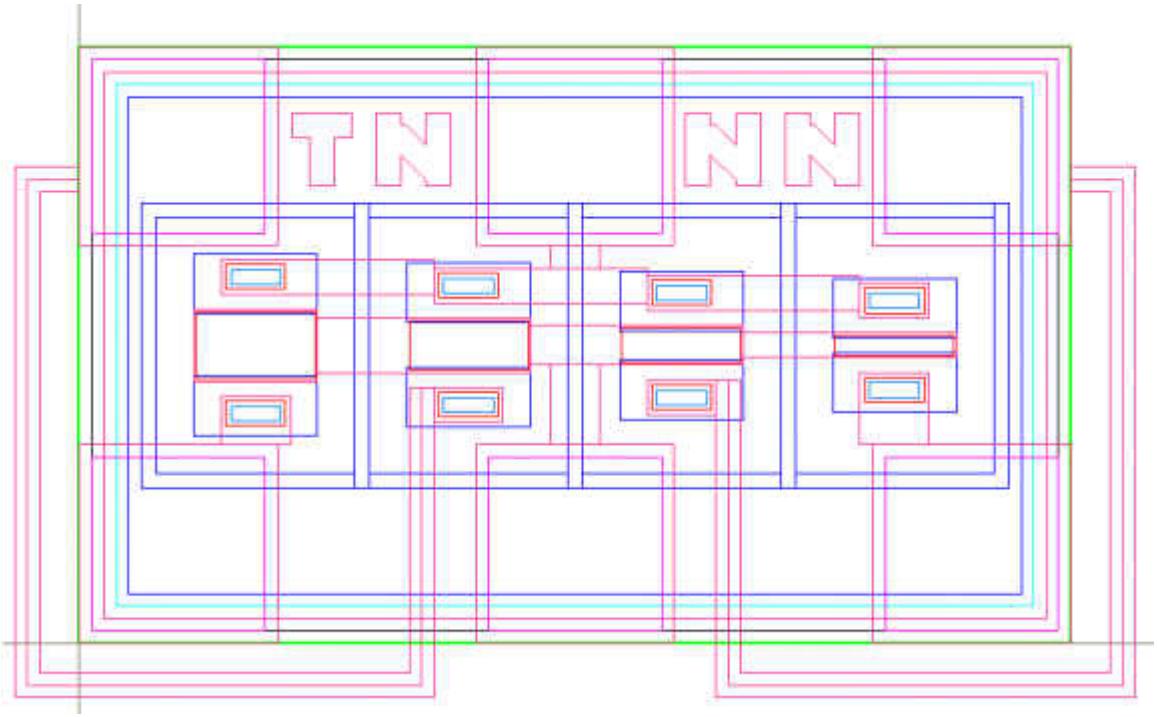

Figure 23

8. Conclusions

The features of the first BTeV silicon pixel wafer sensor prototype have been presented. The GDS design file was submitted in March 2002 to TESLA, Czech Republic for wafer processing and the first wafers are expected back to Fermilab sometime in August 2002.

9. Acknowledgements

The BTeV silicon pixel group thanks to ATLAS and RD48 collaborations for providing the necessary information. The authors wish to thank William Wester for useful suggestions and Mark Larwill for CADENCE software support.

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