

CMOS active pixel architectures for particle detection

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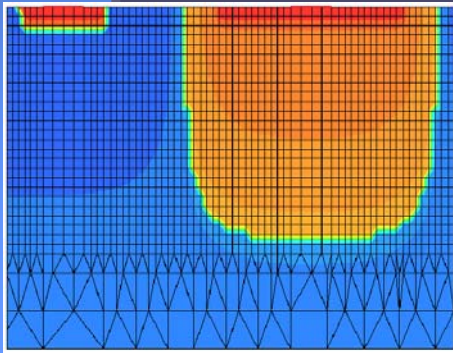
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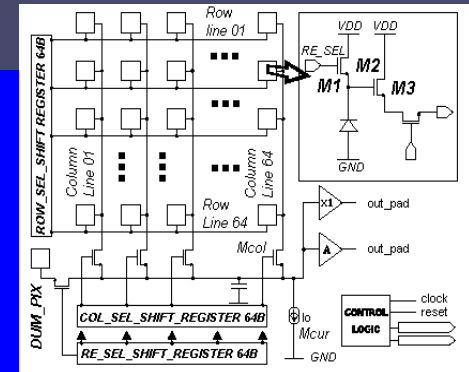
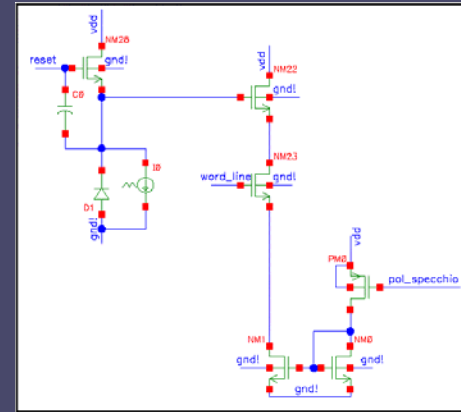
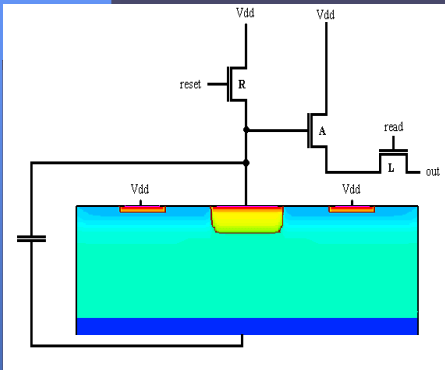
Outline

- Raps project description
- Technology: analysis and selection
- System Architecture:
 - APS (Active Pixel Sensor)
 - WIPS (Weak Inversion Pixel Sensor)
- Chip fabrication
- Future Works and Conclusion

Raps Project Description



- 1: investigation on different standard CMOS technology
- 2: optimization of the sensor device
- 3: pixel design and optimization
- 4: read-out and amplification circuitry design
- 5: digital control system design
- 6: layout and chip fabrication
- 7: test and measure



Technology Analysis and Selection

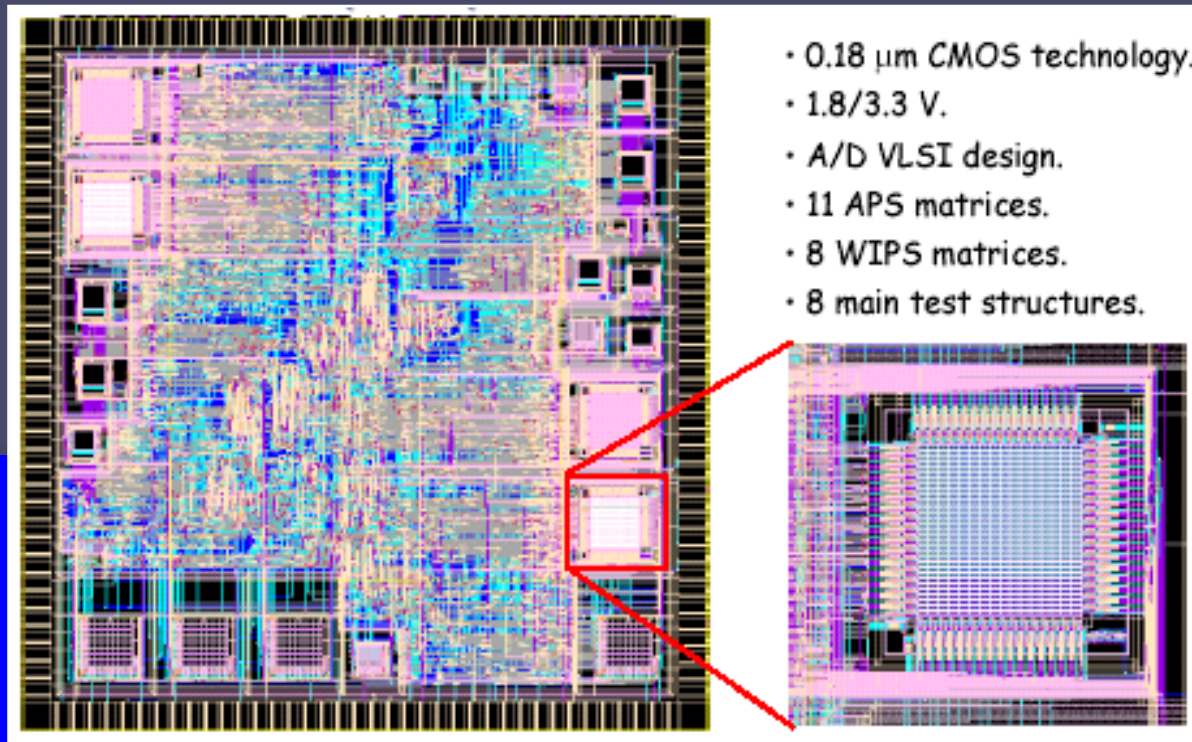
- Standard CMOS technology
- Pixel response optimization:
 - Sensitive area size
 - Parasitic capacitance evaluation



- Technology selection:
 - 0.18 μm
 - no epi-layer
 - twin-tub CMOS.

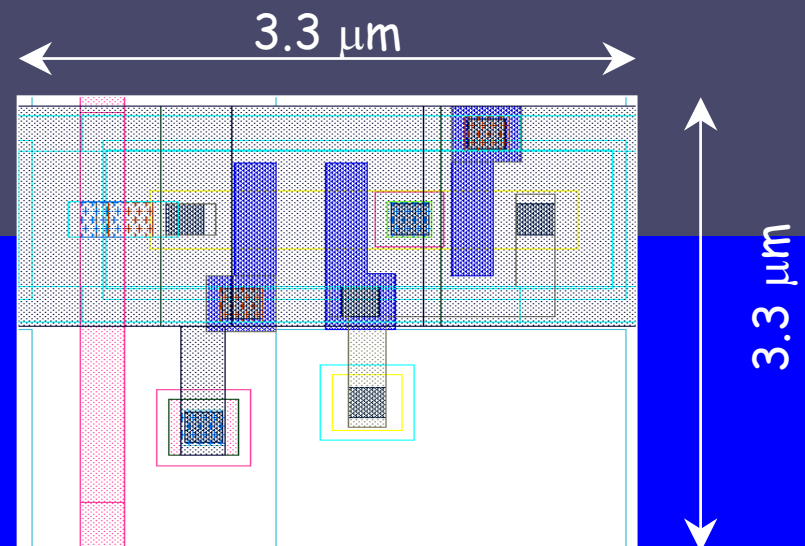
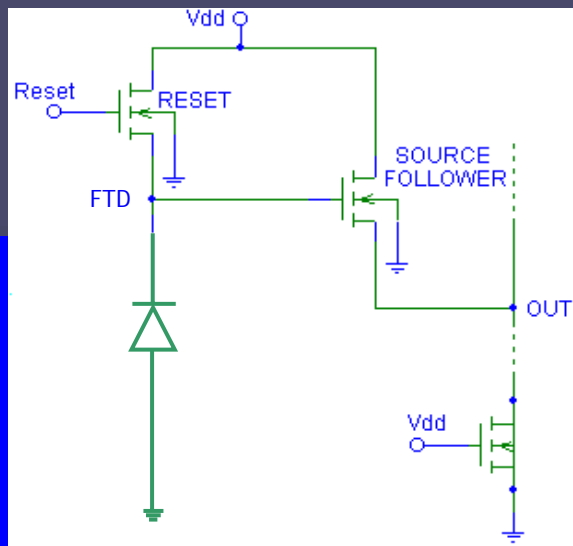
System Architecture: APS and WIPS

■ RAPS01 chip layout



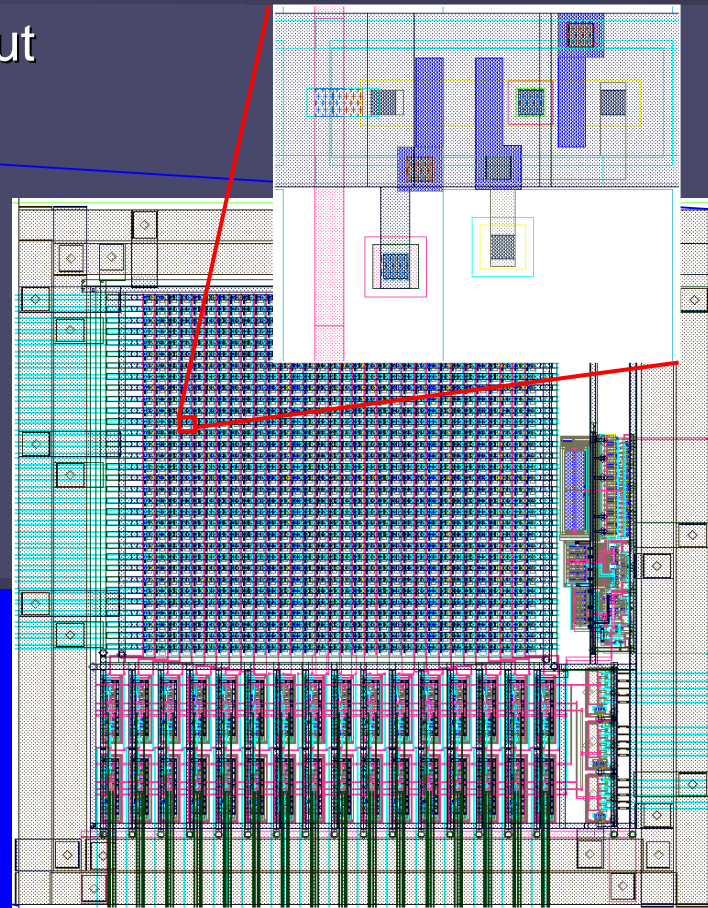
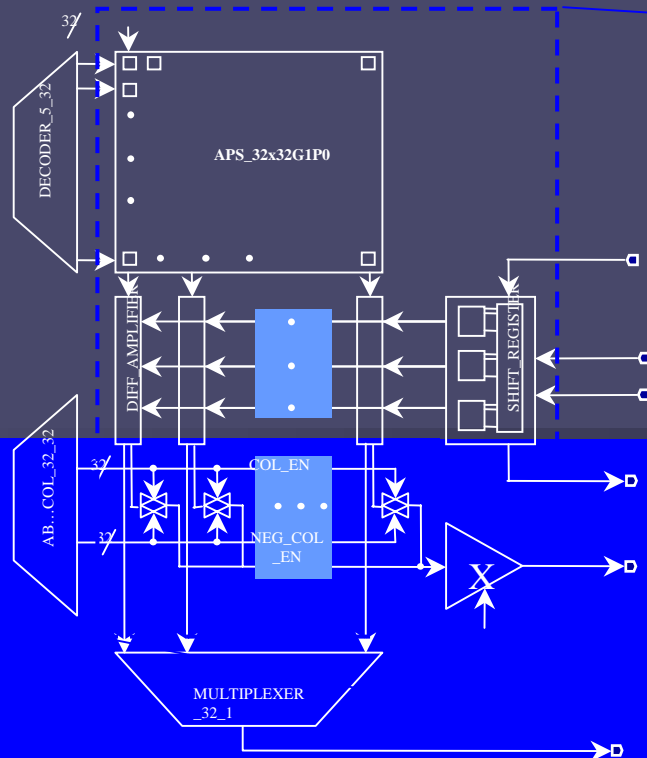
APS pixel and architecture

- APS (Active Pixel Sensor): classical solution for vision application
- Optimization of the sensitive area, maximizing the pixel output voltage swing.



APS pixel and architecture

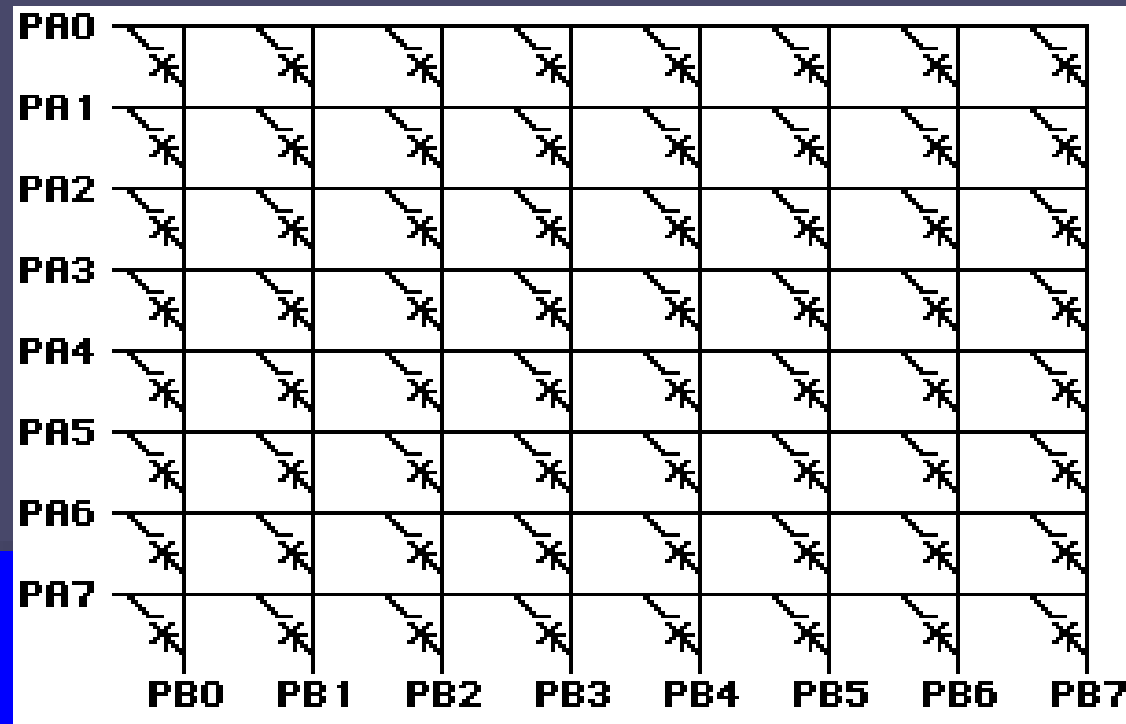
- Frame-based read-out scheme
- Serial row scan / serial output
(n x n) x Tclk [s]



WIPS pixel Idea

Problem: detect a “sparse” event in a pixel matrix.

WIPS solution: an innovative pixel for a sparse read-out scheme.

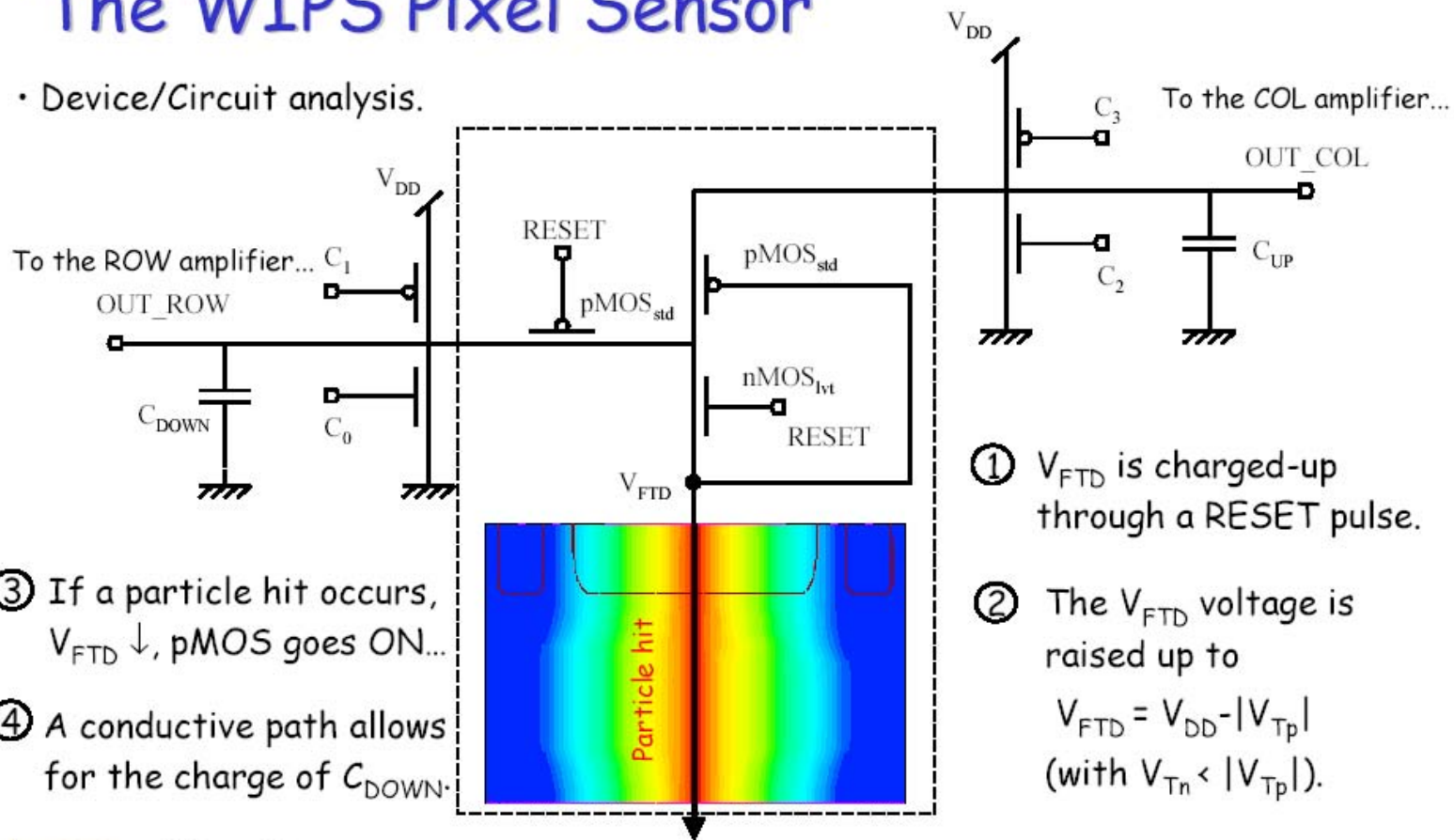


“keypad”-like structure

WIPS pixel

The WIPS Pixel Sensor

- Device/Circuit analysis.



- ③ If a particle hit occurs, $V_{FTD} \downarrow$, pMOS goes ON...
- ④ A conductive path allows for the charge of C_{DOWN} .

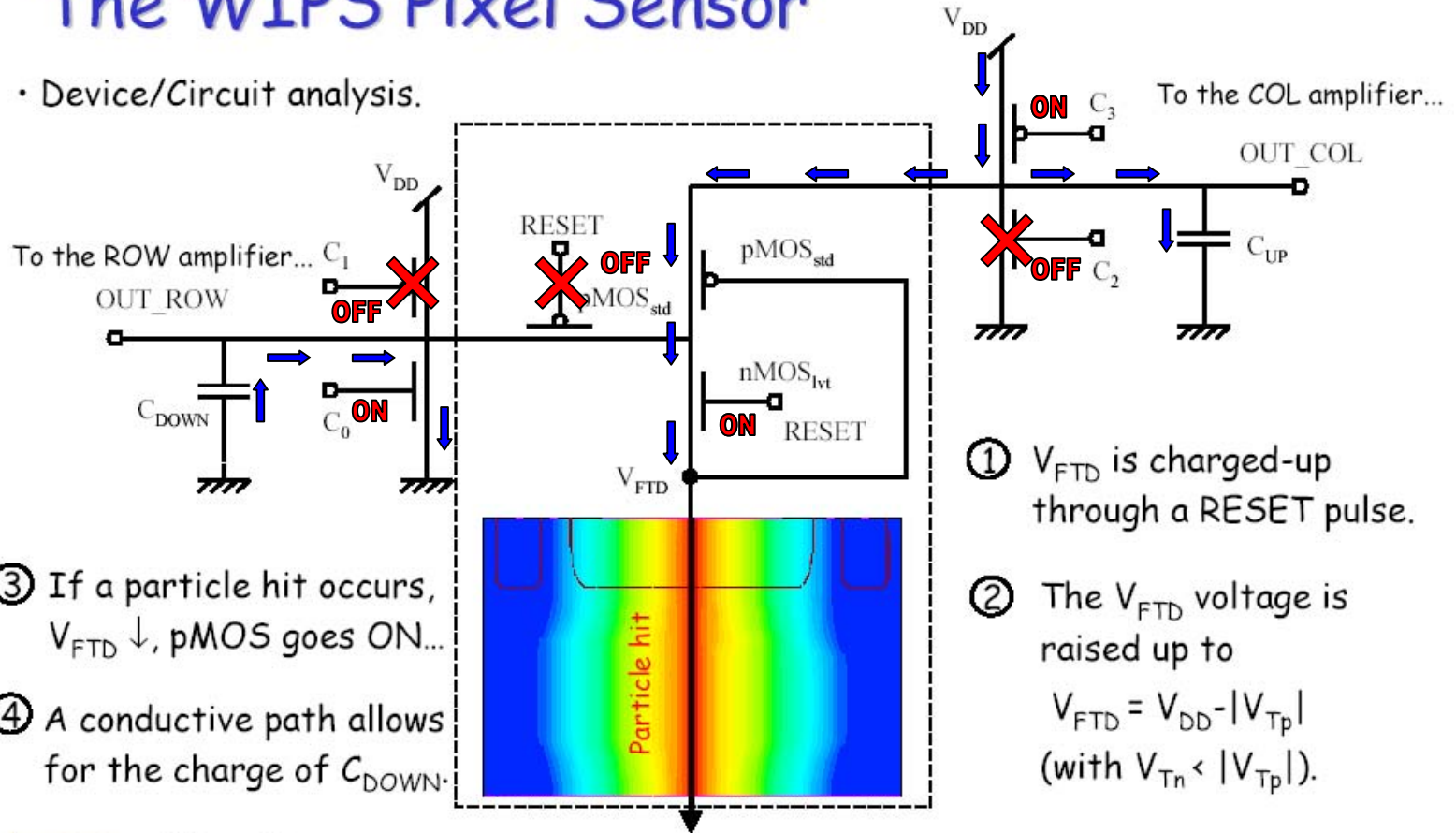
- ① V_{FTD} is charged-up through a RESET pulse.
- ② The V_{FTD} voltage is raised up to $V_{FTD} = V_{DD} - |V_{Tp}|$ (with $V_{Tn} < |V_{Tp}|$).



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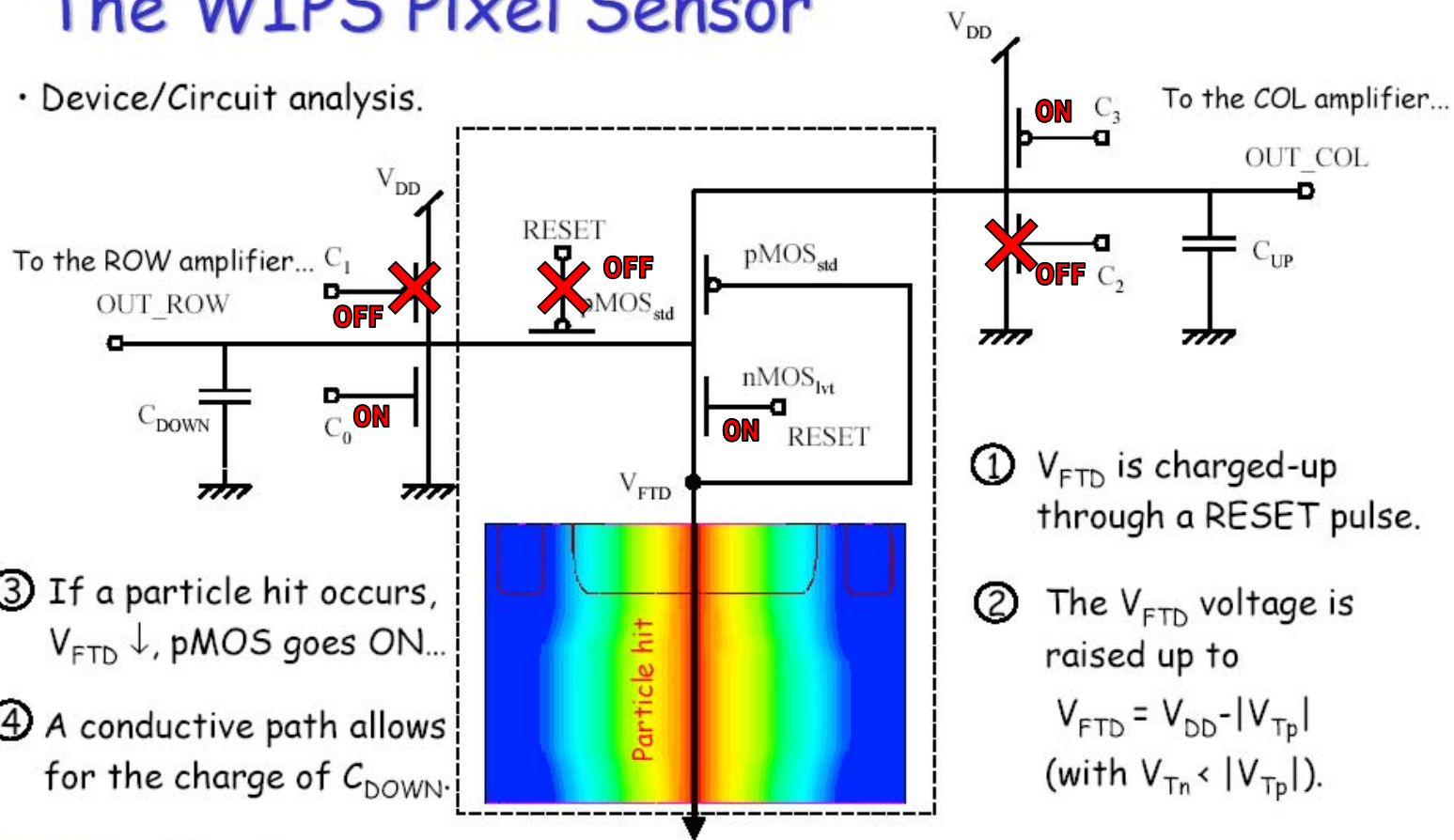
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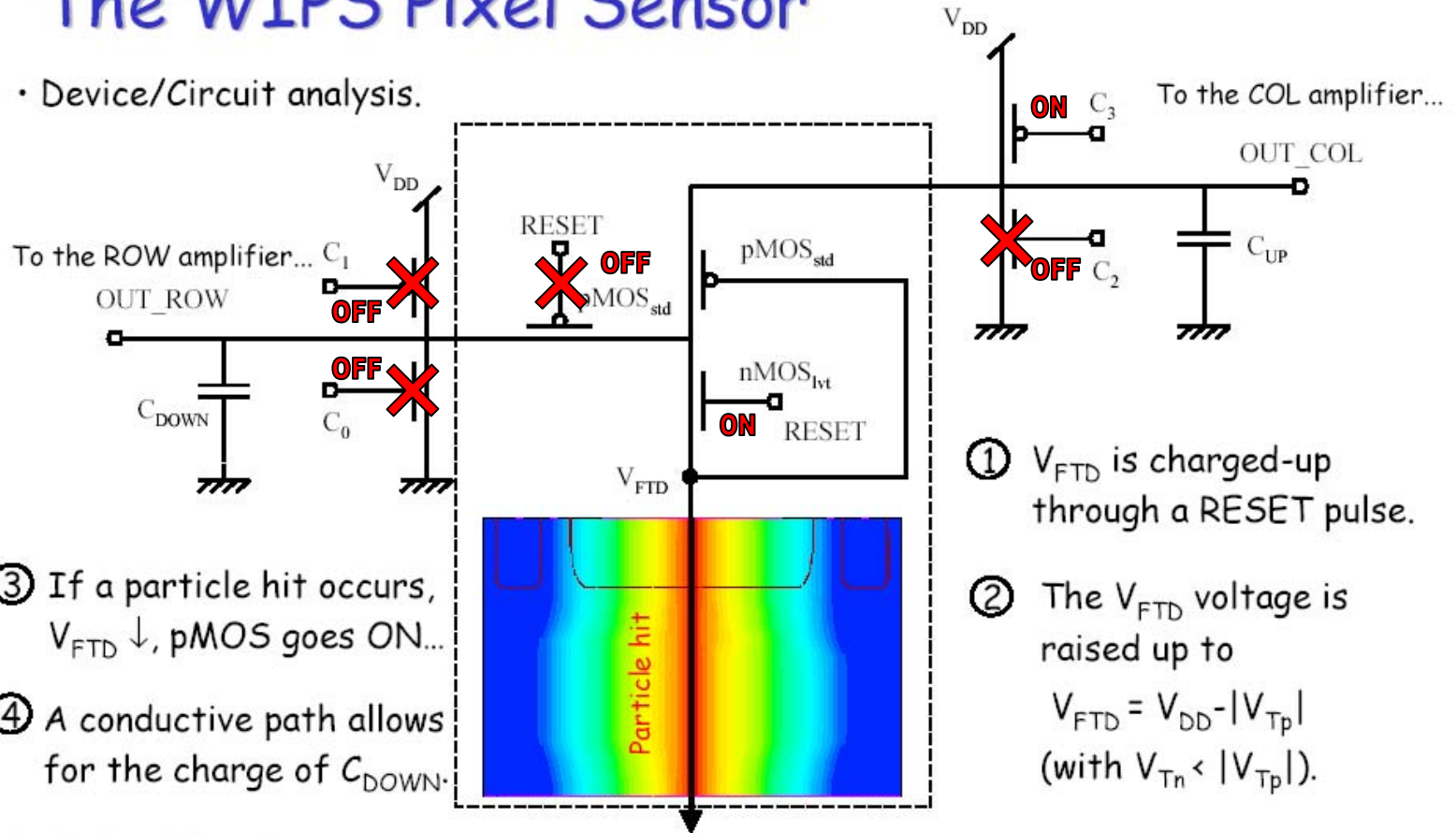
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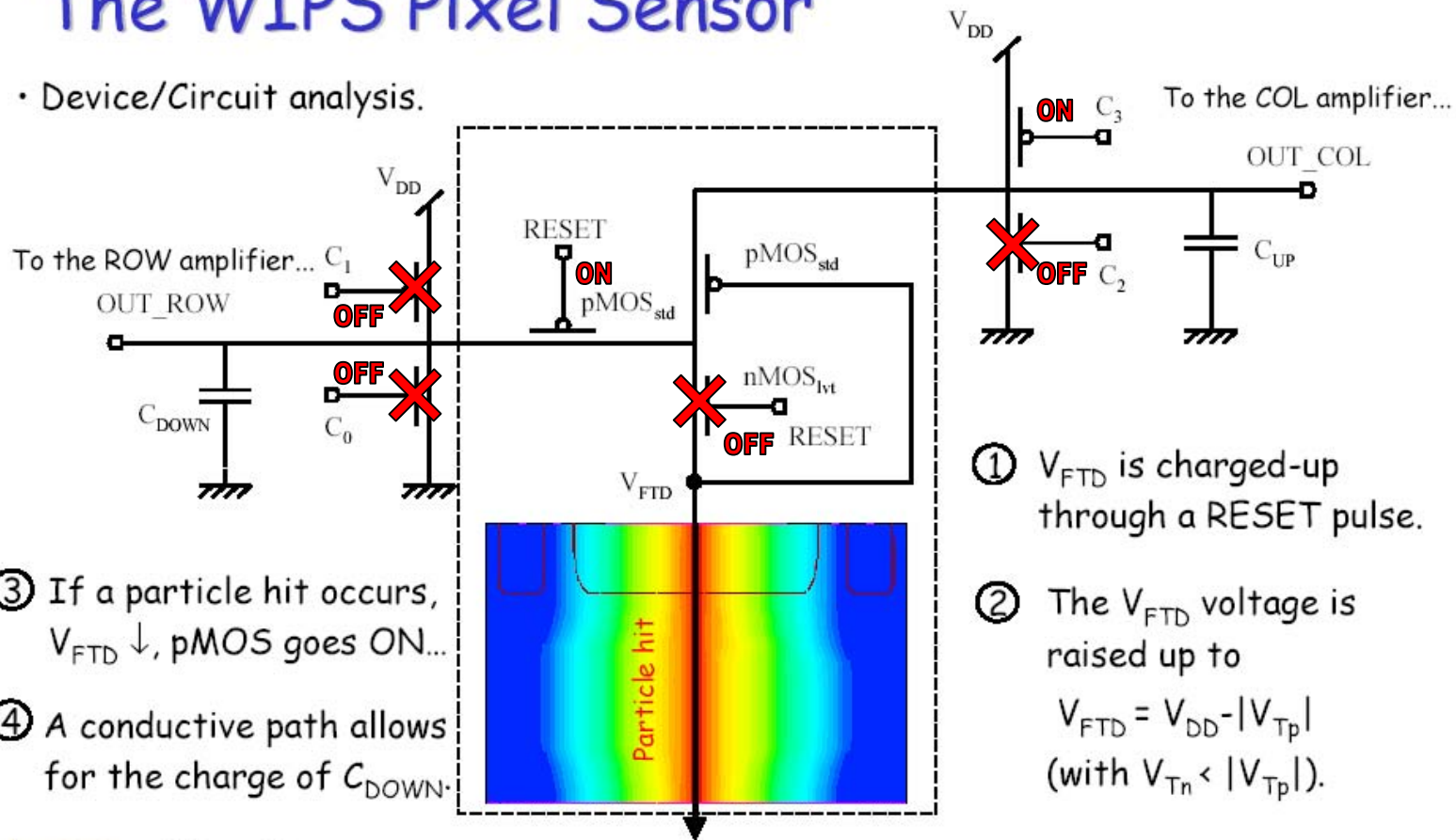
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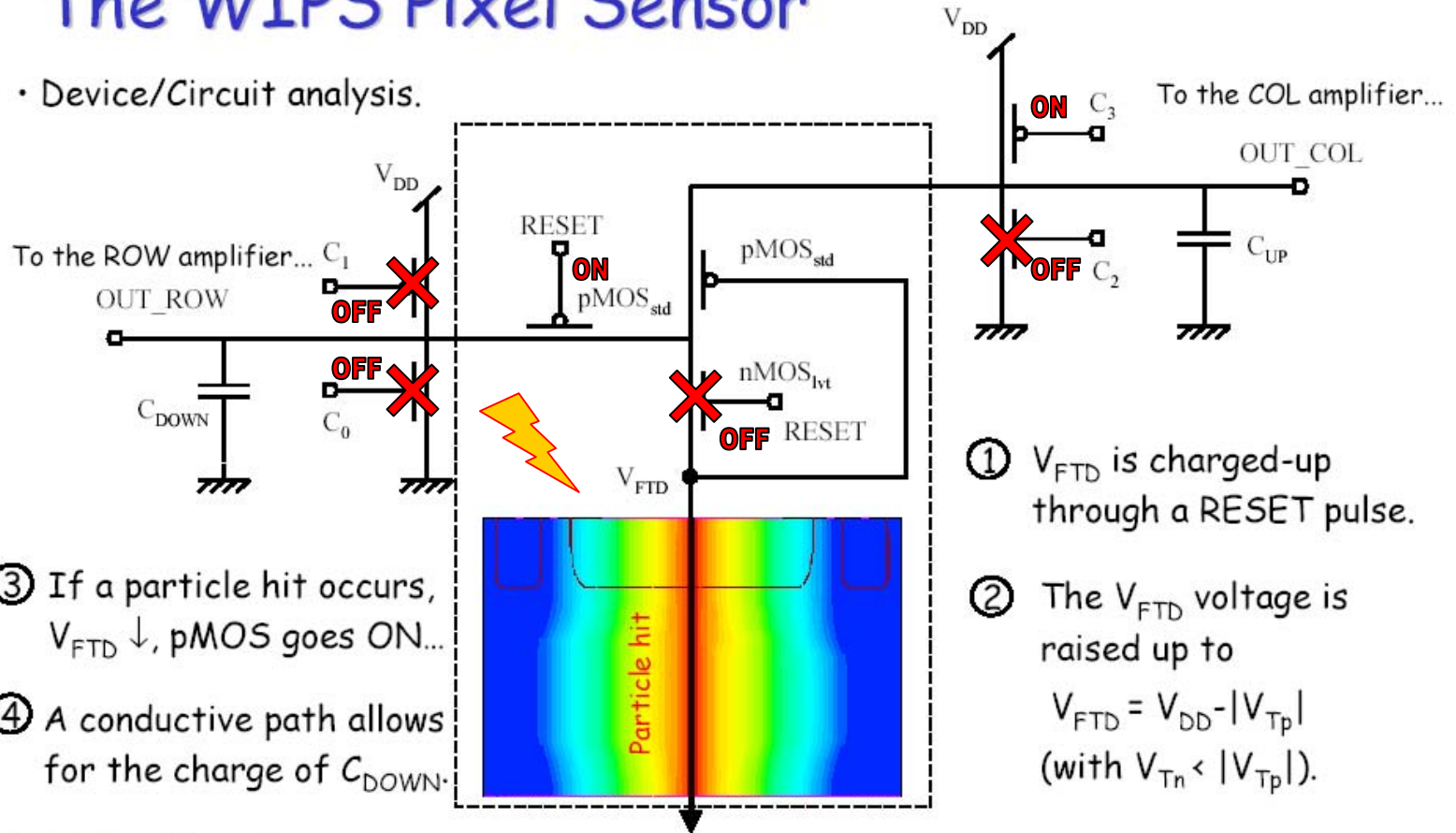
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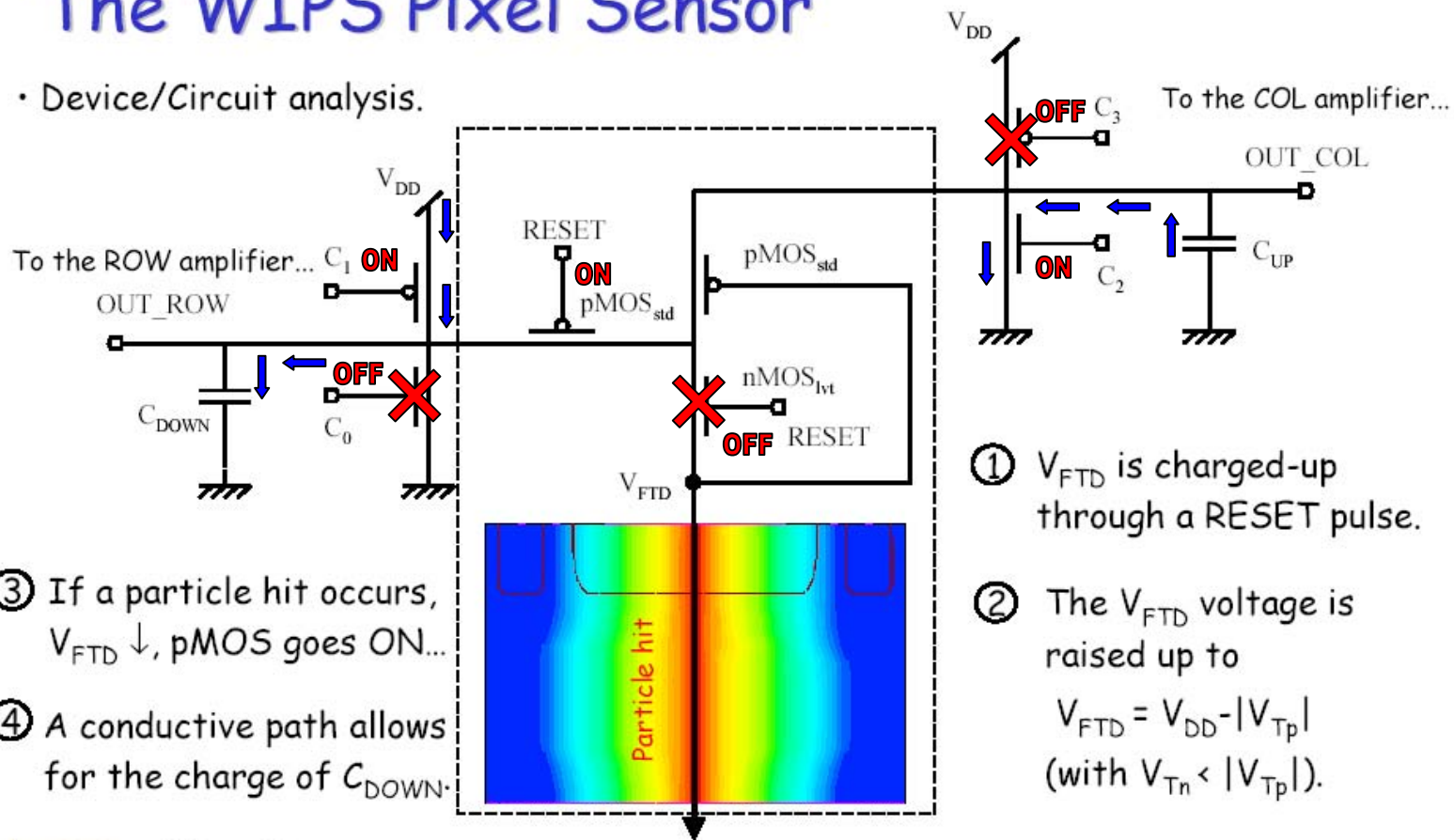
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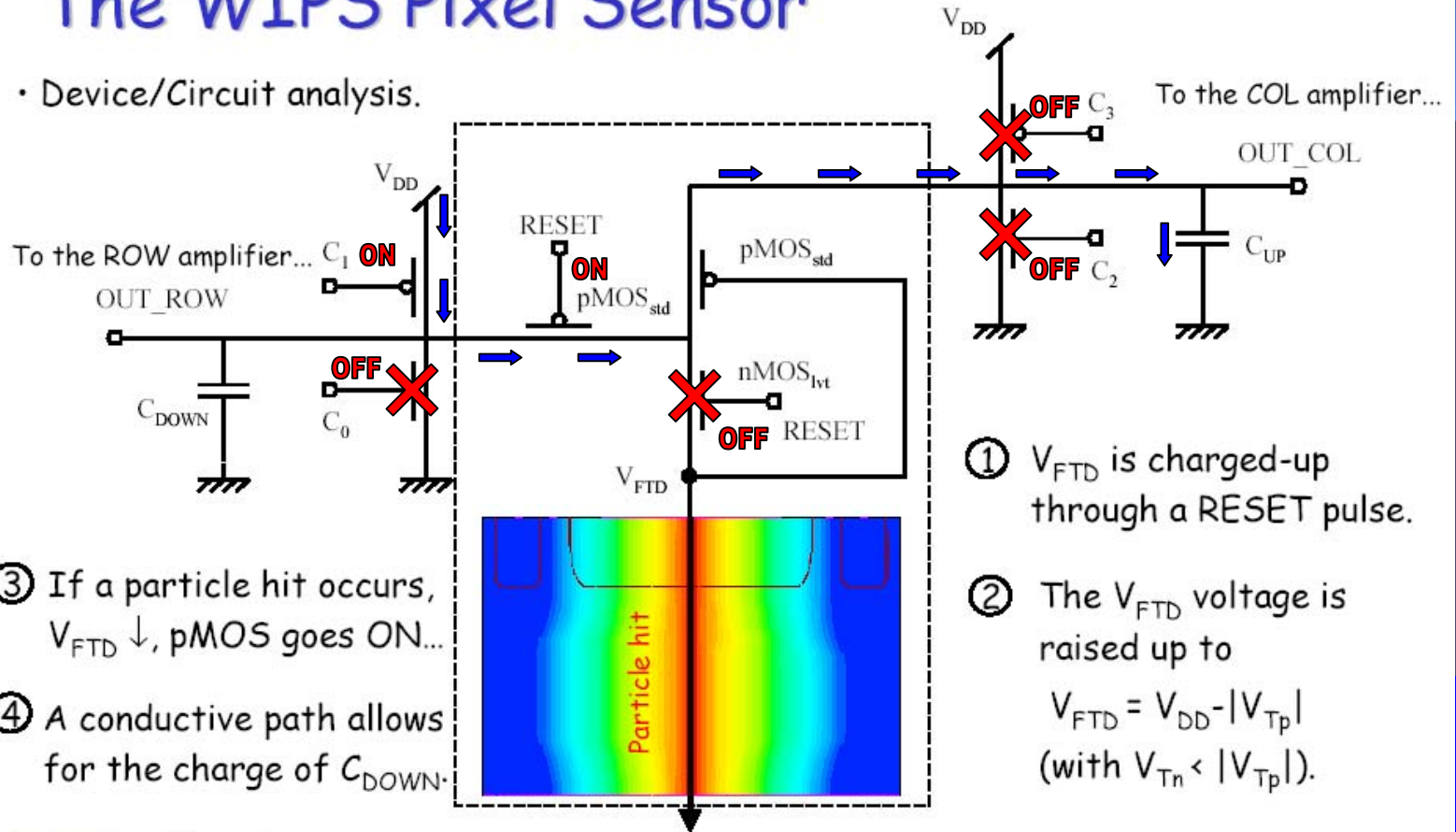
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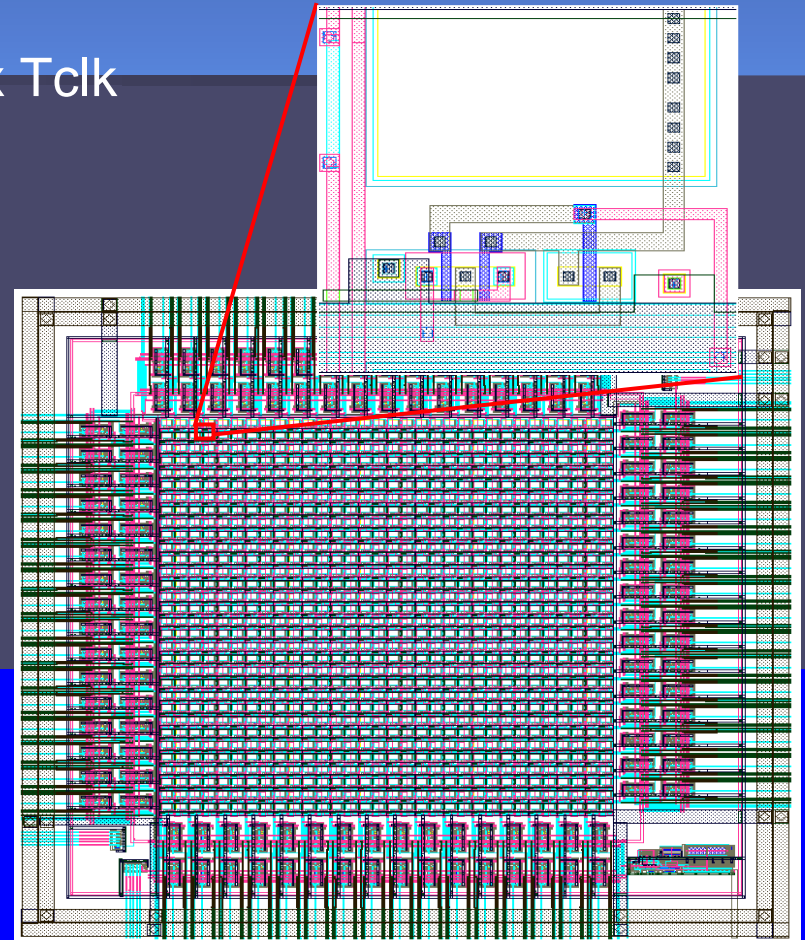
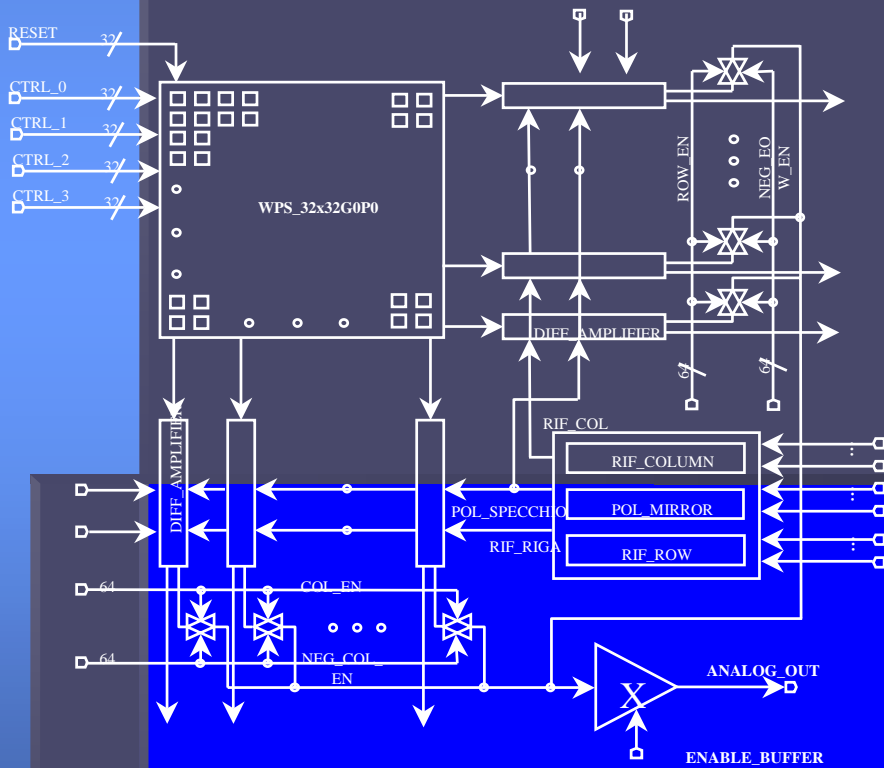
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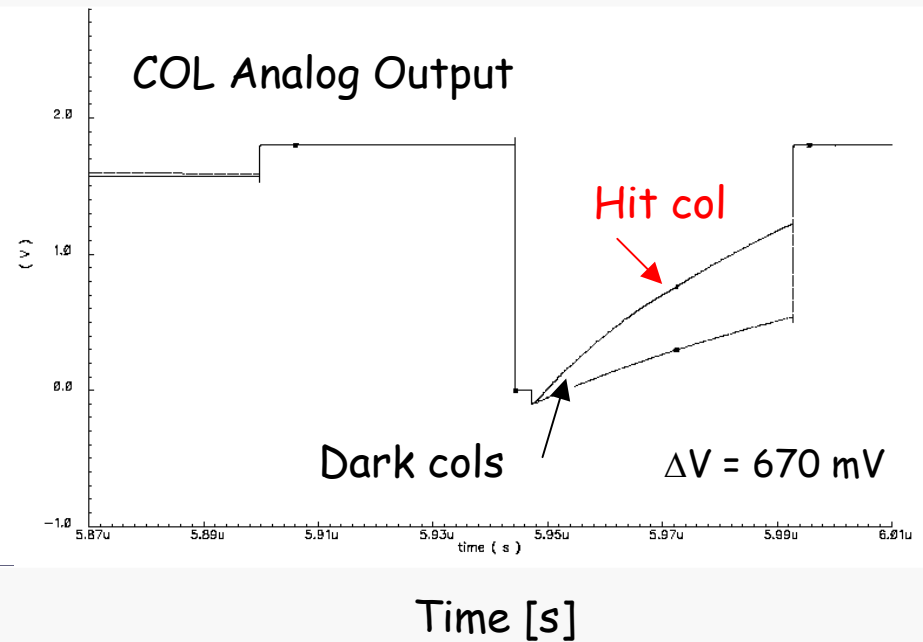
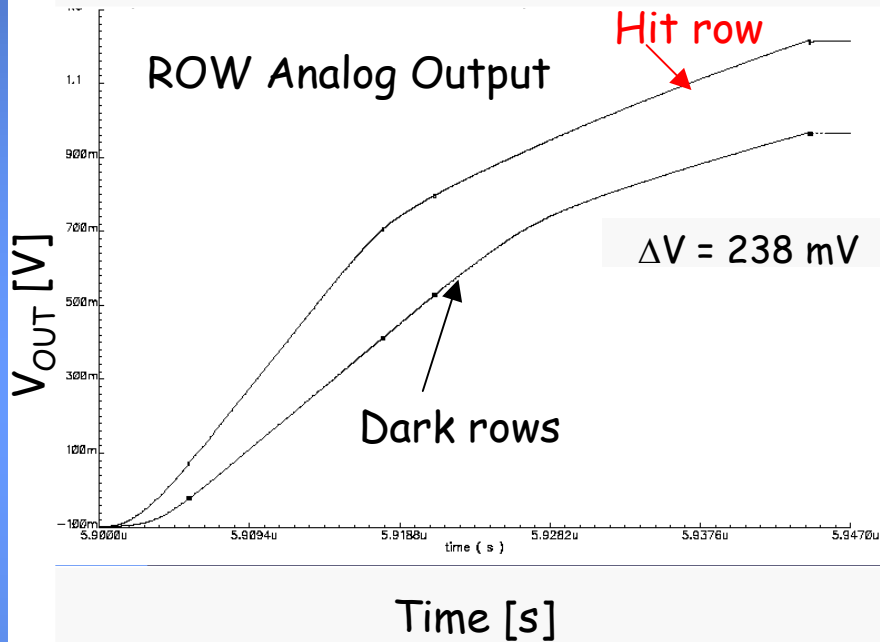
WIPS architecture

Sparse read-out scheme

Single row scan / serial out $(n + n) \times T_{clk}$



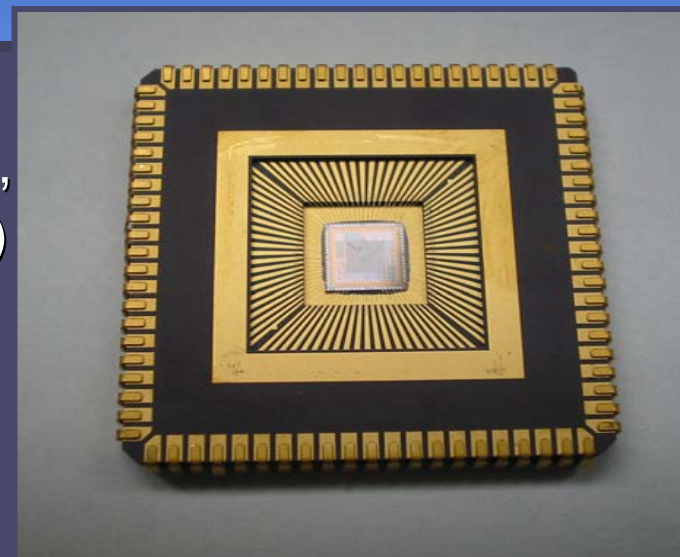
WIPS Performance



- Large voltage swing
- Leakage current control

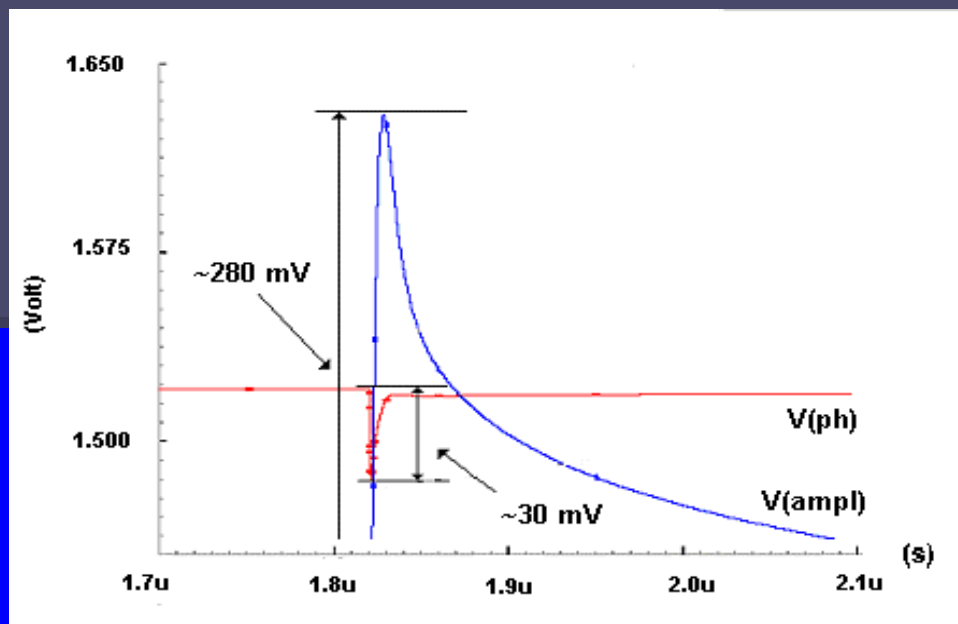
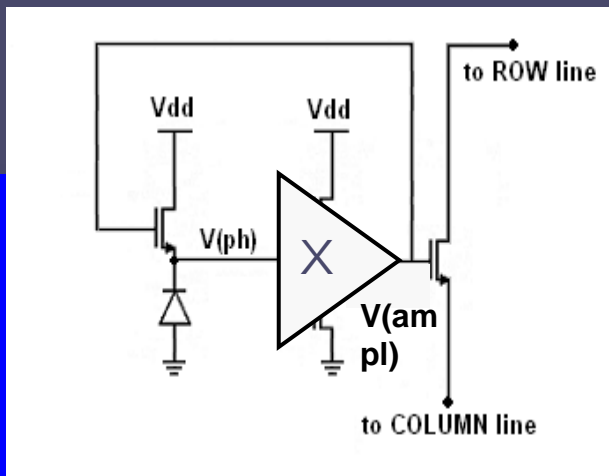
Chip fabrication

- Several prototypal matrices:
 - different substrate options (twin-tub, p-well blocking layer, bias scheme)
 - different array sizes
 - different device sizes and pitches.
- Random pixel access:
 - row, column decoders.
 - digitally-programmable bias of read-out amplifiers.
- Analog/Digital layout.
- Different bonding schemes.
- Layout suitable for laser testability.



Architecture Evolution

- “On-pixel” voltage amplification.
- Exploitation of effective addressing of pixel array.
- Power dissipation critical -> dark current reduction...



Conclusions

- The suitability of standard CMOS technology for particle detection has been investigated.
- Different pixel layout and read-out schemes have been devised and implemented.
- RAPS01 chip fabrication has been completed
- Test results are expected in the near future.
- Work is being carried out toward RAPS02 chip design, aiming at S/N ratio improvement and efficient (sparse) read mode of pixel array.