



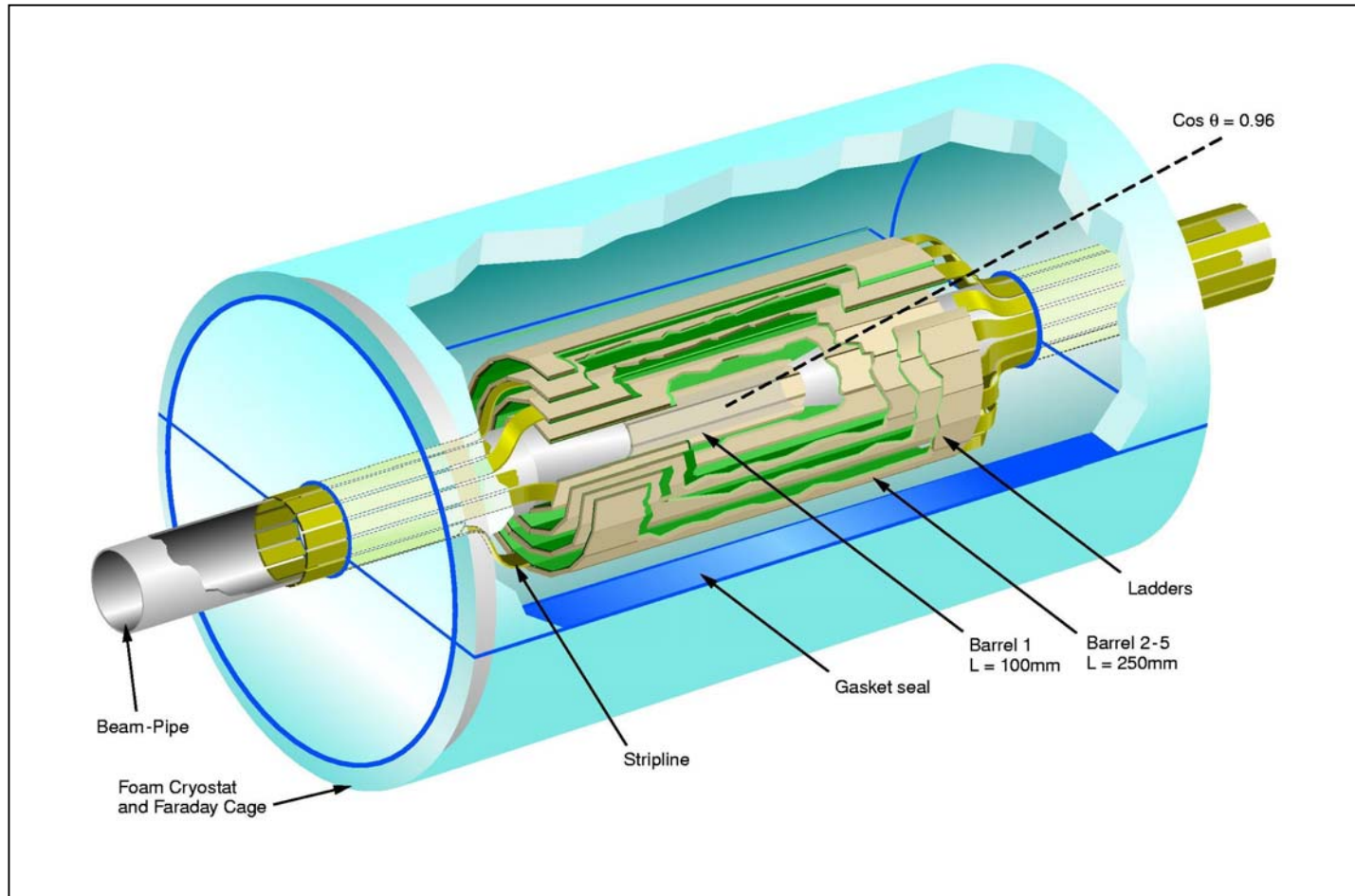
CCLR C
Rutherford Appleton Laboratory

Read-out electronics for a Linear Collider CCD Vertex Detector

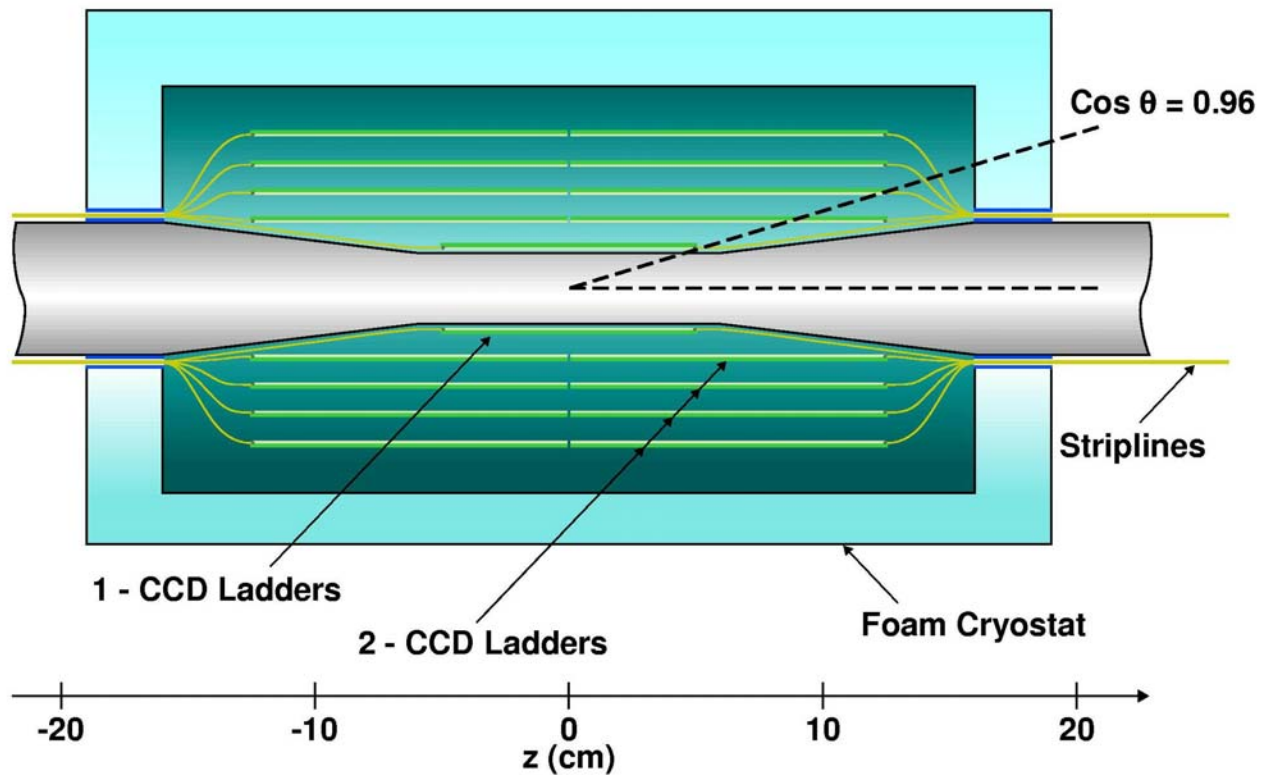
Outline of talk

- Vertex detector
- Column parallel read-out (CPR) layout
- Flash converter and encoder
- Charge-transfer amplifier
- Prototype test results (CPR0)
- CCD test results (CPC1)
- CPR1 testing
- CPR2 design
- Conclusions and future plans

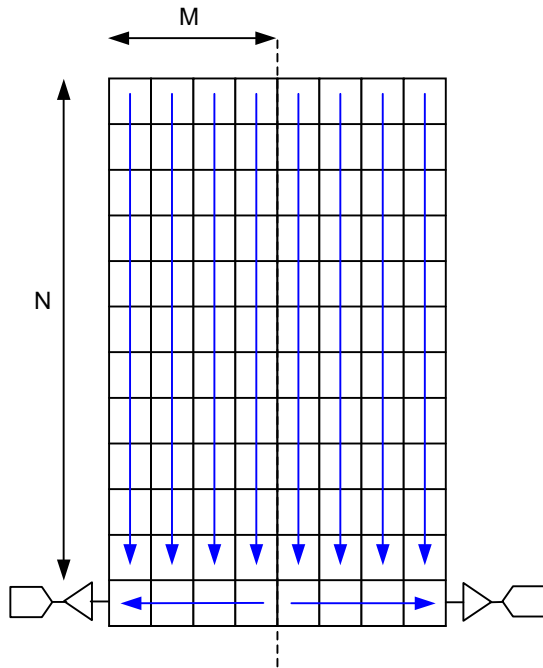
CCD Vertex Detector



CCD Vertex Detector

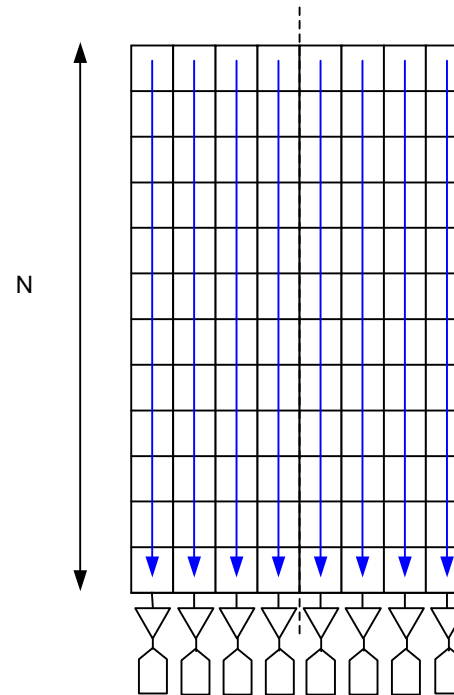


Column Parallel CCD structure



Conventional CCD:
outputs at corners

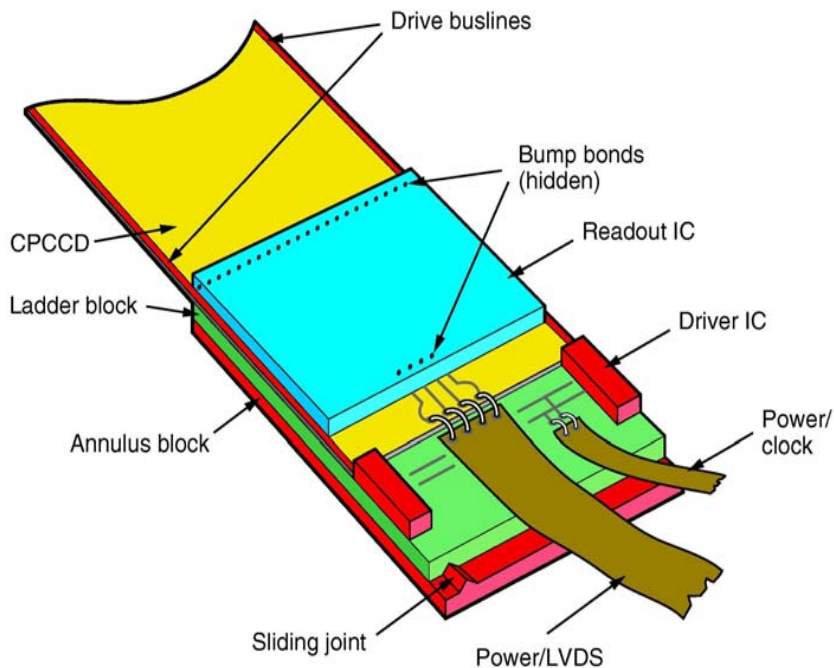
Readout time = $N \times M / \text{Clock Freq}$



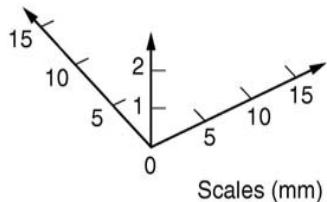
Column Parallel CCD:
outputs along one side

Readout time = $N / \text{Clock Freq}$

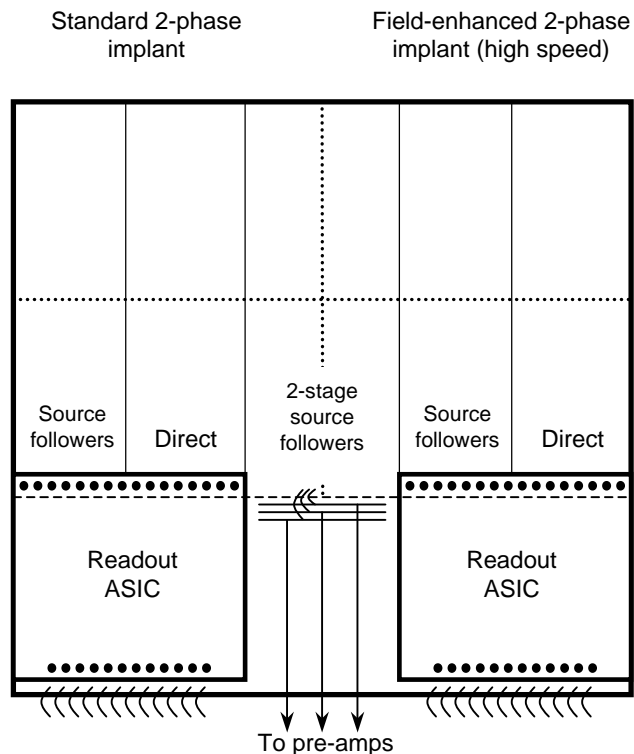
Column Parallel Read-out (CPR) IC



- **Electronics only at the ends of the ladders;**
- **Bump-bonded assembly between thinned CPCCD and readout chip;**
- **Readout chip does all the data processing:**
 - ◆ Amplifier and ADC for each CCD column
 - ◆ Hit cluster finding
 - ◆ Data sparsification
 - ◆ Memory and I/O interface
- **CPCCD is driven with high frequency, low voltage clocks (~50MHz, ~2V);**
- **Low inductance layout for clock delivery.**



CPC1 with CPR1

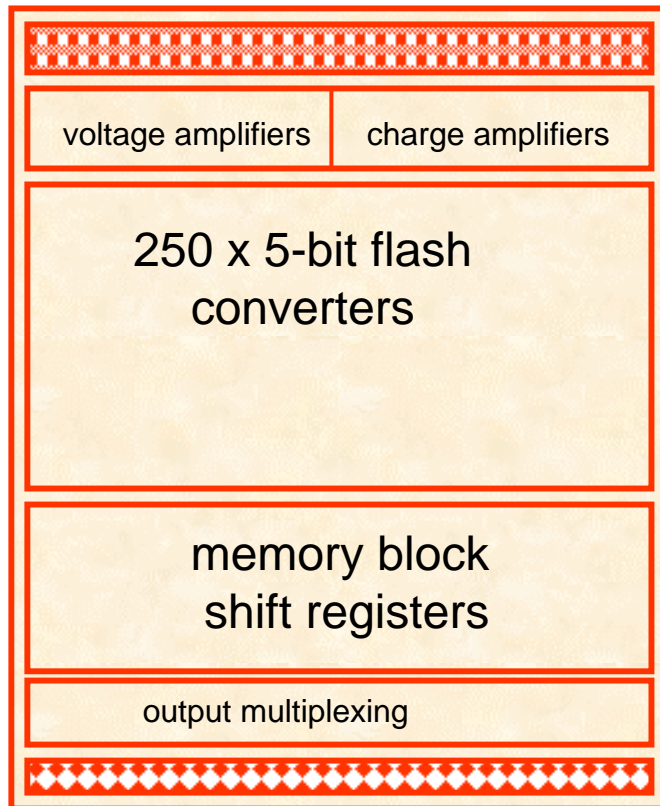


Features in the first CPCCD (CPC1):

- ◆ 2 different charge transfer regions;
- ◆ 3 types of output circuitry;
- ◆ Independent CPCCD and readout chip testing possible:
 - Without bump bonding - use wire bonds to readout chip
 - Without readout chip - use external wire bonded electronics
- ◆ Different readout concepts can be tested.

CPR1 layout

input bump-bond pads



power/control/output bump-bond pads

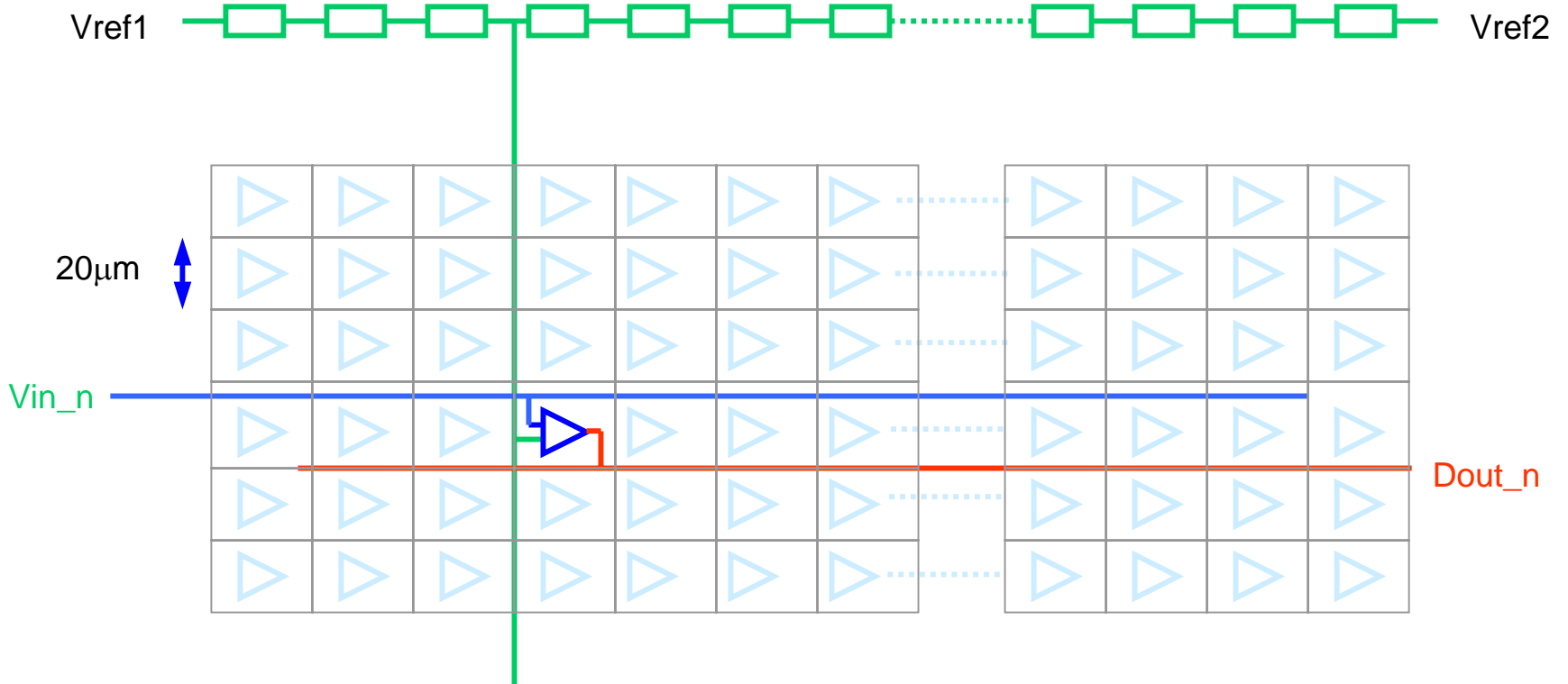
In CPR-1:

- Voltage amplifiers – for source follower outputs from the CPCCD
- Charge amplifiers – for the direct connections to the CPCCD output nodes
- Amplifier gain in both cases: 100 mV for 2000 e⁻ signal
- Noise below 100 e⁻ RMS (simulated)

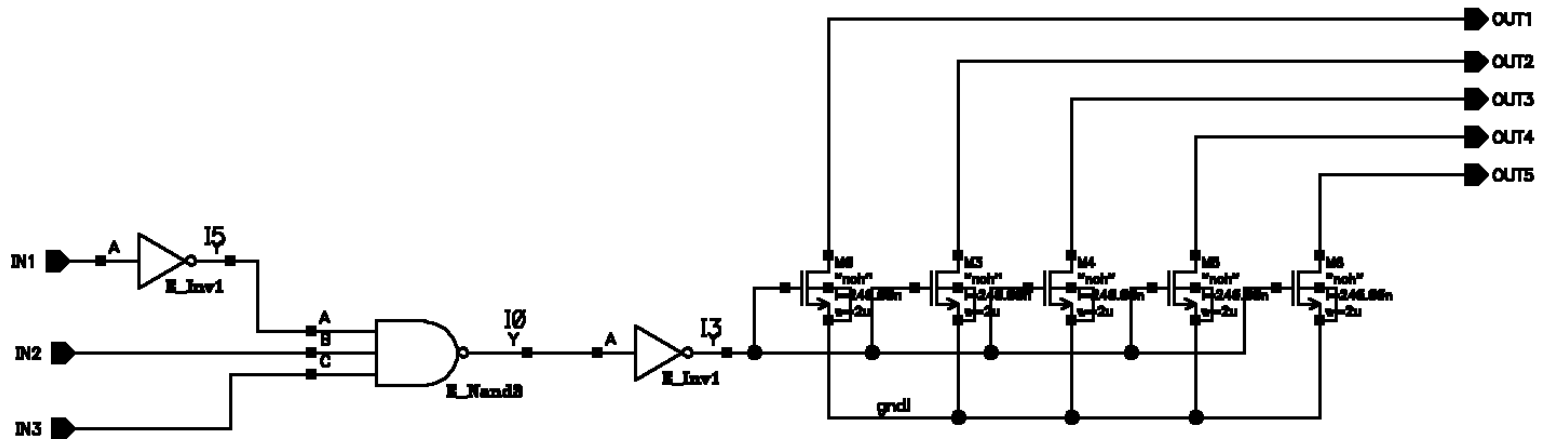
Direct connection and charge amplifier have many advantages:

- Eliminate source followers in the CCD;
- Reduce total power to ≈ 1 mW/channel, no active components in the CCD;
- Programmable decay time constant (baseline restoration).

Flash converter layout



5-bit encoder



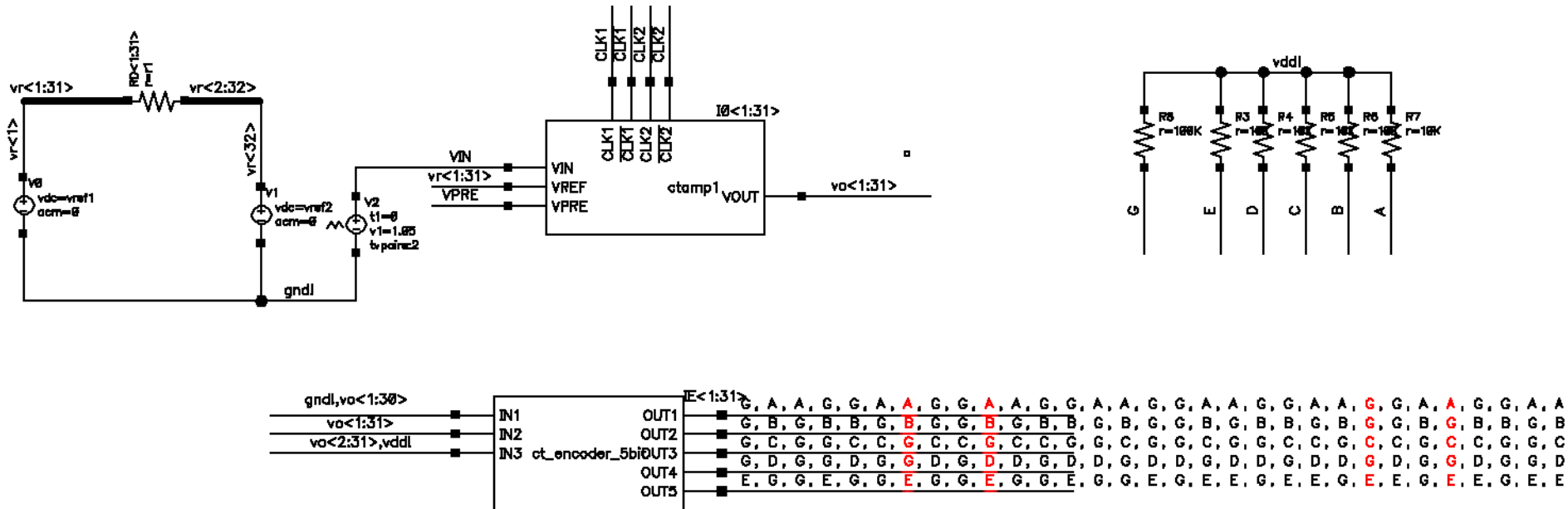
Flash converter encoding

111100000000 → 4
111110000000 → 5
111111000000 → 6
111111010000 → 6
111111011000 → 6, 9

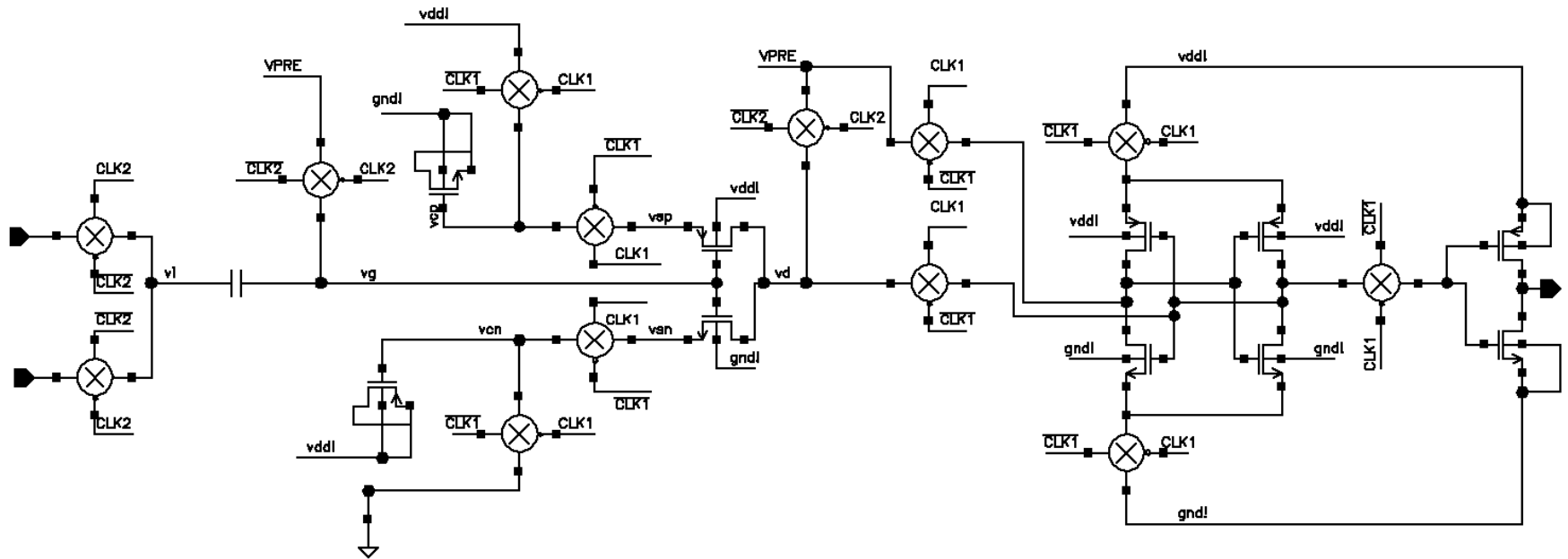
Correction uses modified Gray code

00110 AND 01001 (binary) → 00000 (large error)
01010 AND 01011 (Gray) → 01010 (no error)

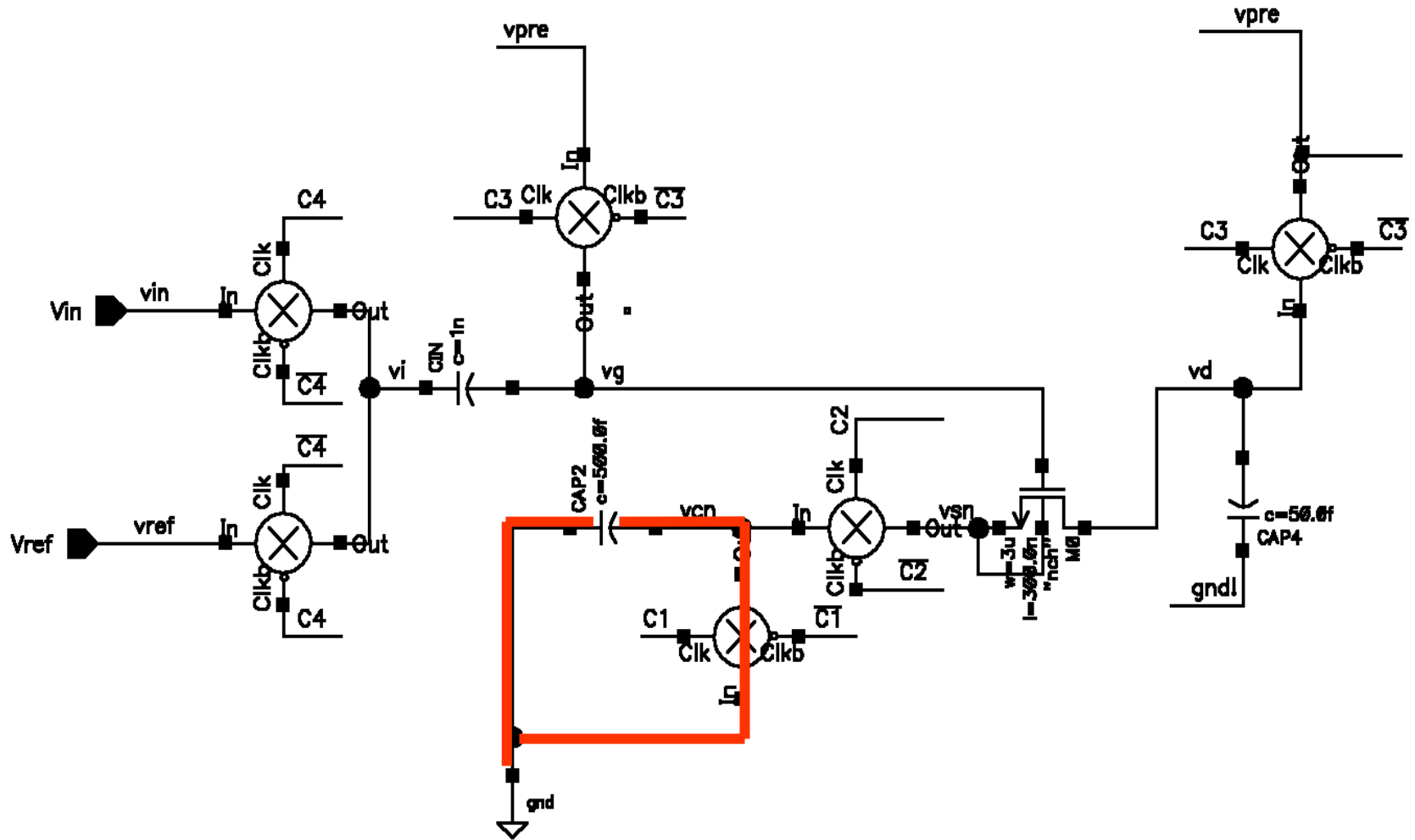
5-bit encoder (31 cells)



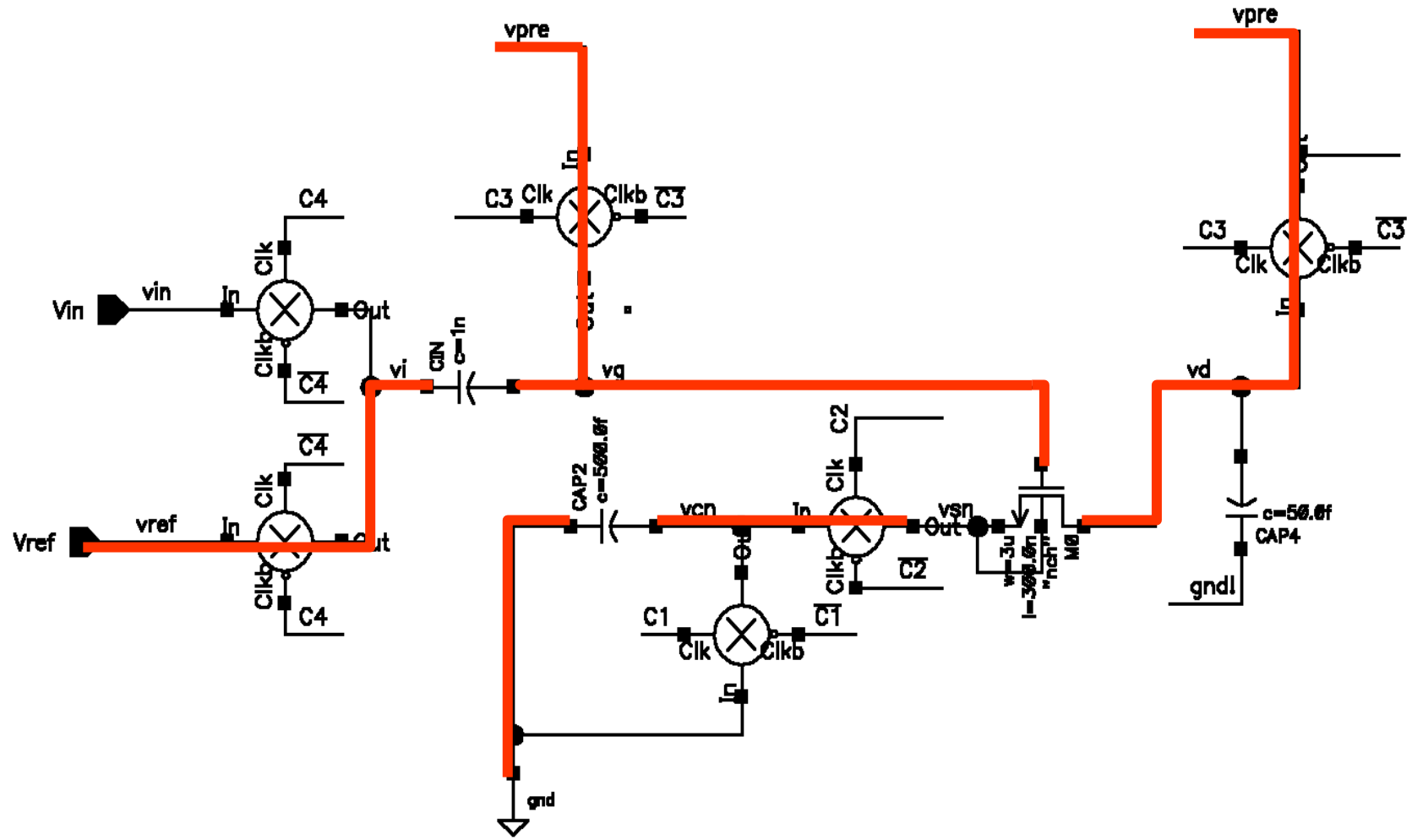
Charge-Transfer Amplifier (CTA) with Comparator



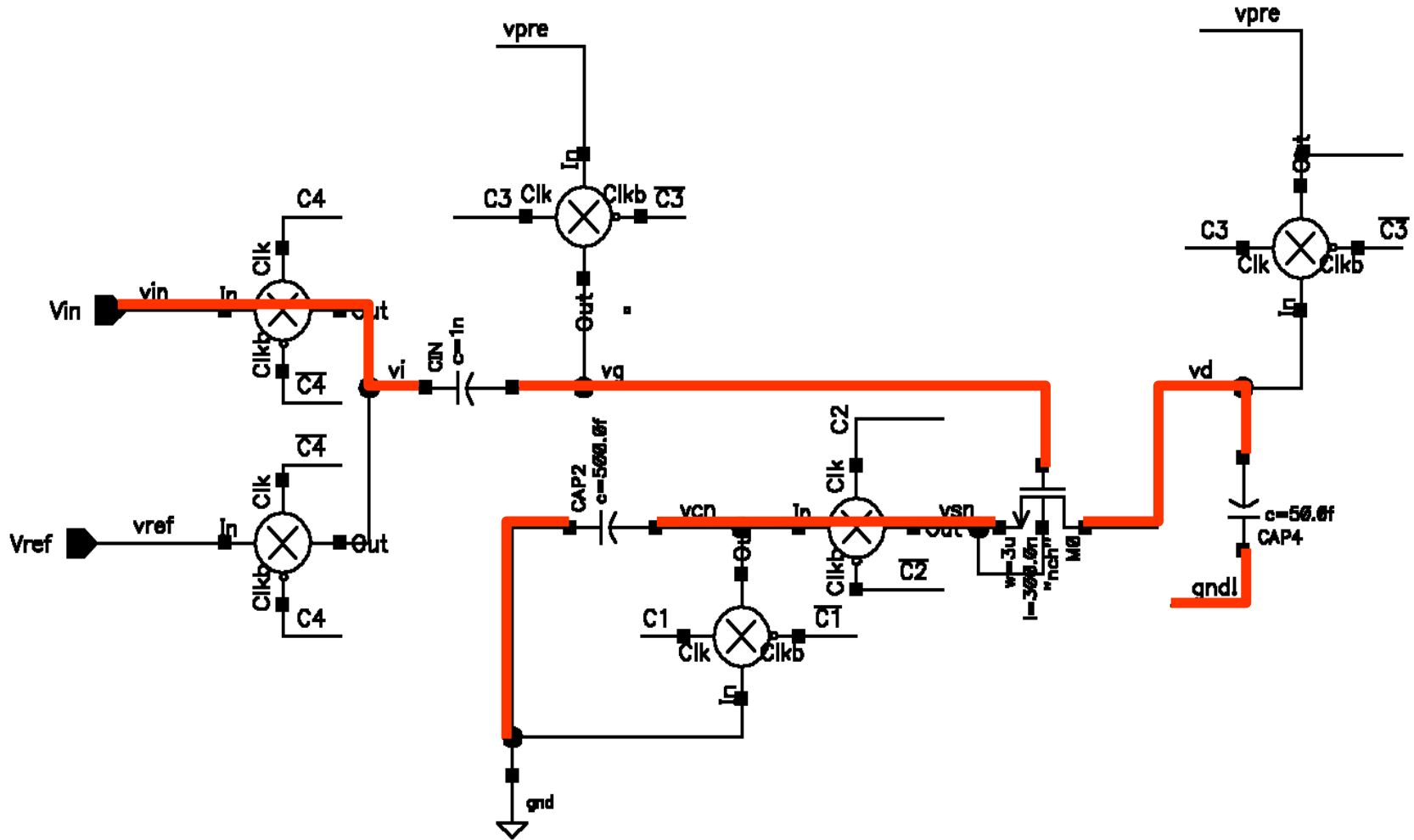
CTA : reset



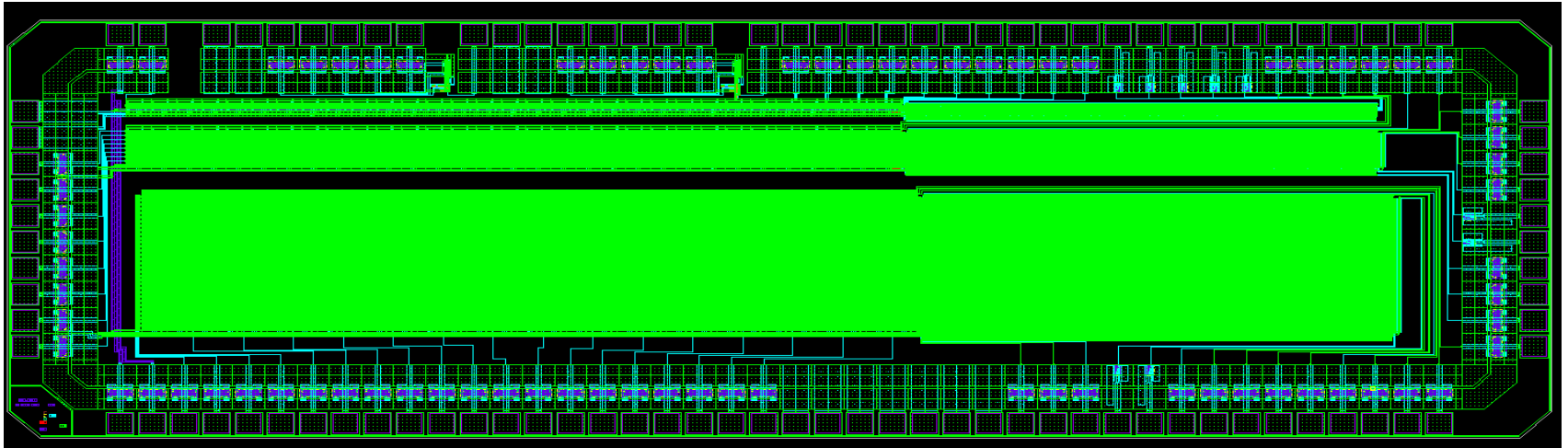
CTA : Pre-charge



CTA: Amplify



CPR prototype (CPR0)

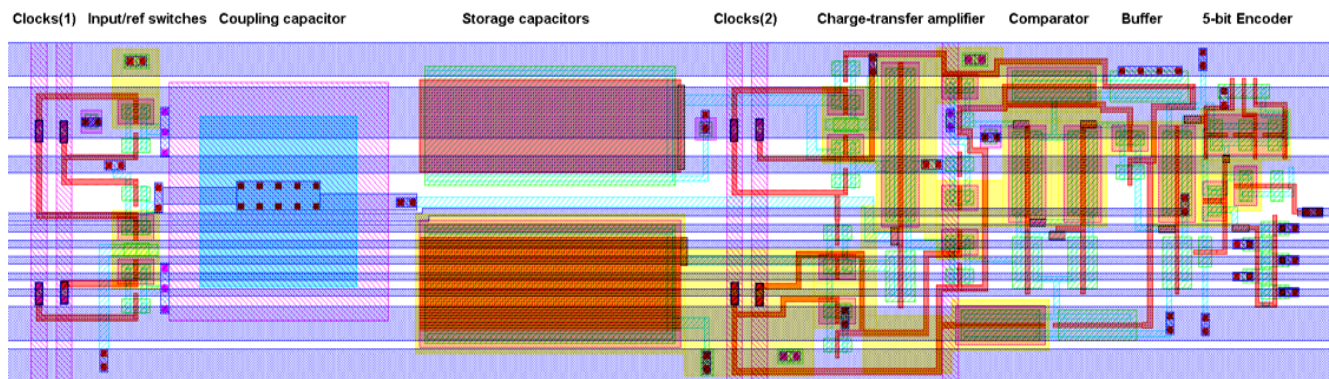


5-bit Flash ADC/memory array with

- 20 μm pitch
- $\sim 100\text{mV}$ dynamic range
- $\sim 20\text{ns}$ conversion time
- Three formats (1-channel, 8-channel, 32-channel)

Amplifier test structure ($< 10\text{ns}$ rise time, voltage gain > 30)

CPR0 channel layout

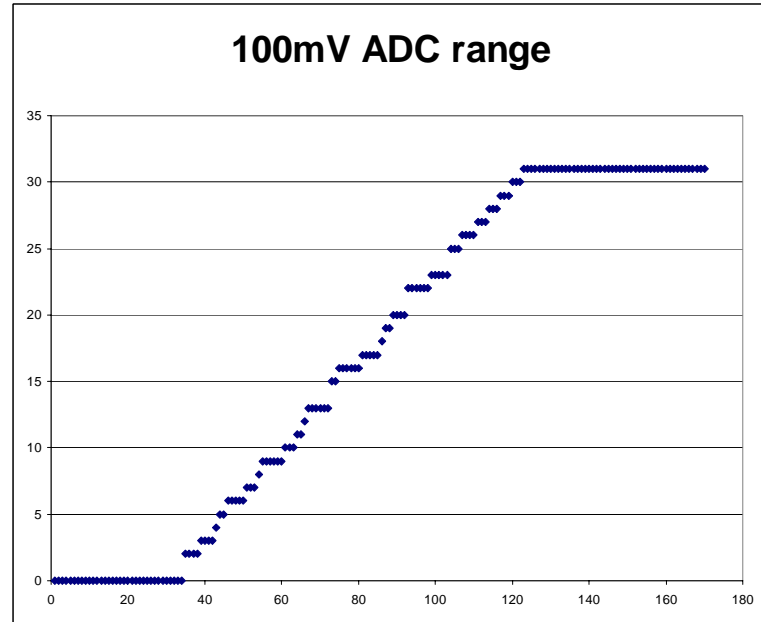
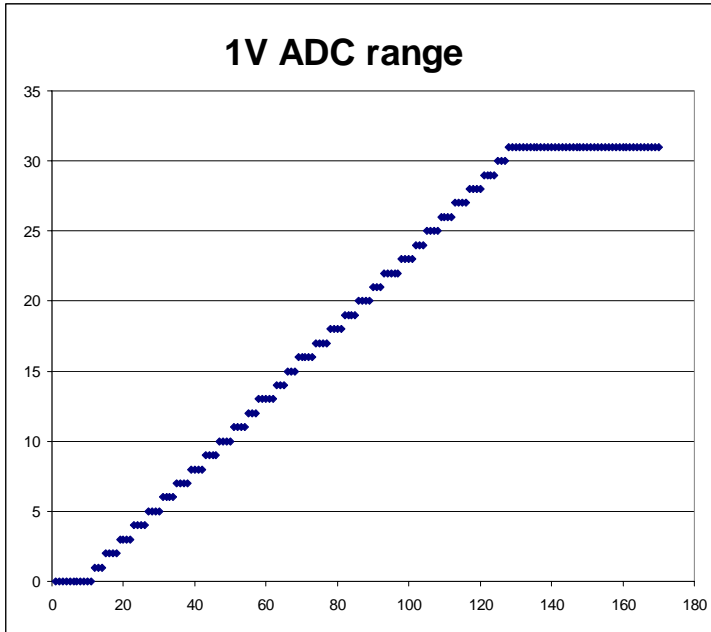


A comparator using Charge Transfer Amplifier, repeated 31 times per ADC

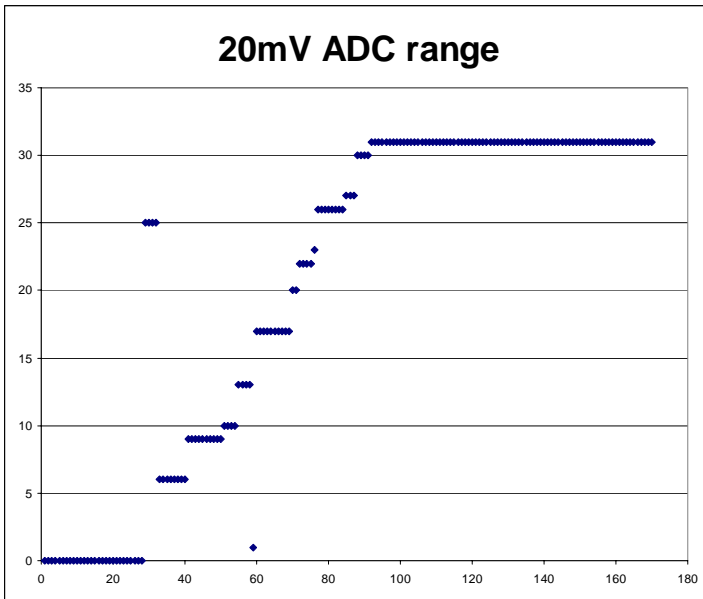
20 μm by 100 μm block:

- Stepped and repeated 31 times (end-to-end) to create 5-bit ADC channel
- Repeated up to 32 times (side-to-side) to create ADC array

CPR0 ADC performance

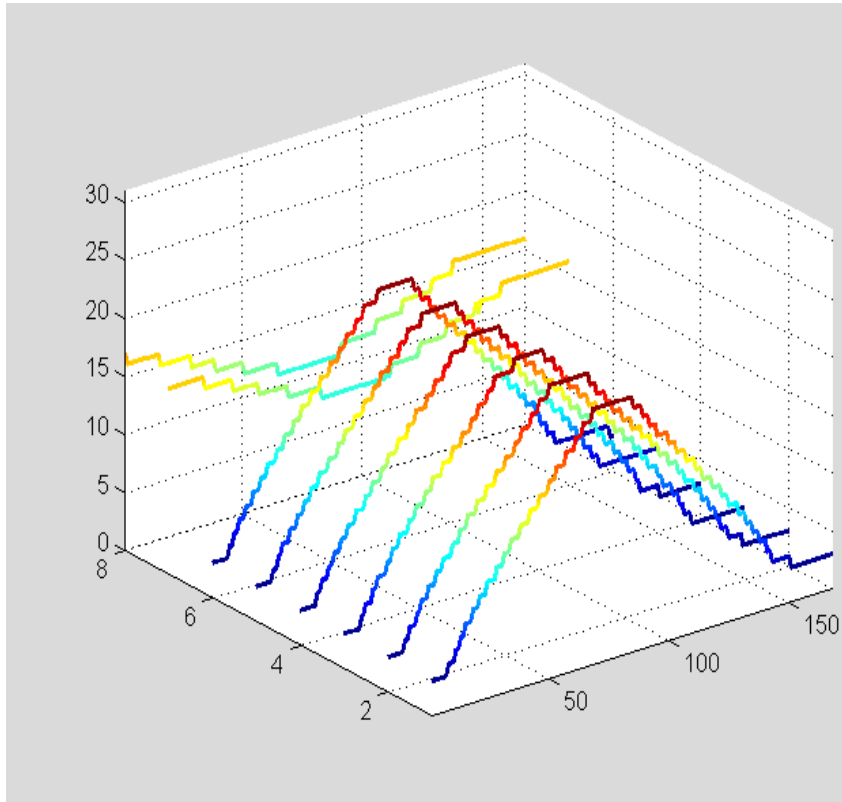


ADC performance limit

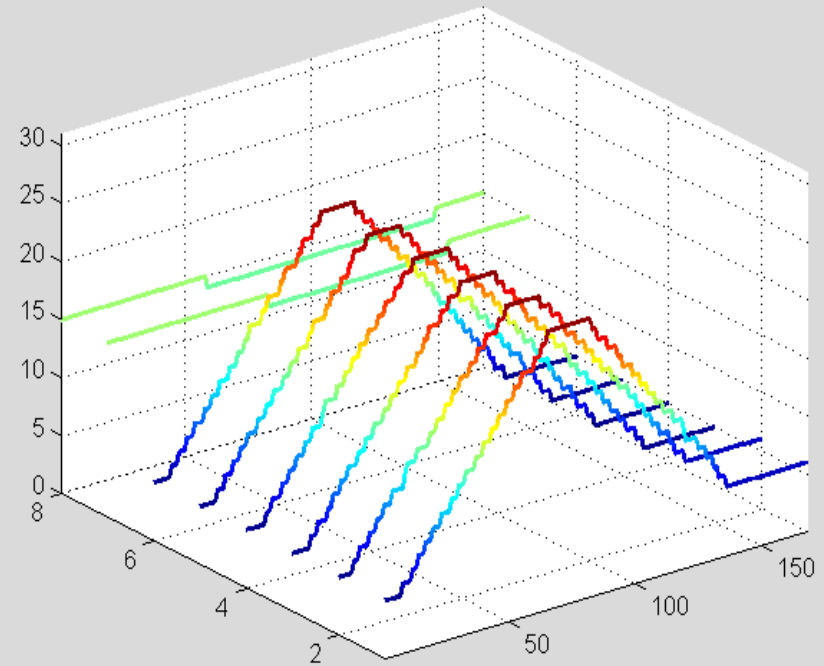


Non-monotonic
below ~20mV

Cross-talk effect

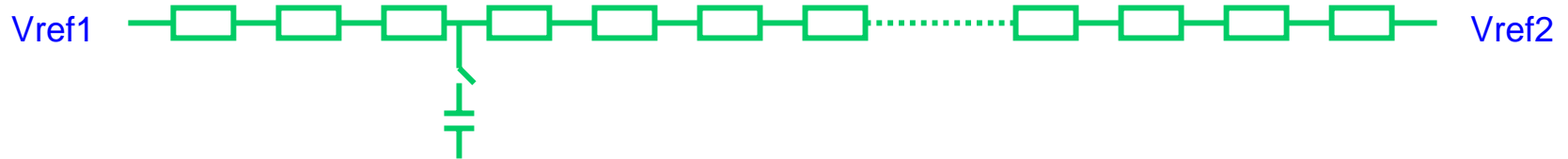


5MHz conversion, ~20% coupling



1MHz conversion, ~5% coupling

Cross-talk elimination



Pulsed channels present dynamic load to resistor ladder, which causes the intermediate resistor voltages to fluctuate.

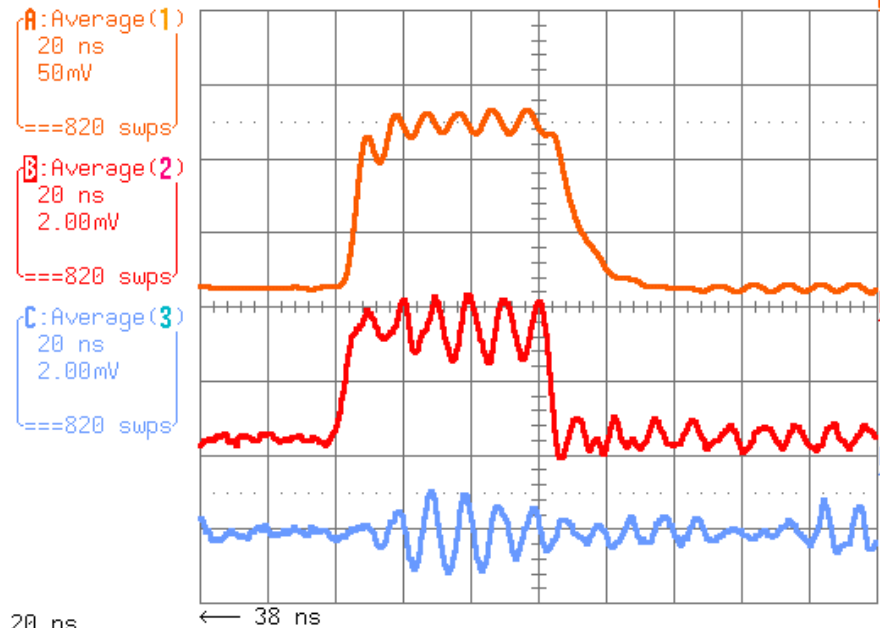
This changes the effective reference for non-pulsed channels, causing coupling from pulsed to non-pulsed channels.

Solution:

Lower value resistors to reduce fluctuation magnitude and time-constants

CPR0 Test amplifier

17-Oct-02
10:17:34



Vout ~120mV

Vin ~3mV

GND (2mV noise)

1	5 mV	DC	⊗
2	2 mV	DC	⊗
3	2 mV	AC	⊗
4	1 V	AC	⊗

Ext10 AC 0.00 V 1MΩ

Summary of CPR0 results

Flash converter:

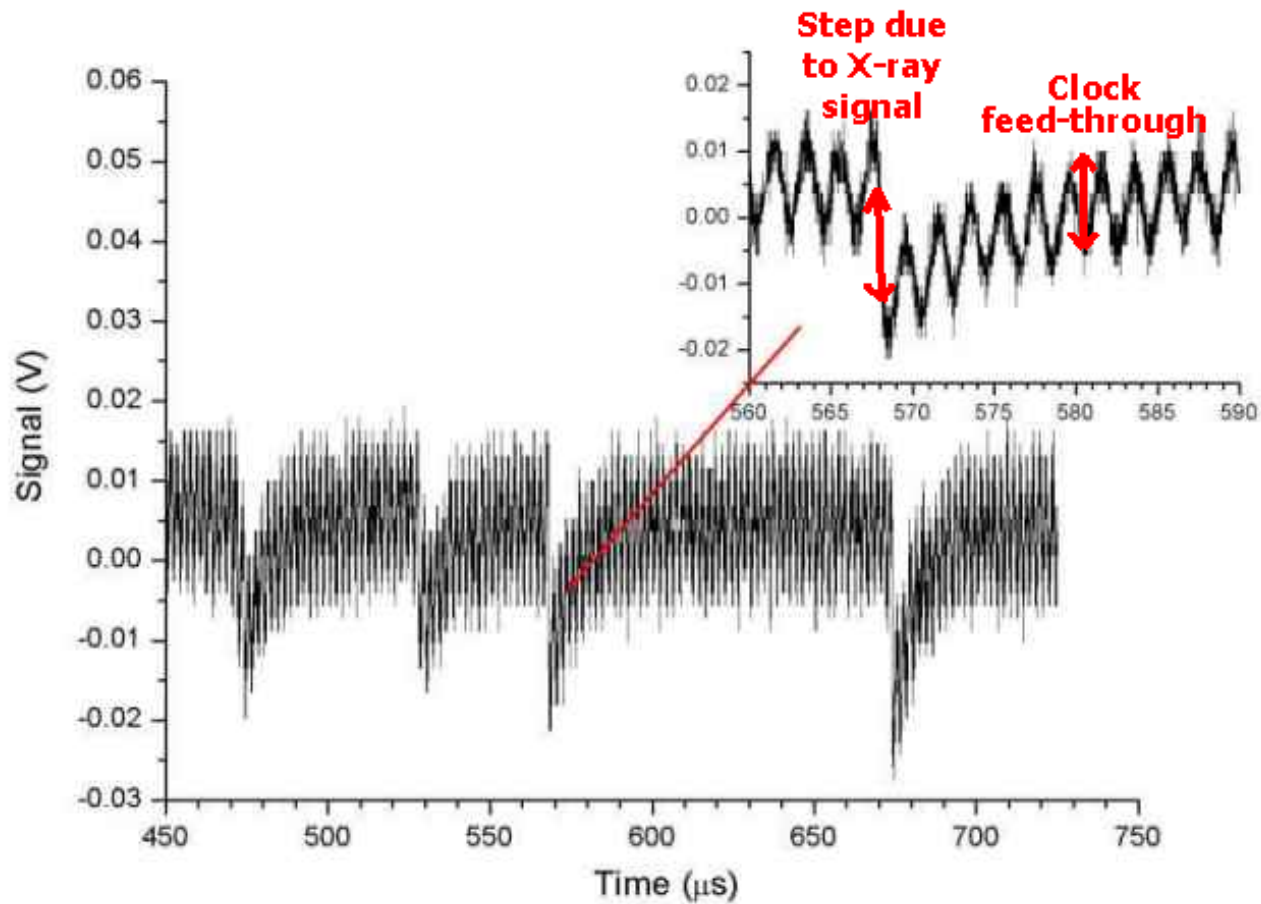
- Some functionality at 50MHz
- Works well at 25MHz, voltage range 1V and below
- Onset of missing codes at $\sim 100\text{mV}$
- Monotonic down to $\sim 20\text{mV}$ (~ 4 -bits effective resolution)
- Cross-talk effect understood

Amplifier

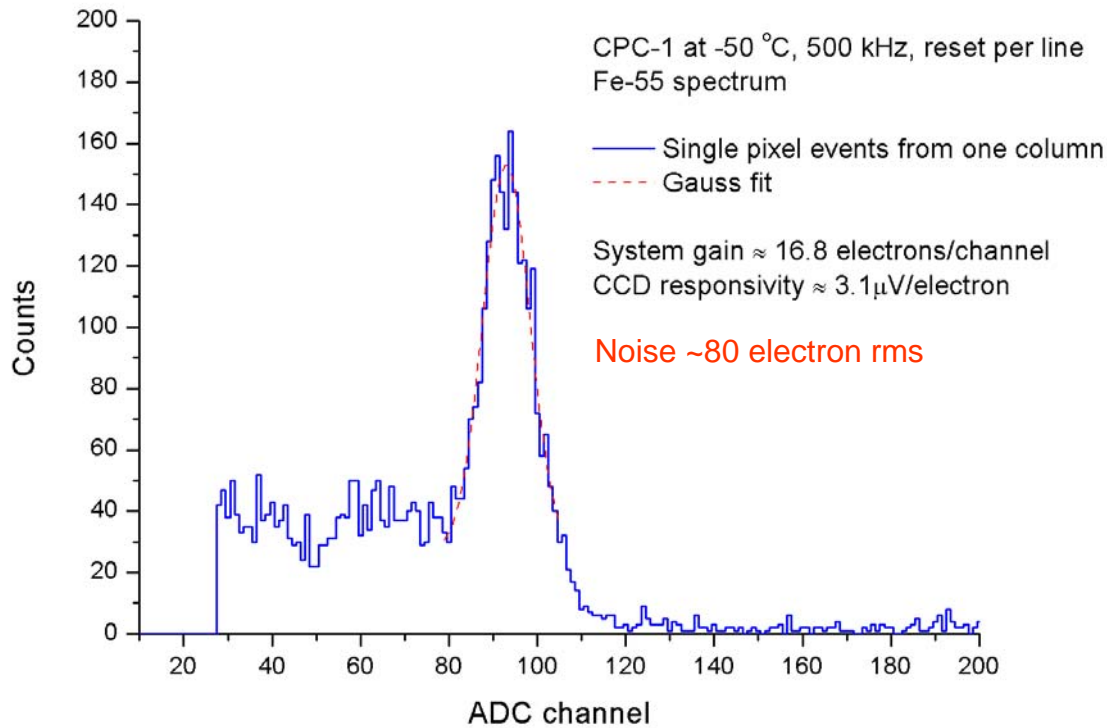
- Rise time $\sim 5\text{ns}$
- Gain ~ 40
- Overshoot due to ground loops and measurement parasitics.

Column parallel CCD (CPC1) test result

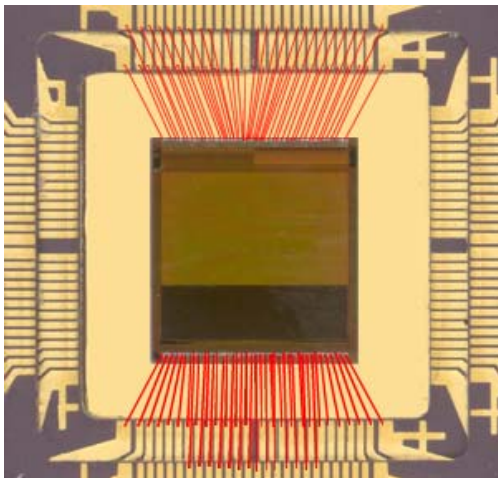
(wire-bonded outputs to conventional amplifiers)



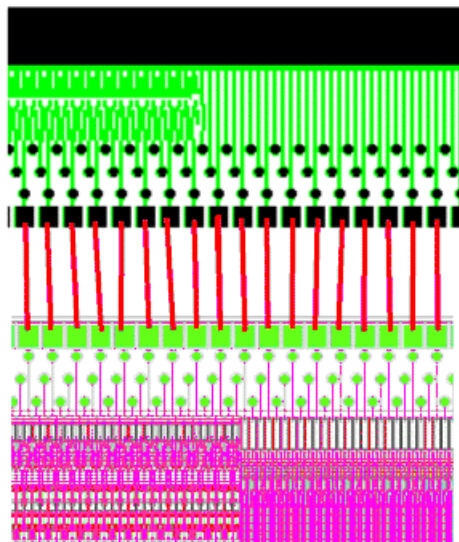
CPC1 Iron-55 spectrum



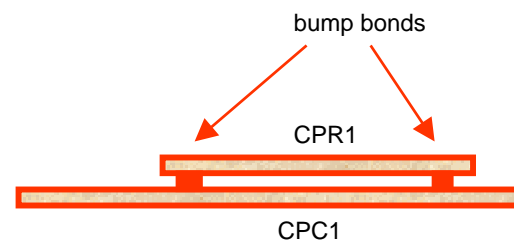
CPR1 testing



Step 1:
CPR1 in PGA (no CCD)
Tests start in 2 weeks



Step 2:
CPR1 wire-bonded
to CPC1 (1 in 3 channels)
Tests start in ~ 2 months



Step 3:
CPR1 bump-bonded
to CPC1
Tests start in ~4 months

CPR2 requirements

Sparse read-out, based on cluster-finding

Example : Low-energy charge-shared event.

Threshold=8, each event is below threshold, but 2-by-2 sum is above threshold

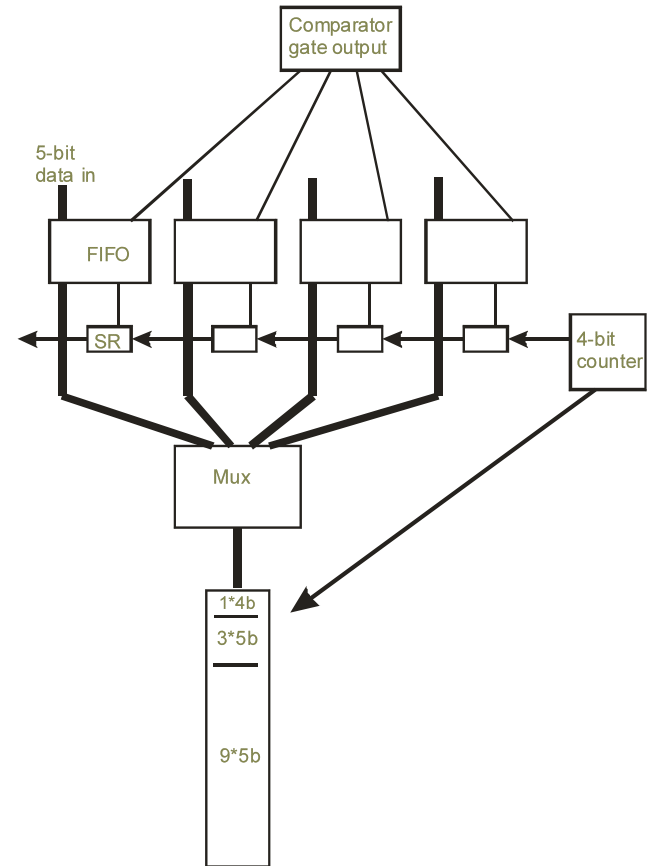
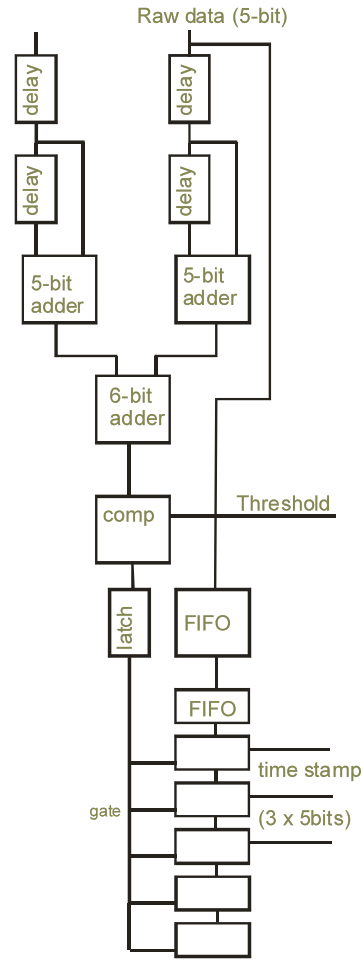
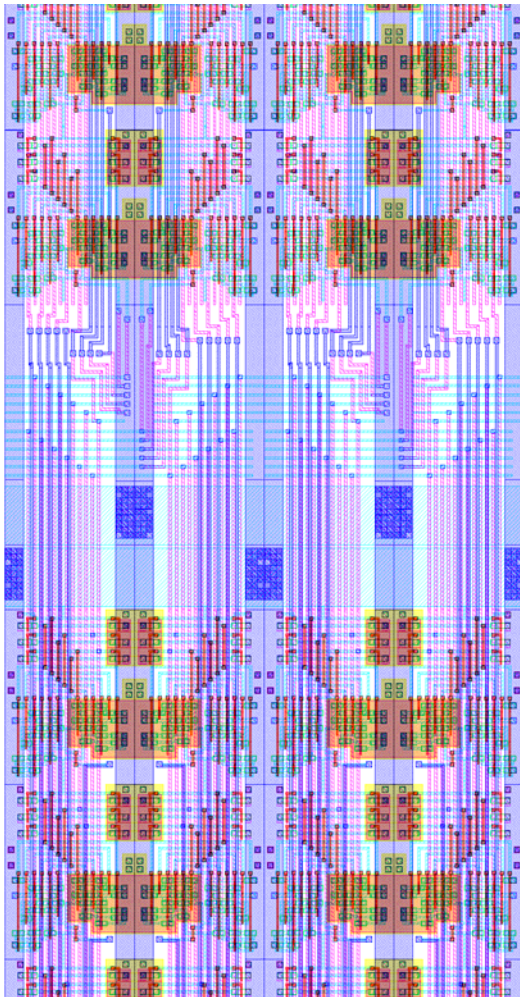
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	5	5	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0

Cluster found

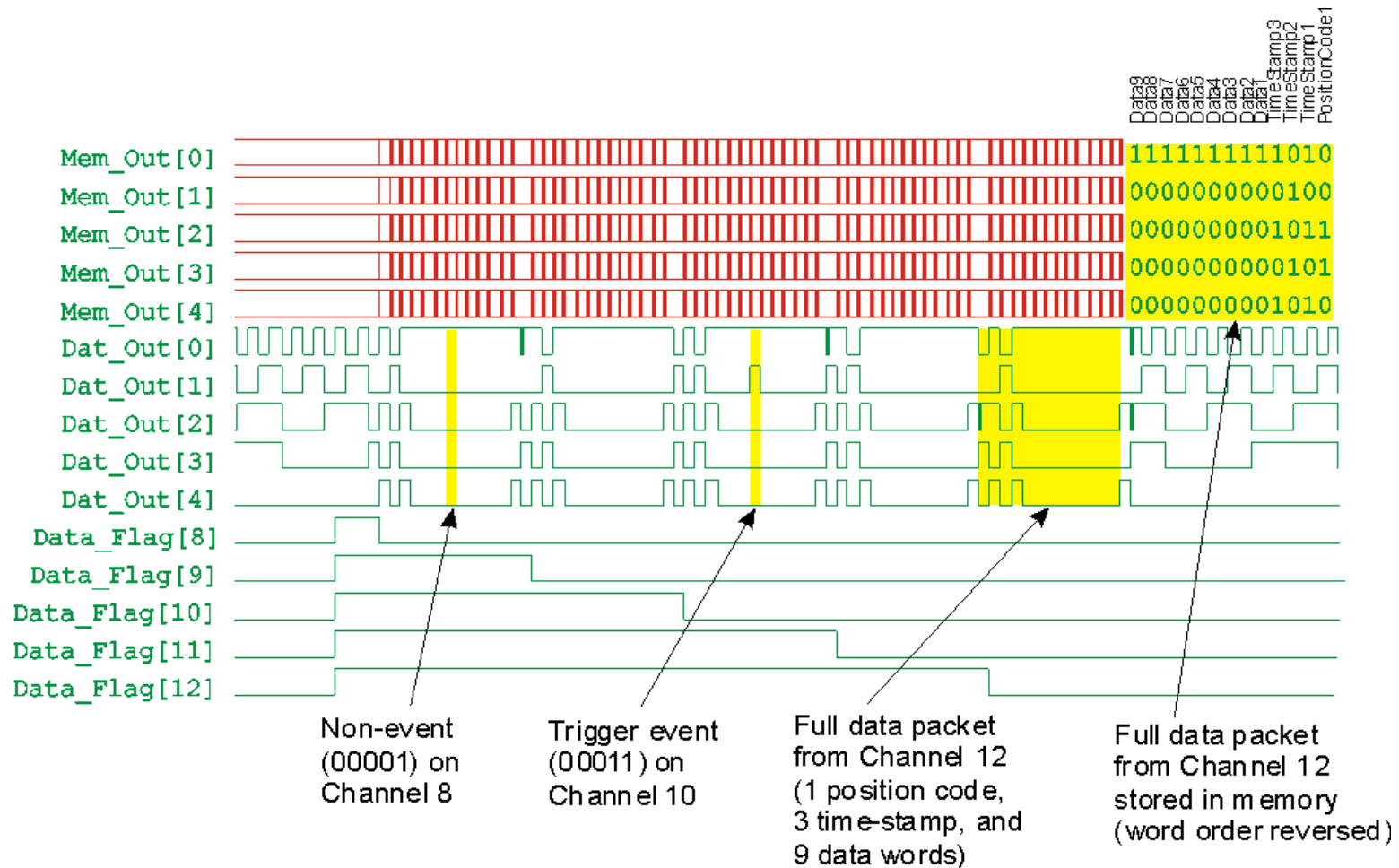
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	5	5	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0

Expanded cluster to be read out

CPR2 layout / architecture



CPR2 simulation



Conclusions

CPR0: 5-bit 20 μ m-pitch ADC array :

functional over wide range of frequency and voltage

CPC1 column parallel CCD

working well with conventional read-out,
low clock feed-through at 2Vp-p, 1MHz.
low noise (~80 electron rms Fe-55)

CPR1 250-channel ADC/memory array

ready for testing

CPR2 250-channel ADC with cluster finding/sparsification

digital design complete
analogue (re)design awaiting CPR1 test results

Future

CPC2/3 large-format CCDs
CPR3 512 or 1024-channel, full ladder read-out
CPR4 production version ?

Acknowledgements

Microelectronics Group

- Peter Murray (analogue and digital design)

LCFI Group

- Chris Damerell
- Konstantin Stefanov (CCD simulation and testing)