Instrumentation for HEP Experiments: Trigger

Academic
Lecture Series

Gordon Watts
University of Washington,
Seattle
Fermilab

Outline

- Introduction
- The Collider Environment
- Trigger Design
  - Hardware Based Triggers
  - Software Based Triggers
  - Farms
- Conclusions

I am bound to miss some features of the triggering systems in various detectors. I have attempted to look at techniques and then point out examples.

Thanks to the many people who helped me with this talk (too numerous to mention).

Where's that Signal?

Academic
Lecture Series

- So, you want to find the Higgs?
  - The usual approach!
  - Build selection cuts around what differentiates the decay from the background.
  - Associated production: $WH \rightarrow l\nu bb$.
  - Look for *W*, b-tag, and then search for *bb* mass peak!
- This is exactly how you would construct an analysis.
- What is the environment?
  - What is really going on here?
  - What decisions does it force us to make?
  - Hardware must be designed to collect these events in the first place.

Academic
Lecture Series

Accelerators

e+e-

Accelerator	Time between collisions (ns)	Luminosity (10^{30} $cm^{-1}s^{-1}$)	Energy (GeV)
CESR (CLEO)	4.2	2000	6
KEKB (Belle)	2	10,000	8 x 3.5
PEP-II (BaBar)	4.2	3,000	9 x 3.1
LEP (Aleph, Delphi, Opal, L3)	2200	50	101 (103??)

ep, pp, $p\bar{p}$

Accelerator	Time between collisions (ns)	Luminosity (10^{30} $cm^{-1}s^{-1}$)	Energy (GeV)
HERA (H1, Zeus)	96	14	920 x 30
TeV (DØ, CDF)	396 (132)	200	2,000
LHC (Atlas, CMS)	25	10,000	14,000

Source: PDB'98

Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

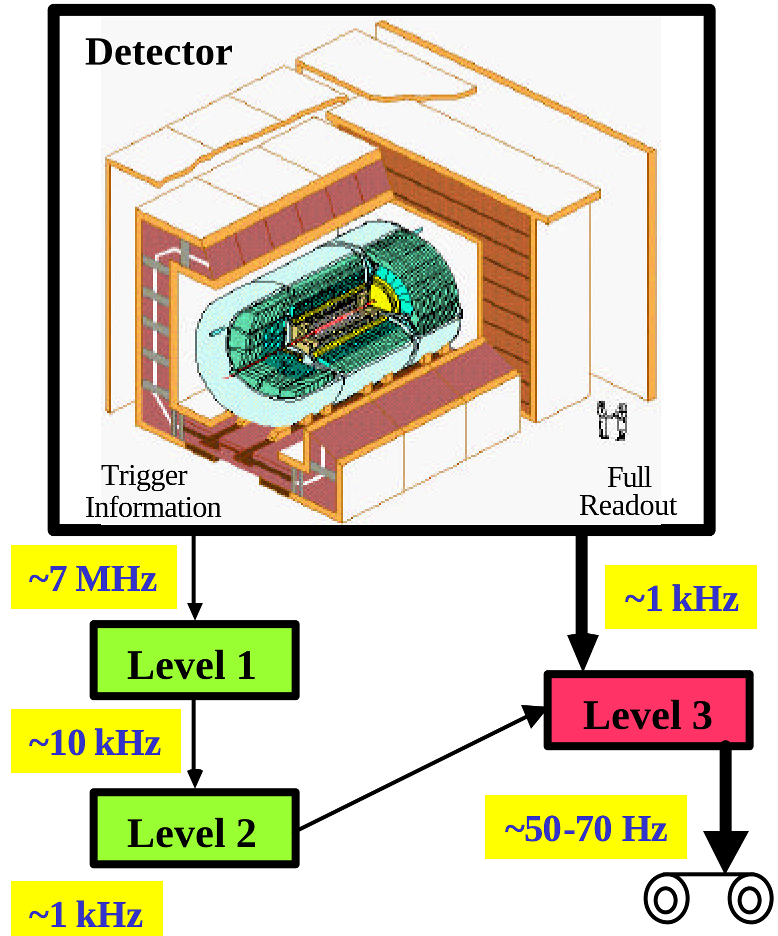
Why Trigger

It's obvious

Still, stunning to consider

Level	Accept Rate	TB/year	$ Tape (raw only)
Raw	7 MHz	25,700,000	52,700 m
L1	10 kHz	32,700	67 m
L2	1 kHz	3,270	6.7 m
L3	50 Hz	185	379,000

- Assume 50% duty cycle for accelerator
  - 15,768,000 working seconds in a year
- **Event size 250 kB**
- $ are for raw events only
  - $1 m per year including reco data



Instrumentation for HEP Experiments: Trigger

Gordon Watts
gwatts@fnal.gov

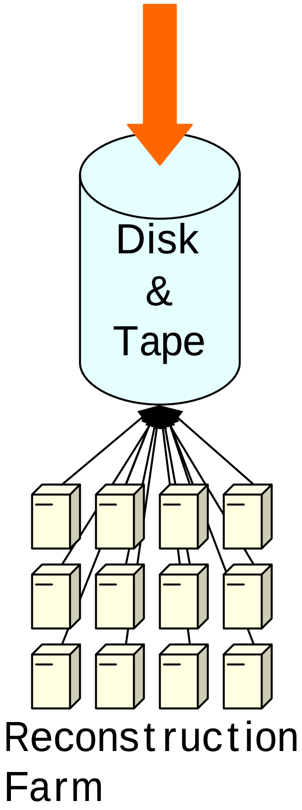
University of Washington, Seattle

Fermilab
March 21, 2000

Academic
Lecture Series

Trigger Design Backpressure

- Bandwidth to Archive (Tape Robot)
  - Tape I/O lags behind many other computer components.
  - A HEP experiment can write TeraBytes of data.
  - Media can run over a million US$ a year (CDF, DØ).
  - How much CPU power for post-triggering reconstruction? If it isn't done online?
- Cannot save all raw data all the time
  - Facilitates the study of Trigger Rates, Efficiencies
  - Enables one to repeat Reconstruction
    - BTeV proposes to write only reconstructed data.



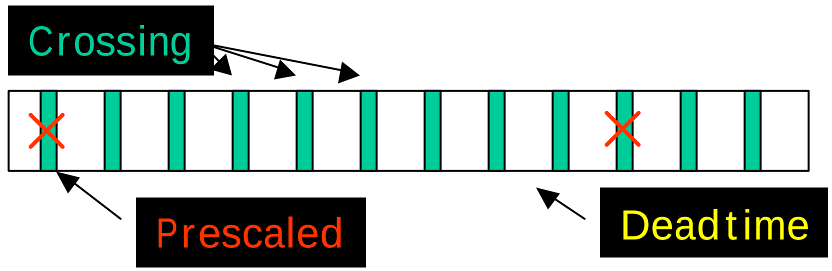
→ Eliminate Background As Early As Possible

Don't Prescale Physics!

Academic Lecture Series

Good Trigger - Bad Trigger

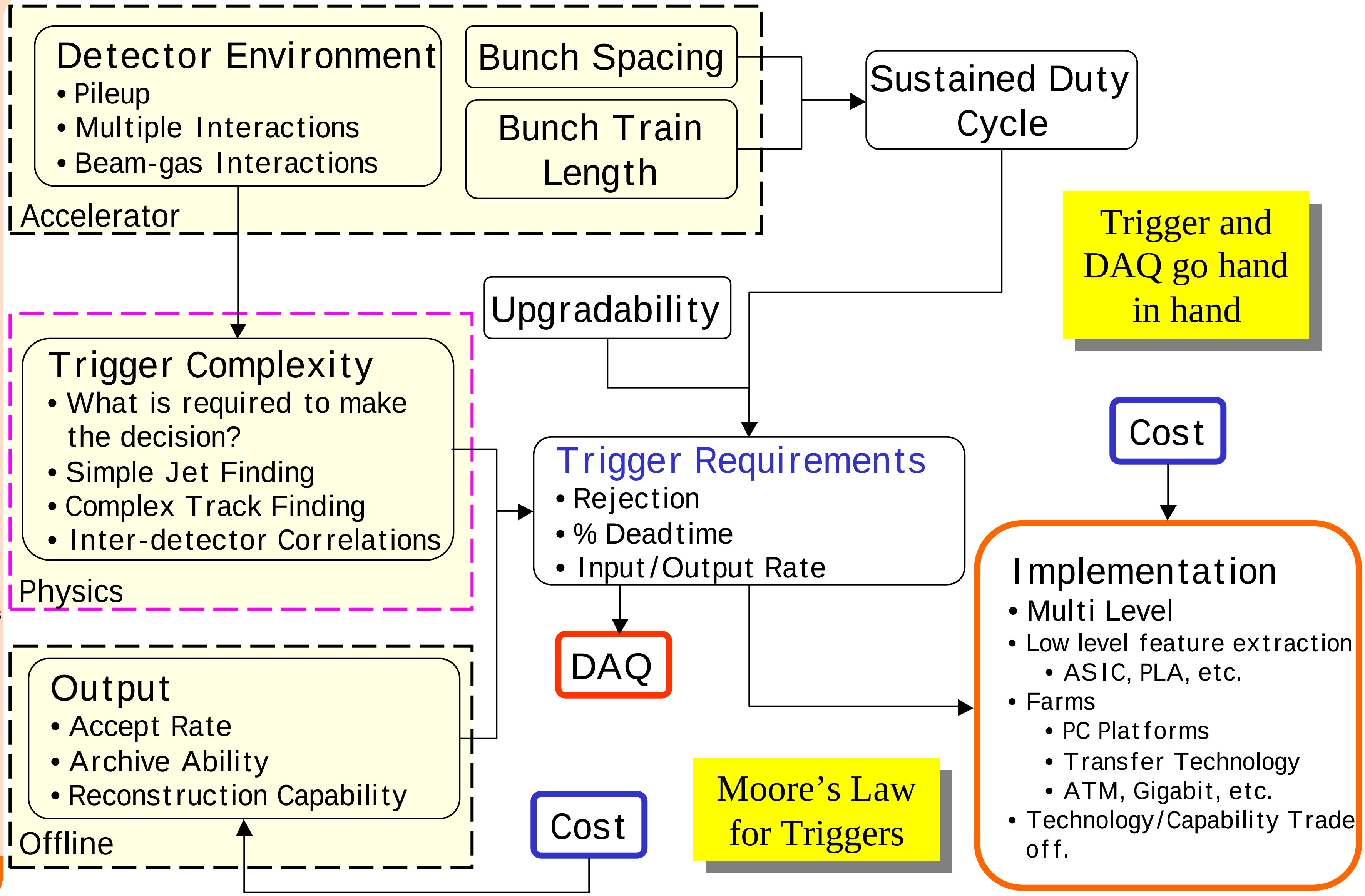
- A good trigger will capture all the physics it is designed to
  - As well as unexpected physics
  - Quickly Change configuration!
- It will ignore common processes
  - QCD backgrounds, soft scatters, detector backgrounds, etc.
- Golden Rule:
  - Don't make a random decision.



- Deadtime
  - % of time that collisions occur and the trigger can't look at them.
  - Caused by trigger processing (or readout) taking too long.
- Prescale
  - Throwing out 1 in n events of a certain type.
  - Cause by trigger selection not being fine enough, overwhelming the DAQ.

Academic Lecture Series

Constraints



Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

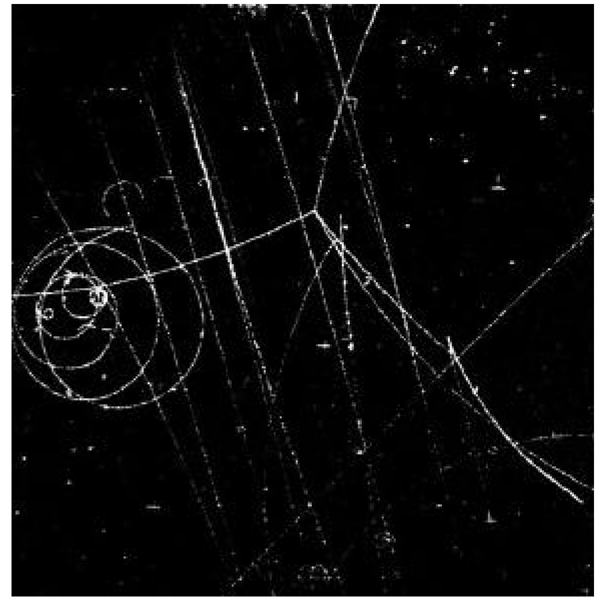
Fermilab
March 21, 2000

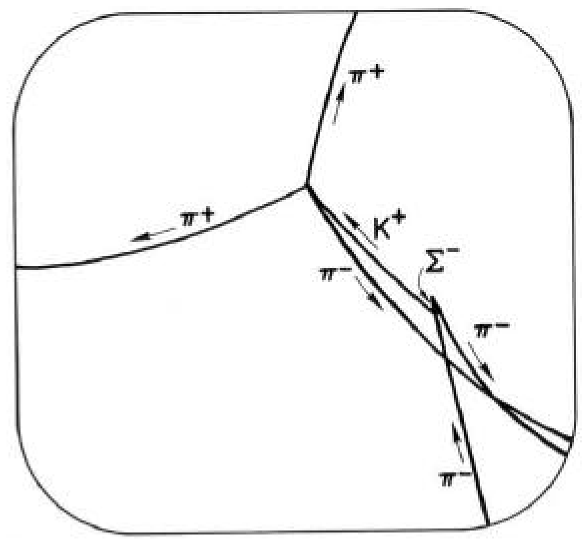
Academic
Lecture Series

History: Bubble Chambers

- Bubble Chambers, Cloud Chambers, etc. (4?)
  - DAQ was a stereo photograph!
  - Low level trigger was the accelerator cycle
    - Each expansion was photographed
  - High level trigger was *human* (scanners).
  - No Trigger
    - Only most common processes were observed.
    - Slow repetition rate.
    - Some of the high repetition experiments (>40 Hz) had some attempt at triggering.

Note: Emulsions are still used in detectors today





Instrumentation for HEP Experiments: Trigger

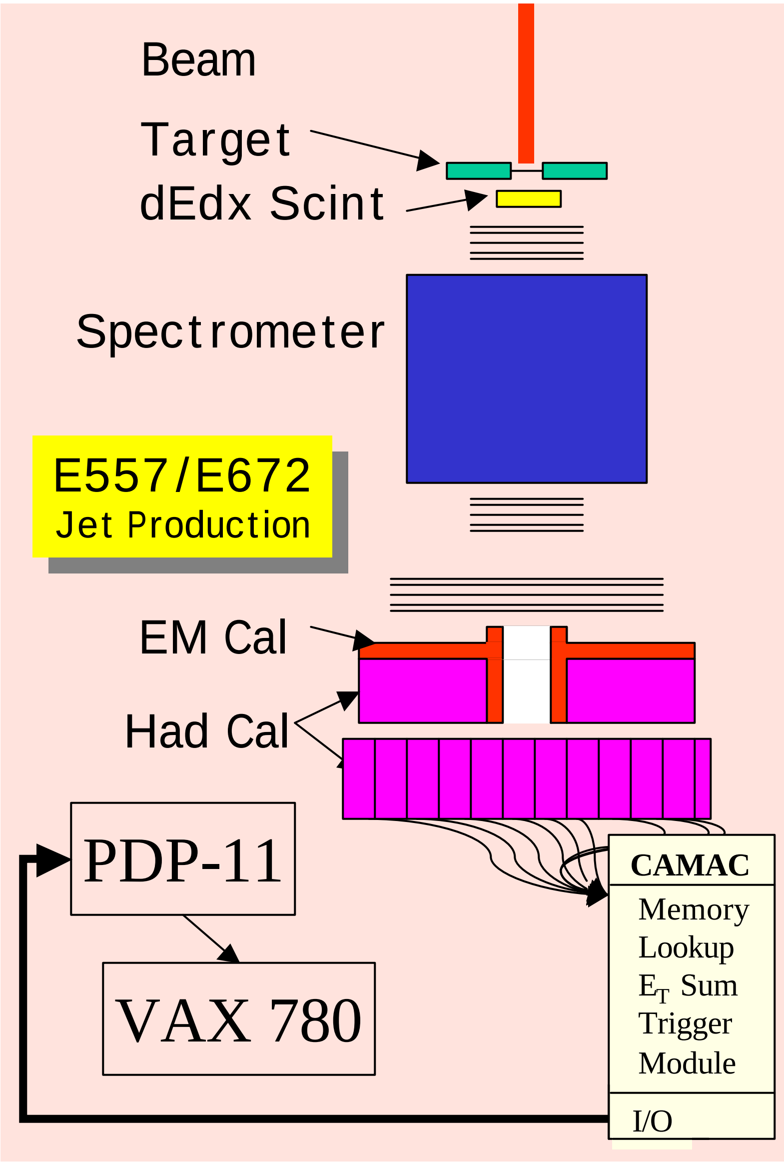
Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

Fermilab
March 21, 2000

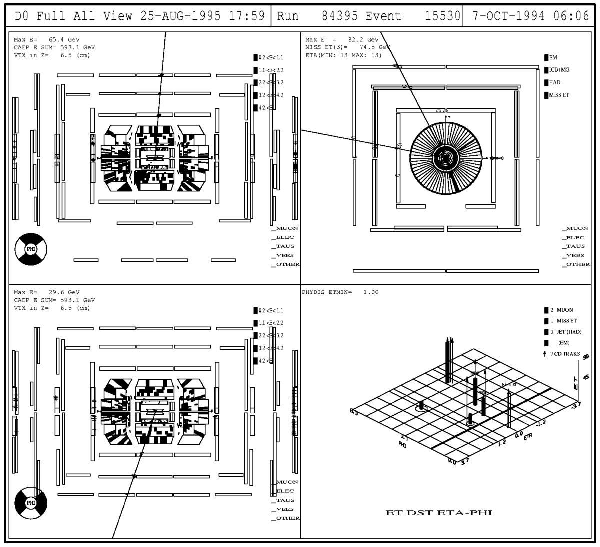
History: Fixed Target

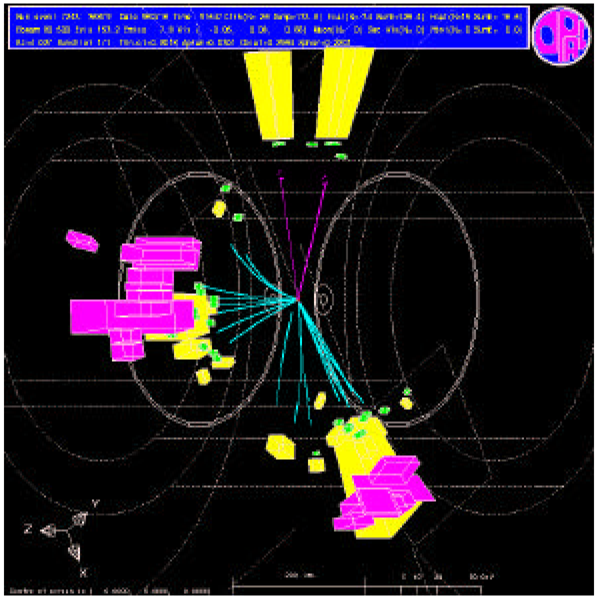
- Triggers around early (1964's Cronin & Fitch CP Violation Experiment)
- Limited
  - No pipelines
  - Similar to today's Level 1 Triggers
  - Large deadtime possible during readout
  - Good trigger required no further interactions after first trigger (24ns)



History: Modern Day

- Modern Day Detectors
  - ~million channels
  - Collision Frequency in the MHz
  - Multilevel Triggers
    - High end electronics
    - Capable of discarding common physics (background) in favor of more rare processes (like top quark production; 1 in a few billion).
  - Large farms to reconstruct data
  - Terabytes worth of analyzed data!
  - 100's of collaborators

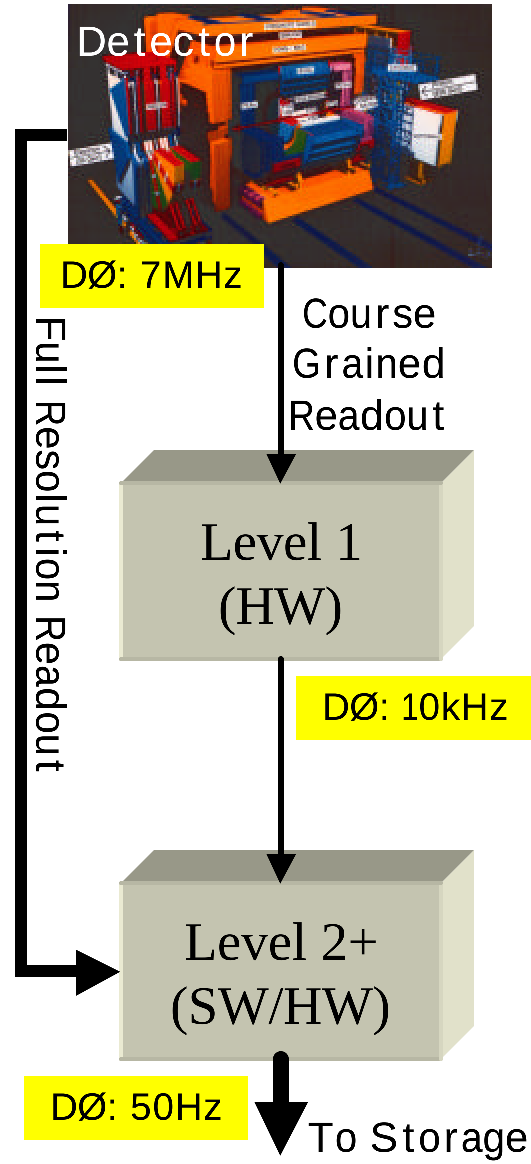




Typical Designs

- Required rejection is orders of magnitude
- Cannot do it at beam crossing rate
  - Algorithms to attain required rejection are too sophisticated.
  - Accelerator backgrounds can also contribute to the problem
    - e^+e^- vs pp
- Multi-Level trigger
  - Algorithms implemented in Hardware
    - Specialized, often matched to geometry of detector
  - Algorithms implemented in Software
    - Farm
  - Or a mix

Real Time

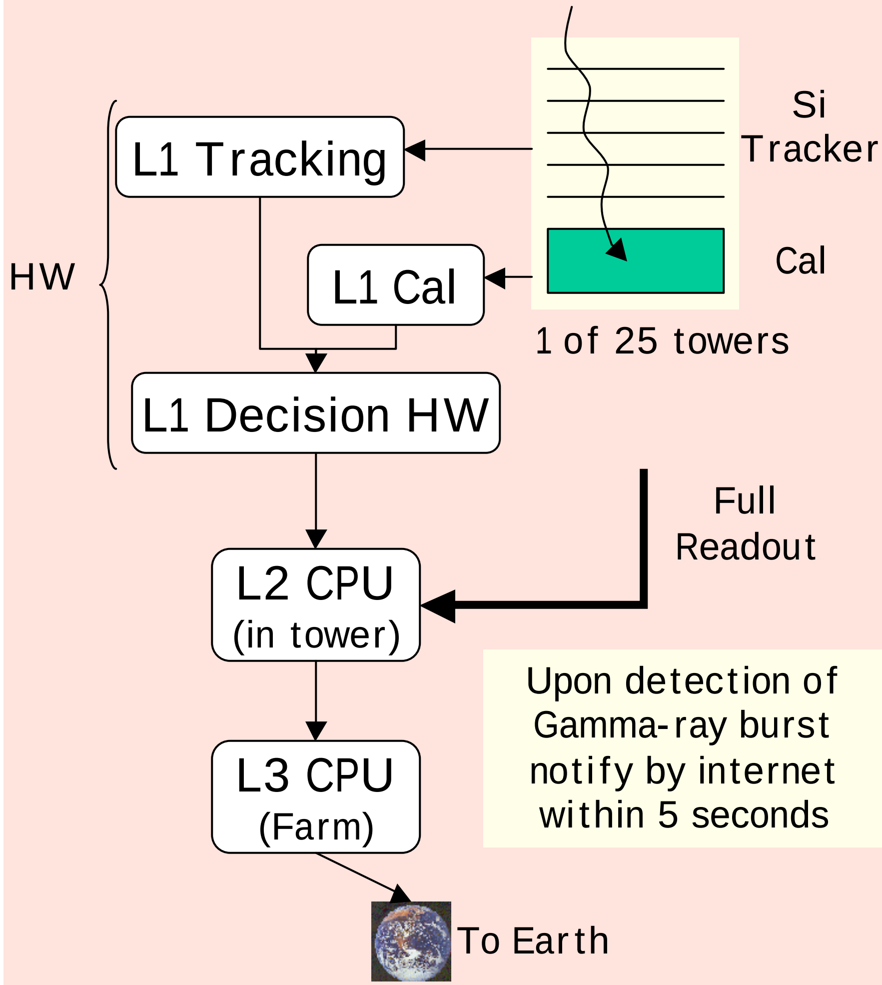


Multi Level Trigger

- Level 1 is hardware based
  - Identifies Jets, Tracks, Muons, Electrons
  - Operates on reduced or course detector data
- Level 2 is often a composite
  - Hardware to preprocess data
    - Some Muon processors, Silicon Triggers
  - Software to combine
    - Matches, Jet finders, etc.
- Level 3 is a farm
  - General Purpose CPUs
- Almost every one uses this scheme
  - Vary number and function of levels.

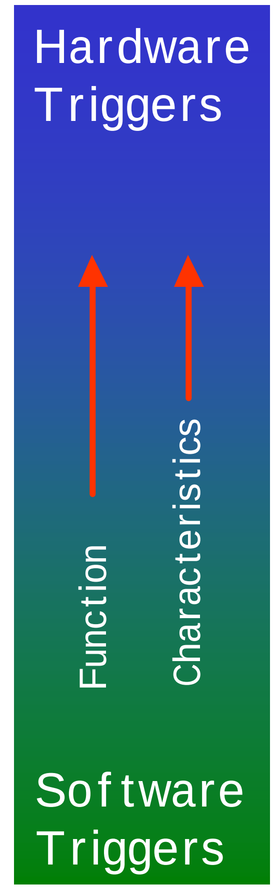
Even GLAST uses them

Gamma-ray Large Area **Space** Telescope



Typical Designs

- Higher level trigger decisions are migrating to the lower levels
  - TeV and LHC detectors have very tough Level 1 rejection requirements
  - Correlations that used to be done at Level 2 or Level 3 in are now done at Level 1.
- Recent Developments in Electronics
  - Line between software and hardware is blurring
  - Complex Algorithms in HW
  - Possible to have logic designs change after board layout.



Software Migration is following functional migration

Good, since complex algorithms often have bugs!

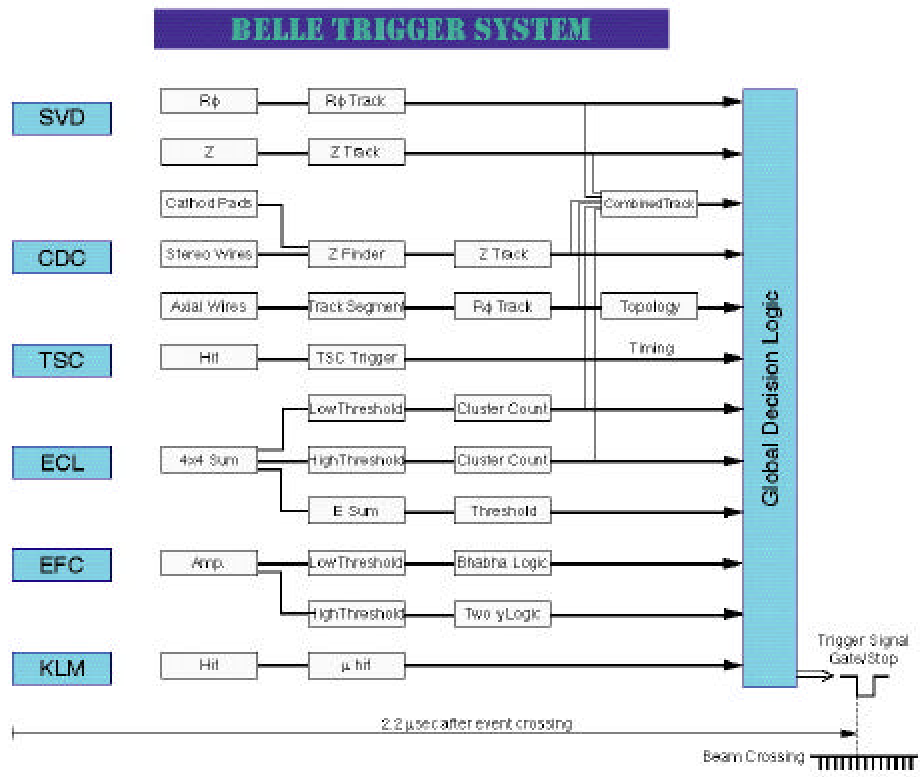
Algorithms in Hardware

- Cut out simple, high rate backgrounds
  - beam-gas (HERA)
    - z vertex
  - QCD (TeV)
    - jet energy, track matching
- Capabilities are Limited
  - Feature Extraction from single detectors
    - Hadronic or EM Jets, tracks, muon stubs
  - Combined at Global Trigger
    - EM Object + Track
- Characteristics:
  - High speed & Dead-timeless
  - Limited ability to modify algorithm
    - But thresholds typically can be modified
  - Algorithms Frequently Matched to the detector (and readout) geometry
    - Vertical Design
- Built from Modern Components
  - Custom (ASICs)
  - Programmable Logic Arrays (FPGAs, etc.)

Academic
Lecture Series

Belle Level 1 Block Diagram

- Each detector has its own trigger device
  - Track finder, jet finder, etc.
- These feed a global decision maker which has limited ability to make correlations
  - it usually does not get the raw data.



Instrumentation for HEP Experiments: Trigger

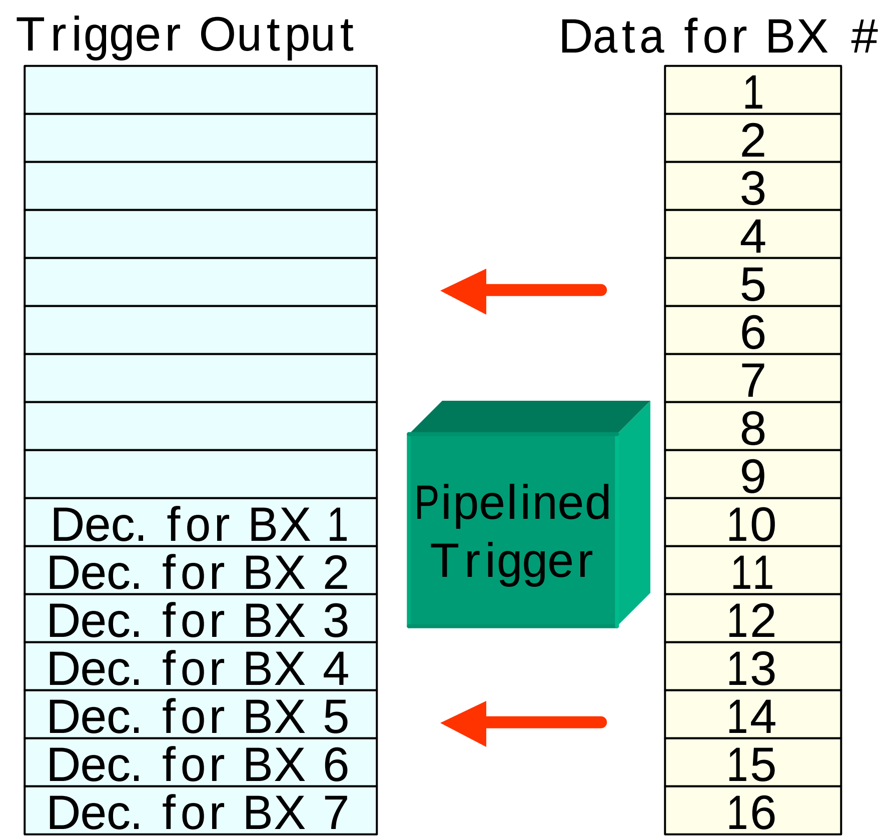
Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

Fermilab
March 21, 2000

Pipelines

- Trigger cannot cause deadtime during decision
  - Not only is Beam Crossing (BX) too run full algorithm
  - Many Simple algorithms take longer than a single BX
- To make dead timeless must have pipeline to store everything in FE
  - Switched Capacitor Arrays (SCAs)
  - DRAM
  - Shift Registers
  - Sample & Hold Shaping
  - Old fashion Delay Lines



- Most detectors us a combination of techniques
  - Some new ones, like BTeV use a uniform technique.

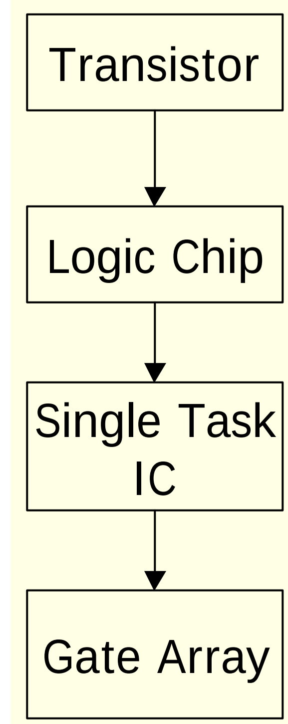
Track Finding

- Hardware is well suited to simple questions
  - A Calorimeter Tower over threshold
    - Gang together towers and do simple charge discrimination
  - Track finding is much more difficult
    - Must Implement hit searches and loops in hardware
- Track finding
  - Axial Only
    - Simple in that only the r-? view needs to be looked at.
    - Large Logic Arrays are the way to solve this problem.
  - Stereo Information
    - Have to determine where layers intersect.
    - Cuts down on background.
    - Shift Registers can be used, or more complex techniques.
    - Complexity increases as a function of the number of intersections there are along a stereo element.

The Field Programmable Gate Array

Academic Lecture Series

- Board on a chip
  - Revolutionized the way board design is done.
  - Logic design is not frozen when the board is laid out.
    - But much faster than running a program in microcode or a microprocessor.
  - Can add features at a later time by adding new logic equations.
  - Basically a chip of unwired logical gates (flip-flops, counters, registers, etc.)



Simple Programmable Logic Devices (SPLD)
Complex Programmable Logic Devices (CPLD)
Field Programmable Gate Arrays (FPGA)
Field Programmable InterConnect (FPIC)

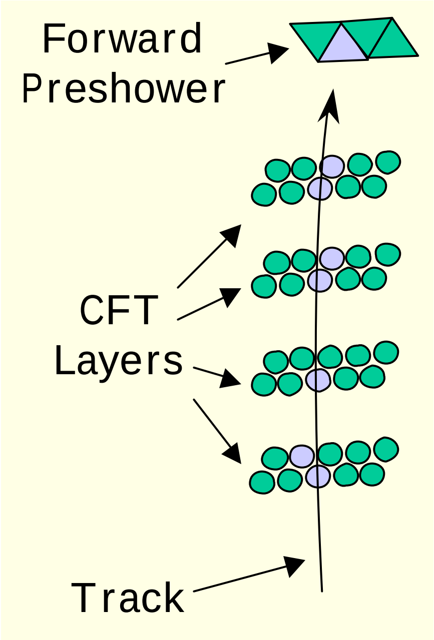
Several Types

- The FPGA allows for the most logic per chip.

Academic Lecture Series

Tracking at the TeV

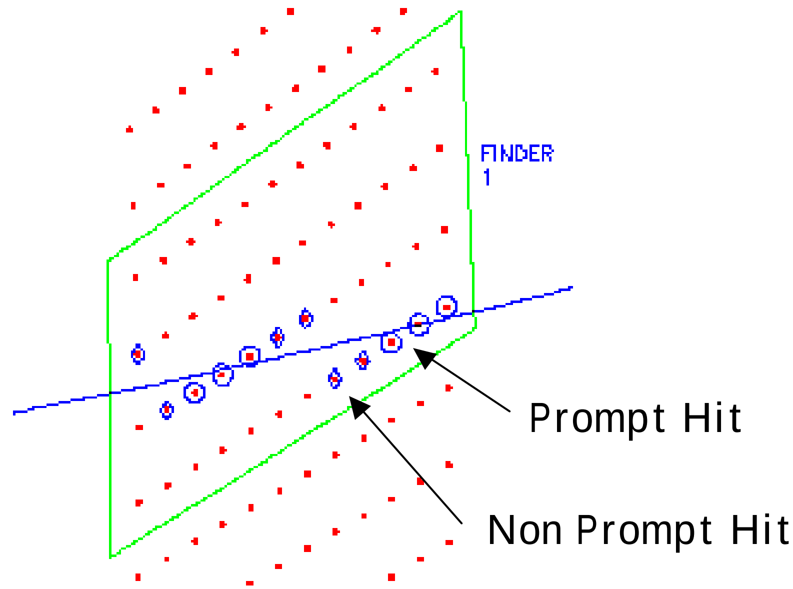
- Use FPGAs in the Track Trigger
  - Fiber Tracker (Scintillating Fiber) – DØ
  - Open Cell Drift Chamber - CDF
  - Finds Tracks in bins of p_T
    - 1.5, 3, 5, and 10 GeV/c @ DØ
  - Done by equations:
    - Layer 1 Fiber 5 & Layer 2 Fiber 6 & etc.
    - Inefficiencies are just more equations
  - Firmware becomes part of the trigger
    - Versioning
    - Fast & Flexible - Can be reprogrammed later.



- 80 sectors
- 1-2 chips per sector
- 16K equations per chip
  - One eqn per possible track.

Drift Chamber Tracking

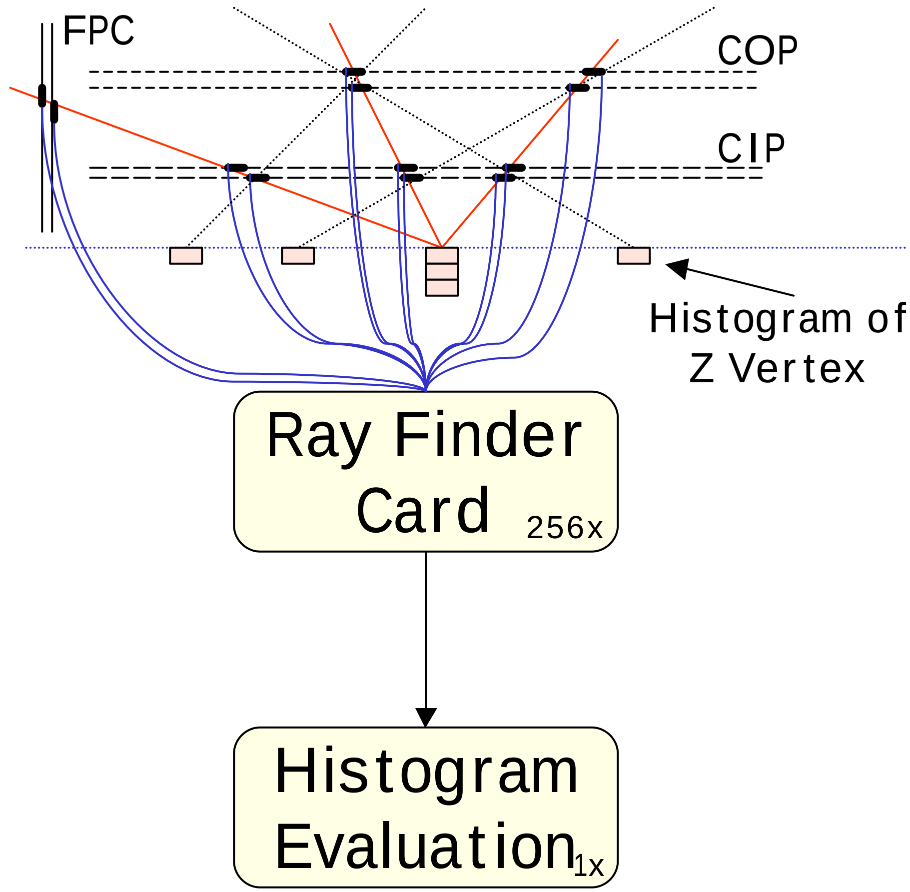
- DØ's Fiber Tracker gives instant position information
  - No drift time to account for.
- CDF divides hits into two classes
  - Drift time < 33 ns
  - Drift time 33-100ns
- This timing information is used as further input to their FPGAs for greater discrimination.
  - This is not done on every wire.



- Babar also uses FPGAs & LUTs to do track finding
  - 2ns beam crossing time!

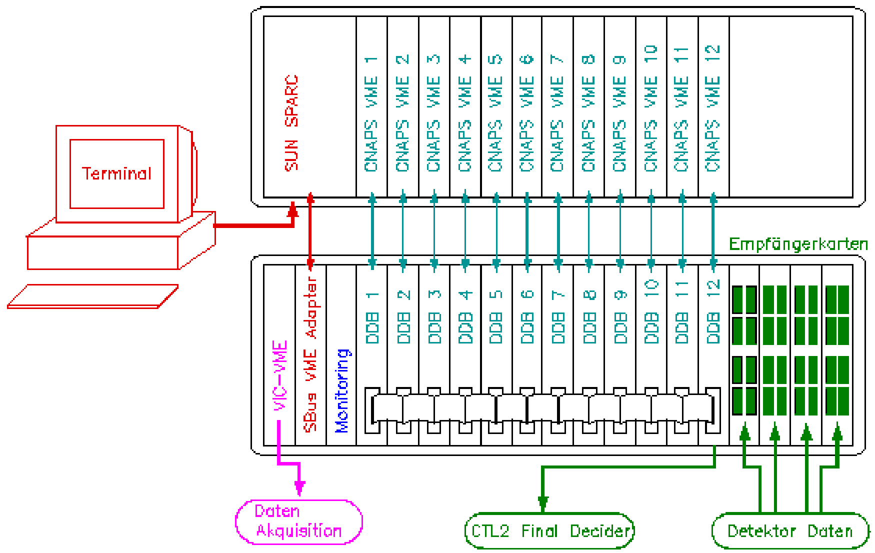
H1 Vertex Finder

- Beam-Gas is the largest cause of background at HERA
  - Vertex position is not near interaction point
- Vertex Trigger
  - Does tracking by finding rays using a custom CMOS gate array
  - Histogram the z
    - Uses FPGA to build the histogram
    - High speed static RAM lookup to find result.



Neural Networks

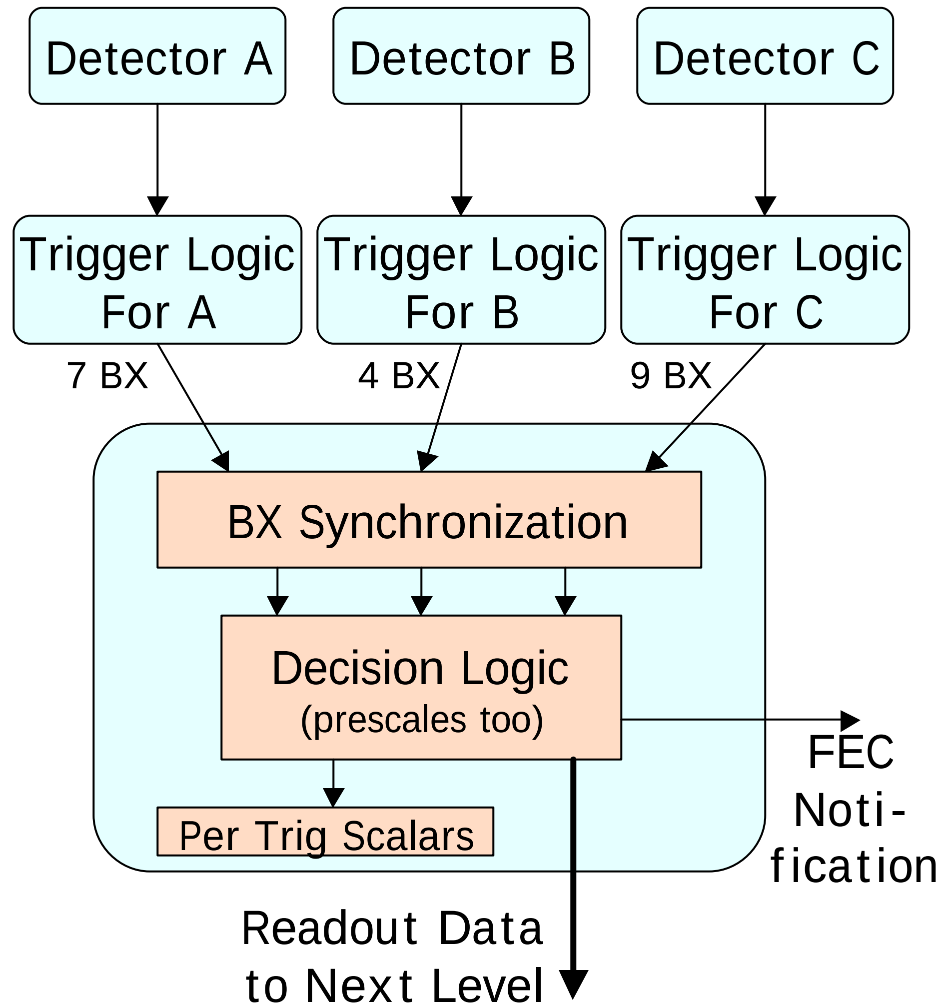
- H1 has a NN Trigger
  - Used to look for missed or odd physics and reject certain backgrounds.
- Neural Net trigger is based on CNAPS chips
  - Simple Massively Parallel Processor
  - Suited to training and evaluation of many-node NN.
    - Up to 64 hidden nodes,
    - 64 inputs.
  - 20 ?s decision time
  - 9 units, trained on physics (bb, cc, etc.) and the same background.
- Trained offline
  - ~ 2000 signal events
  - ~ 2000 background



- Preprocessor Board
  - Formats data (FPGAs)
  - Can implement simple algorithms (jet finding)
- CDF implemented a tau trigger
  - Analog Chip (Intel ETANN)
  - Worked well enough to see a W peak

Trigger Manager

- Often first time there are inter-detector correlations
  - simple matching
- Decision Logic is always programmable
  - Often part of Run configuration
  - Human Readable Trigger List
- May manage more than one Trigger Level.
- Usually contains scalars
  - Keeps track of live-time for luminosity calculations.



Belle Inputs to Global

- Belle's inputs into the global are typical
  - # of tracks are done by bit numbers
  - Correlation information is done the same way.
- Some experiments have 256 or more inputs to L1 Global.

Detector		label	#Bits	comments
CDC	rφ	$N_{CDR-Full}$	2	CDC Full Track (N = 1, 2, ≥ 3)
		$N_{CDR-Short}$	2	CDC Short Track (N = 1, 2, ≥ 3)
		CDC:B-B	1	CDC Back-to-Back Tracks
		CDC:open	1	$\phi_{open} > 90°$
	Z	N_{CDZ}	2	CDC Z-track (N = 1, 2, ≥ 3)
TSC		Timing	1	"Timing" Trigger
		N_{TSC}	2	# of TSC hits (N=1,2,≥3)
		TSC:multi	1	$N_{TSC} \geq Min$ (=2 now)
		TSC:patt	1	TSC pattern (1-n bacck-to-back now)
ECL		E_{Tot}	3	$E_{Tot} > E_1, E_2, E_3$
(CsI)		N_{icl}	3+1	Number of Isolated clusters (0-7)+1
		CsI:BB_{pre}	1	CsI Bhabha (prescaled)
		CsI:BB	1	CsI Bhabha (non-prescale)
		CsI:Cosmic	1	CsI Cosmic flag
		CsI:Timing	1	CsI(Neutral trigger) Timing
EFC		EFC:BB	1	EFC Bhabha
		EFC:Tag	1+1	Tag for two-photon + reserve
CALIB		Random	1	Random
		CALIB	2	Calibration Triggers [a)]
KLM[a)]		MU	1	Muons
SVD[a)]			6	SVD Tracks
TRK [a)]			4	Loaclly comb. track
		Total	28+13	

a) these are reserved for future implementation. [revised 98.12.27]

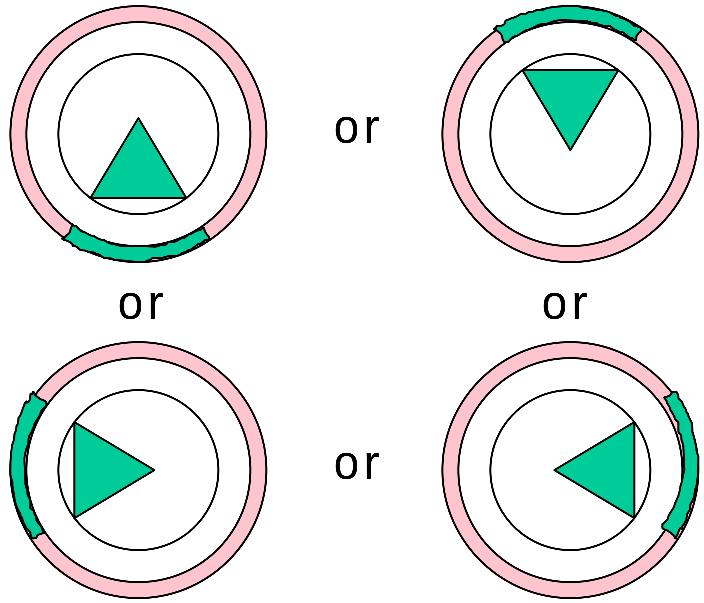
Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

Academic
Lecture Series

Decision Logic

- Simple AND requirements
  - A jet AND a track and a MUON stub
- More Complex OR requirements
  - A jet in Quad 1 with a track in Quad 1 OR a jet in Quad 2 with a track in Quad 2 etc.
- FGAs and truth tables well suited to this.
  - Can be arbitrarily complex trigger requirements.



- Prescales are adjustable…

Instrumentation for HEP Experiments: Trigger

Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

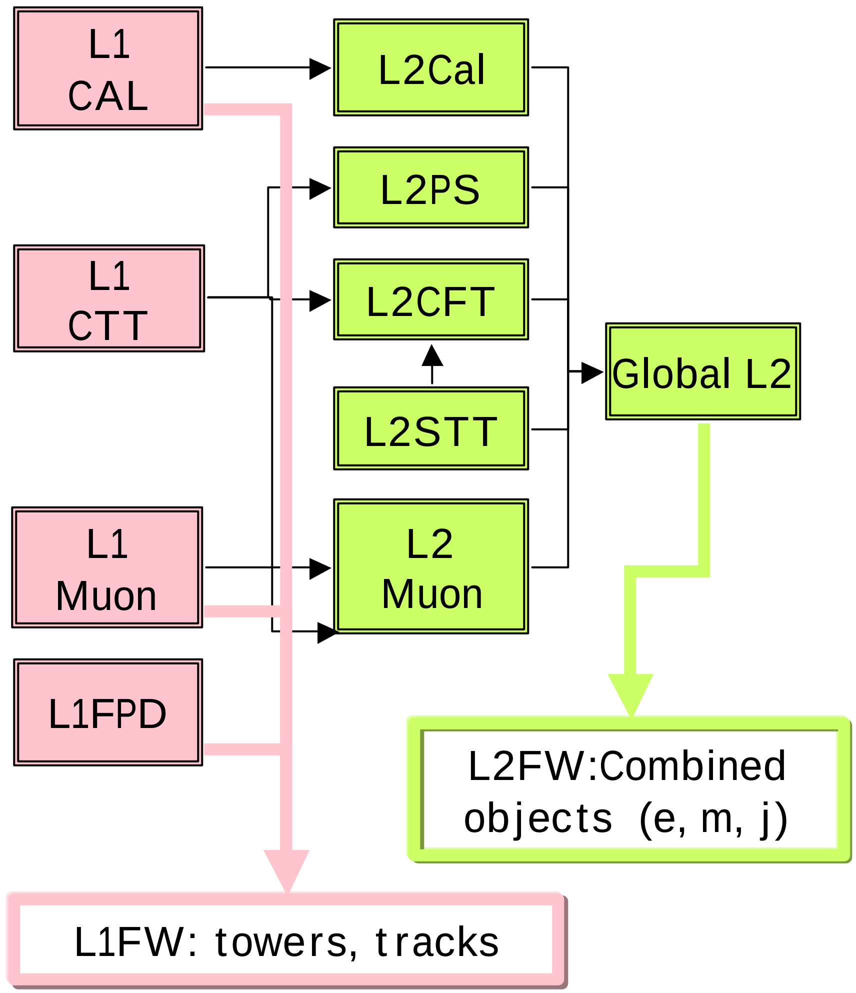
Fermilab
March 21, 2000

Algorithms in Software

- Sophisticated Algorithms
  - Frequently separating background physics processes from the interesting processes.
  - Some experiments run their offline reconstruction online (Hera-B, CDF)
    - Perhaps 2D tracking instead of 3D tracking.
  - Data from more than one detector often used.
- Two common implementations:
  - **DSPs tend** to live at lower levels of the trigger.
    - Stub finders in muon DØ's muon system.
    - Transputers in ZEUS' L2, DSPs on HERAB L2 & L3
  - **CPU Farms** tend to be at the upper end
- Sometimes difficult to classify a system
  - Blurring of line between software and hardware.

Hybrids – Level 2 at TeV

- Use a combination of both Hardware and General Purpose Processors
- CDF & DØ's Level 2 Trigger
  - Each box is a VME crate
  - Contain specialized cards to land and reformat data from detector front-ends
  - Contain ALPHA processor to run algorithms.

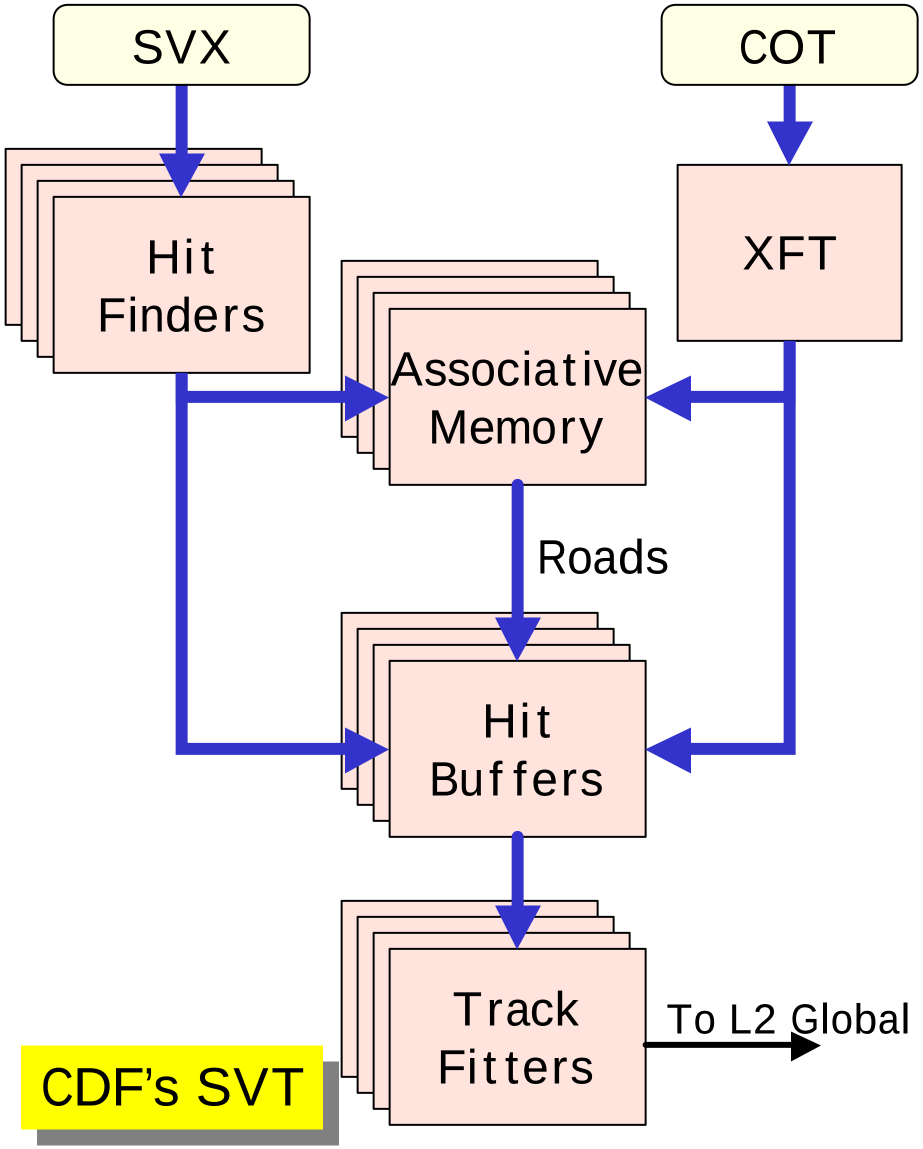


DØ's Level 2

Academic Lecture Series

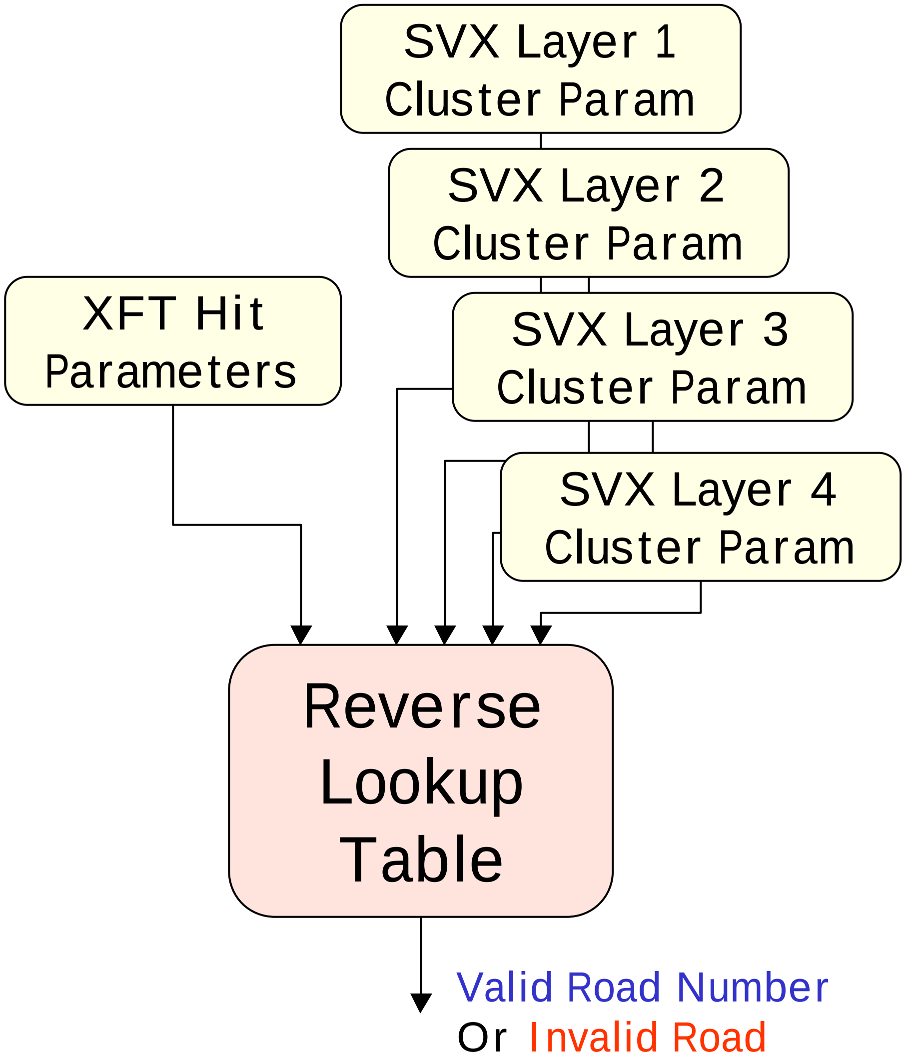
Hybrids – SVT

- Both CDF & DØ will trigger on displaced tracks at Level 2
  - DØ's will be another specialized set of L2 crates.
- Input to Level 2 Global
  - Select Events with more than 2 displaced tracks
  - Resolution is almost as good as offline.
  - Refined track parameters
- Track Fitters
  - CPU Farm.



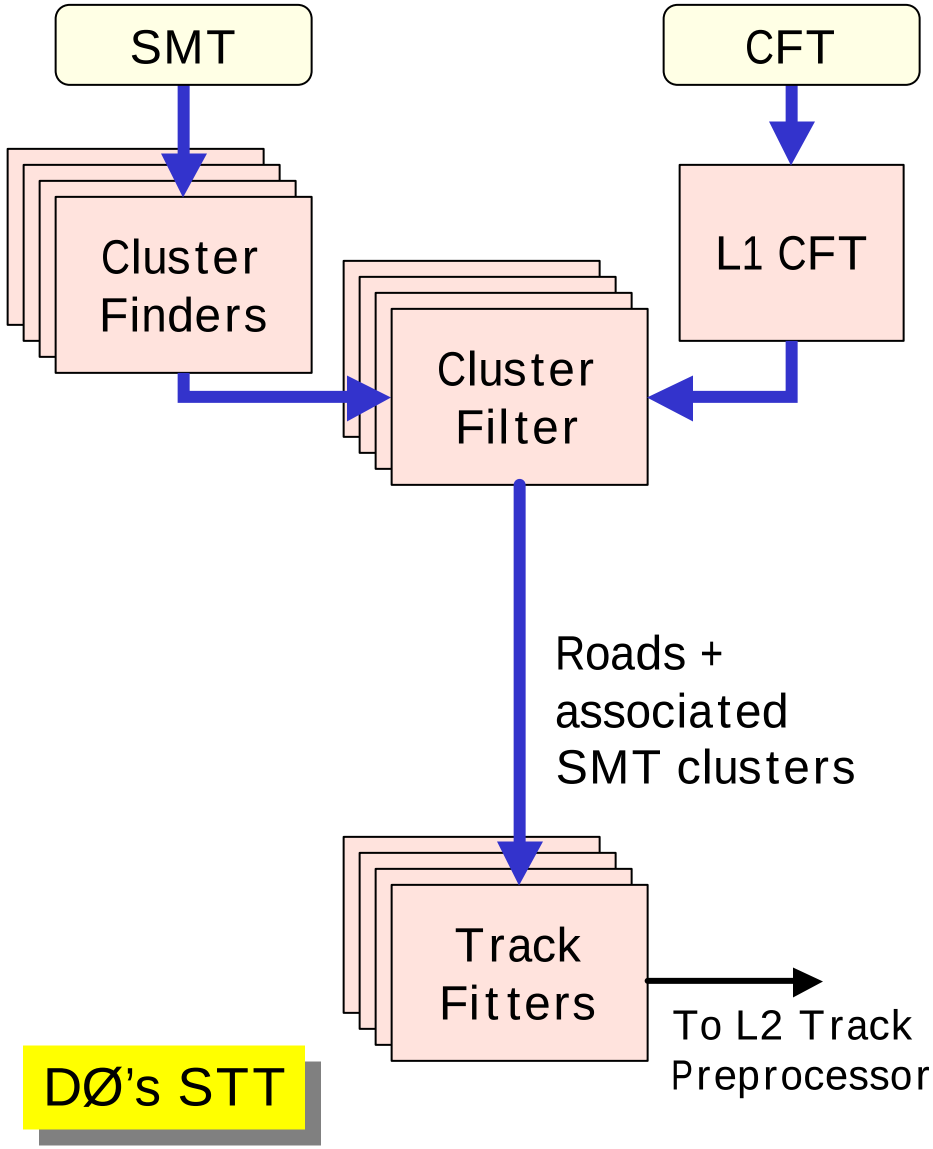
Associative Memory

- Associative Memory
  - High speed matching of 4 SVX clusters and a XFT cluster
    - To a valid road (p_T > 1.5 GeV/c)
  - A Reverse Lookup
    - Normally a valid road index would give back the XFT and SVX hit parameters
    - Operates similar to a CAM.
  - Each AM Chip does 128 *roads.*
  - Custom CMOS.



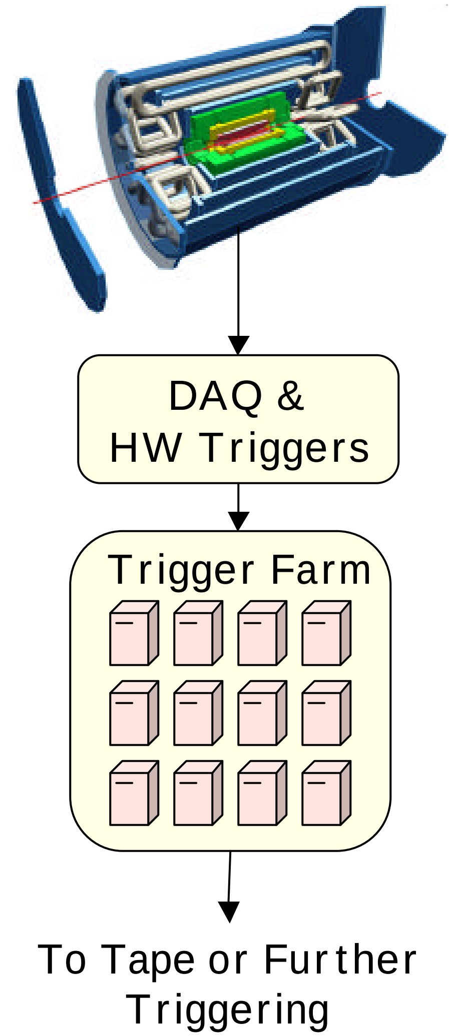
DØ SVT

- DØ's Silicon Track Trigger is similar in design to CDF's
- Operates at a reduce speed
  - 10kHz instead of 50 kHz.
- Uses FPGAs instead of Associated Memory.
  - Track fitters also use DSPs



Farm Triggers

- Industry has revolutionized how we do farm processing
  - Wide scale adoption by HEP.
  - Online and Offline.
  - One CPU, one event
    - Not massively parallel
- Data must be fed to farm
  - As many ways as experiments
  - Flow Management & Event Building
- Farm Control
  - Distributed system can have 100's of nodes that must be kept in sync.



Readout Control & Event Building

- Events come from many Front End Crates (FECs)
  - Many Sources directed at the one CPU doing the work.
  - Directed
    - FECs know what each node needs and start sending it
  - Requested
    - Farm Node Requests the data it wants (ROI).
- Event Builder – Final assembly of all FECs
  - CDF has a separate machine (16)
  - DØ does it in the Trigger Farm Node
  - ATLAS, CMS, HERA-B do it bit-by-bit.

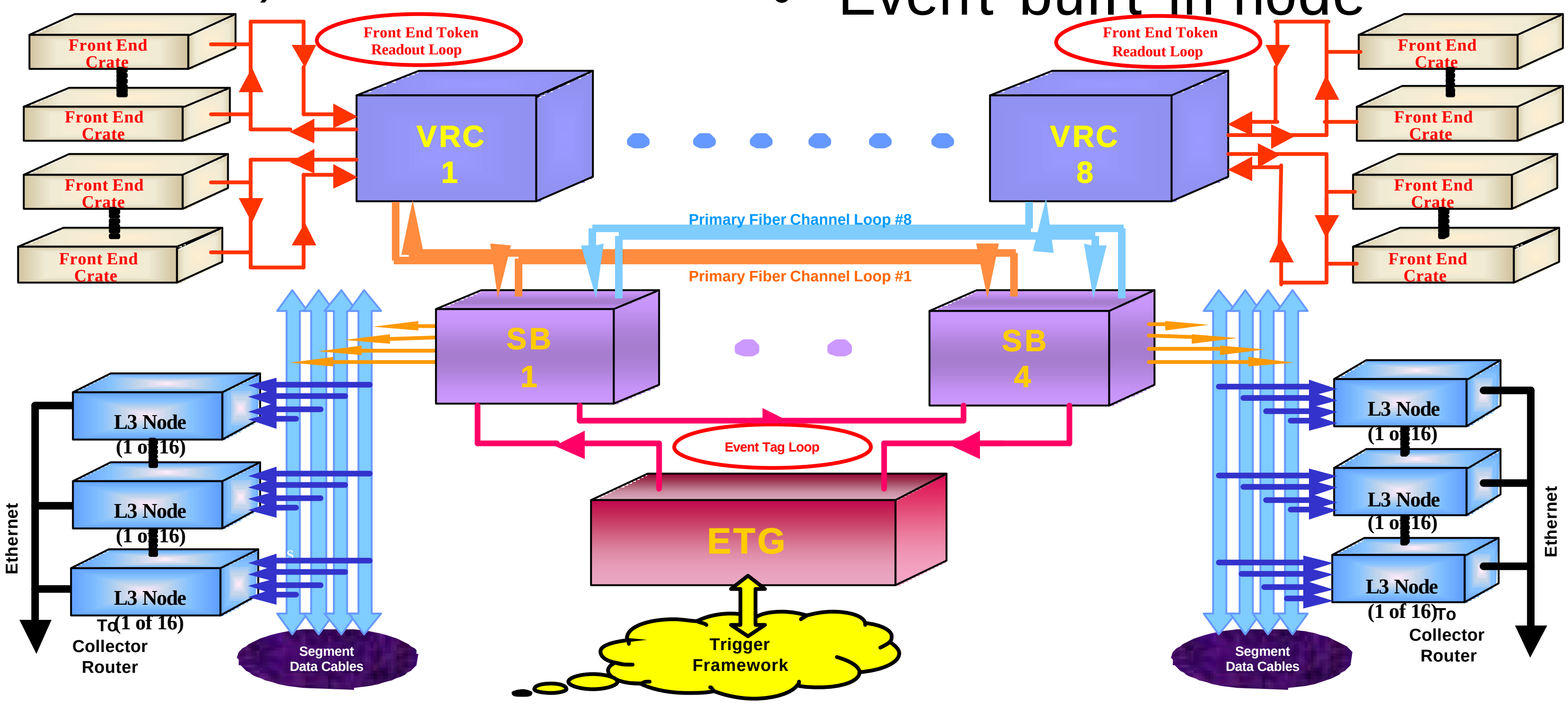
Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

Academic
Lecture Series

DØ

- Data Flows as soon as there is a L2 Accept
  - Destination is unassigned
  - Data Driven (each packet contains an event number).
- Backpressure accomplished via recirculation loops
  - When full, no new data can enter the system.
- Event built in node



Instrumentation for HEP Experiments: Trigger

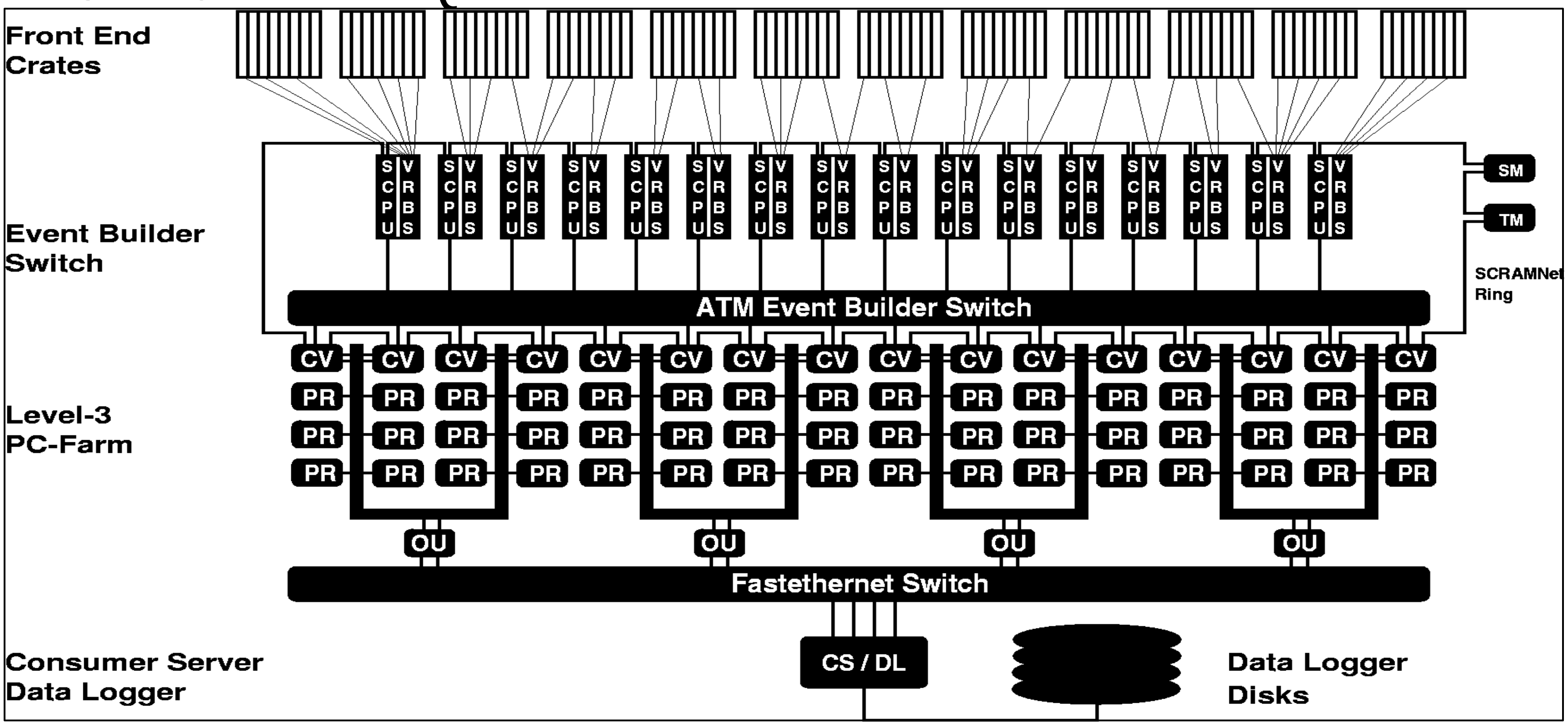
Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

Fermilab
March 21, 2000

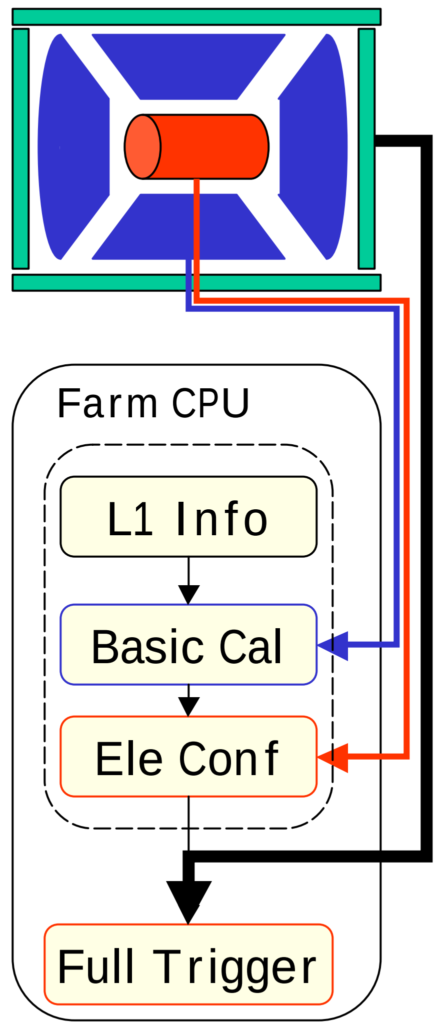
CDF

- Data Flows when Manager has Destination
  - Event Builder Machines
- One of first to use switch in DAQ.
- Dataflow over ATM
  - Traffic Shaping
- Backpressure provided by Manager.



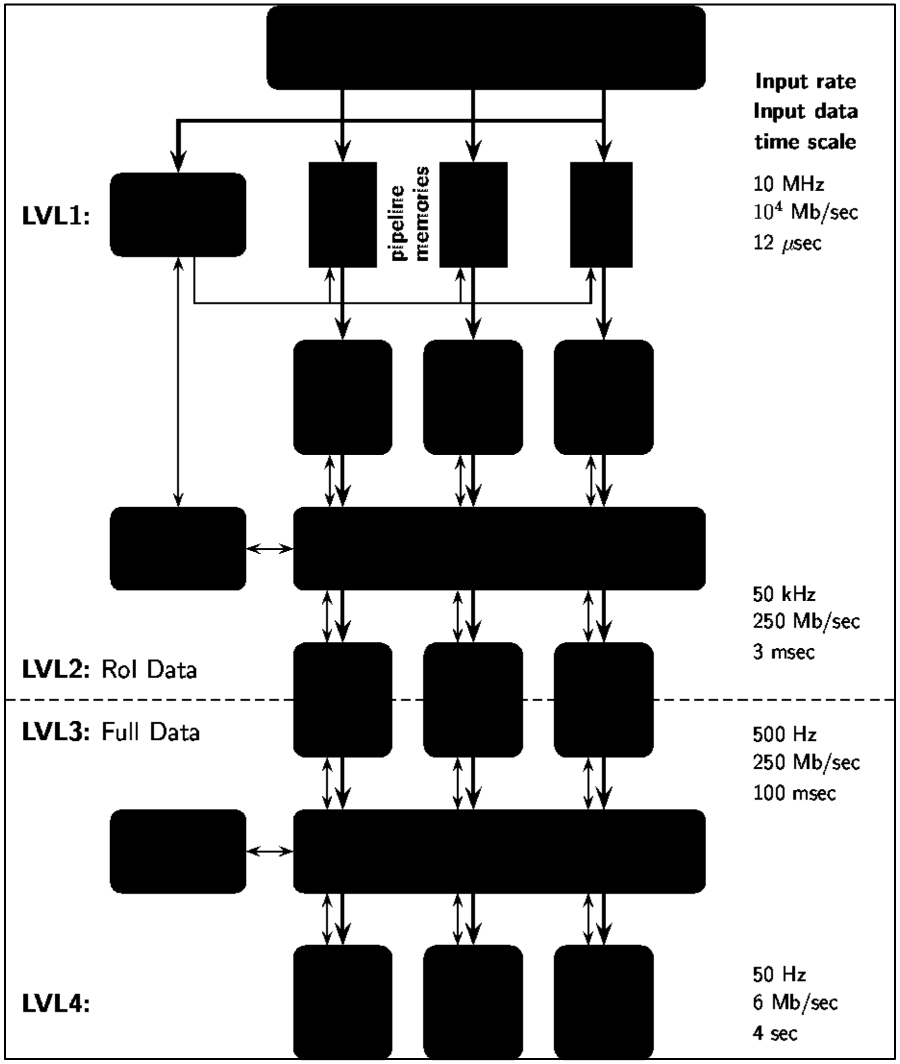
Regions of Interest (ROI)

- Bandwidth/Physics Compromise
  - Farm usually reads out entire detector
  - HW often look at single detector
- ROI sits in the middle
  - CP Farm CPU requests bits of detector
    - Uses previous trigger info to decide what regions of the detector it is interested in.
  - Once event passes ROI trigger, complete readout is requested and triggering commences.
- Flexible, but not without problems.
  - Pipelines in front ends must be very deep
  - Farm decisions happen out-of-event-order
    - Pipelines must be constructed appropriately.
- ATLAS, HERA-B, BTeV…



HERA-B

- Looks for B_0 to J/? K^0_S
- Level 1 is pipelined
  - Results distributed to L2 processors
- Level 2 processors request only what data they want
  - If pass, request full readout.



Academic Lecture Series

Instrumentation for HEP Experiments: Trigger

Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

Fermilab
March 21, 2000

High Speed Data Links

- Data Rate into Farm is High
  - Require high bandwidth technology
- **Commodity** or Custom Technology
  - Commodity Technologies
    - ATM
    - Gigabit Ethernet
    - Fibre Channel
  - Custom Technologies
    - Often built on off-the-shelf protocols (and driver chips), without the full blown protocol (like IP)
- ATM
  - Wasn't adopted by the mass market
  - Still expensive for what you get.
  - Not obviously well suited to physics
    - Cell Size, etc.
  - GigaBit looks much more attractive now.

Control

- The event farms can have 100's of nodes.
  - Complex configuration possible
    - Especially during commissioning and calibration runs
  - Must be automated
- Farm Steward
  - A Resource Manager
  - Communicates with the rest of the trigger
    - **CORBA** – defacto standard
    - **TCP/IP** – often with layers, isn't cross-platform.
- Physics Algorithms Framework
  - Framework optimized for fast processing
    - Algorithms become plug-in modules
  - Designed to run both online and offline.

Academic Lecture Series

Monitoring

- Monitoring
  - Continuous dump of L1 scalars and higher level pass/fail rates
  - Control room monitoring of those rates as a function of time
  - CPU Node monitoring
- WEB Access
  - Many experiments put real-time data on the web
    - trigger rates, pictures of the latest event, DAQ status, etc.

Farm OS

- Intel Compatible CPUs have a lock
  - Commodity, cheap, very fast
    - Rumors of 1 GHz AMD Athalon at COMDEX this week with no nitrogen cooling??
  - There are a number of OSes that run on this platform
    - BeOS, Linux, Solaris, Windows NT
  - Linux seems to have won out
    - Similar to HEP's mainframe tools: UNIX
    - DØ is using Windows NT on its L3 Farm

Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

Conclusions

- Sophisticated Triggers moving into HW
  - Algorithms too complex for hardware can be put on a single chip.
  - Software algorithms are becoming more complex to retain the same rejection rates.
- Blurring of Software and Hardware
  - Programmable Chips (FPGAs) common in all levels of Trigger/DAQ.
- Two rounds of experiments coming on line
  - Trigger Farms with 100's of computers
  - ATM switch concept test
- We've Followed the Commodity Market
  - PLAs, Cheap CPUs
  - Where is it heading now??
    - Embedded systems, small embedded systems with network connections.

Academic Lecture Series

Tevatron Near Future

- Latest Schedule has Run 2a starting **March 1, 2001.**
  - Detectors rolled in and taking data.
- Commissioning, calibration, understanding new detectors & triggers…
- Run 2b
  - Starts after 2-4 fb^{-1}
  - Replace parts of Si
  - Upgrade Tracking Trigger for high luminosity environment?

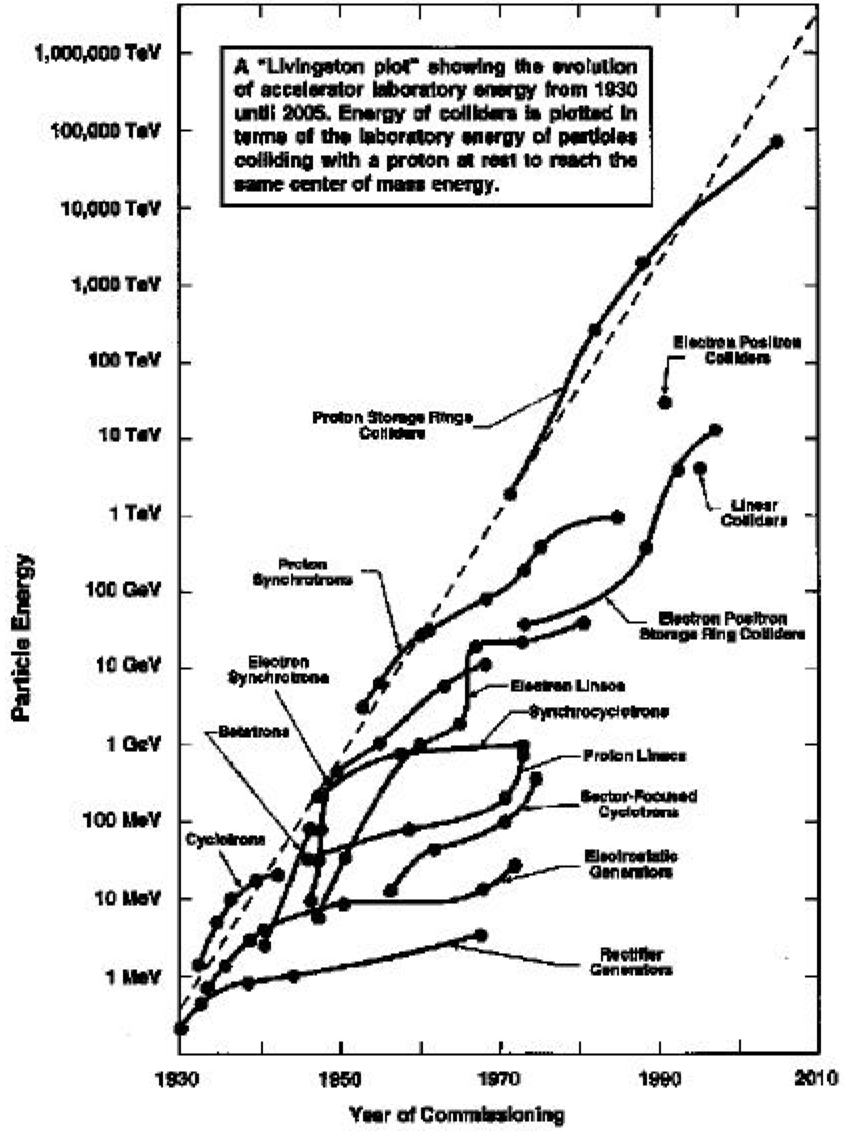
CHEP 2001
Will have some real experience to report on!

Future

- Triggers are driven by their environment.
- What Accelerators in the Future
  - Near Term:
    - Linear Collider (LC)
    - Muon Collider
    - Very Large Hadron Collider (VLHC)
  - Long Term:
    - ?? Era of large Colliders drawing to a close?

Future

- Technology has driven accelerators to this day



Academic Lecture Series

Instrumentation for HEP Experiments: Trigger

Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

Fermilab
March 21, 2000

Future

- Silicon Triggering
  - Pixels
  - On board Triggering

Instrumentation for HEP Experiments: Trigger

Gordon Watts
gwatts@fnal.gov

University of Washington, Seattle

Fermilab
March 21, 2000

Future Trends

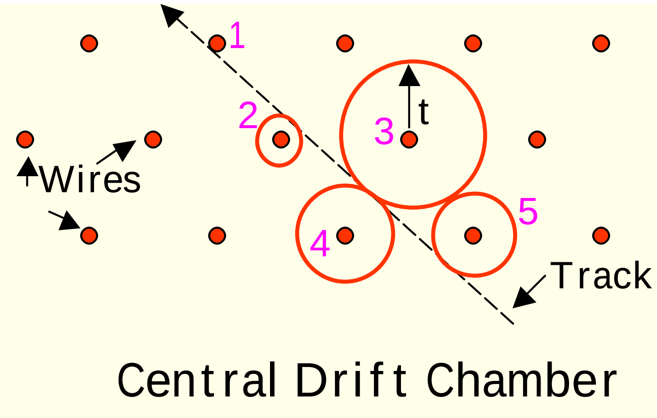
- HEP has stolen from the market place before
  - High Speed Networking
  - PLAs
  - Commodity CPUs
  - Not always the best match
- Where is the market moving now?
  - Small networked devices
  - Wireless devices and very-local area networks
  - embeded systems
- How will this affect triggering?
  - Triggers part of detector based readout chips
  - Fewer central processors at earlier stages of trigger
  - More complex trigger decisions at earlier times

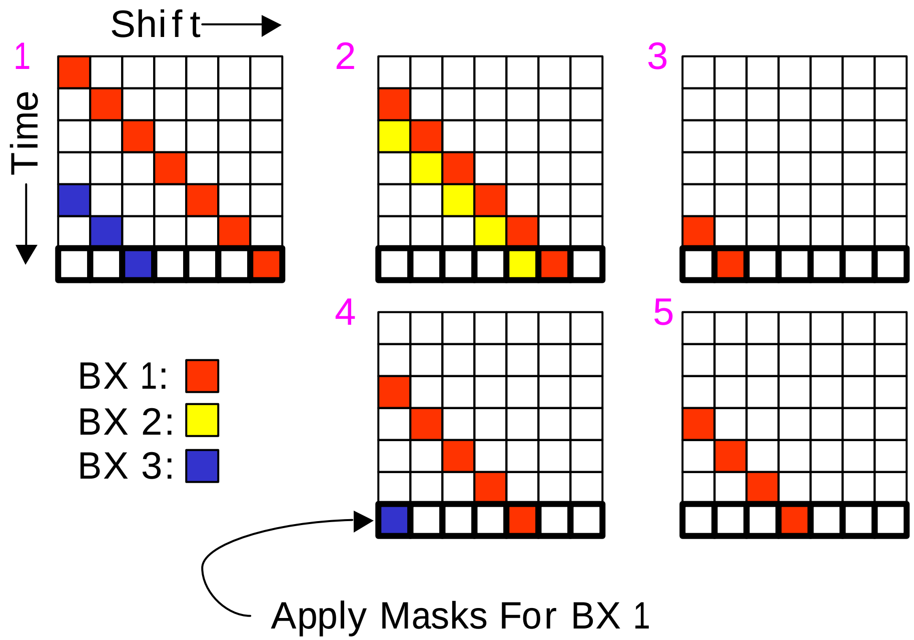
Gordon Watts
gwatts@fnal.gov

University of
Washington,
Seattle

Track Finding In Drift Chambers

- If drift time is larger than BX
  - Must wait several BXs until all data arrives.
  - In meantime data may have arrived from an earlier BX.
  - CDF's COT: Drift time is xx BX long.
- Use shift register
  - One Shift Per BX
  - Apply masks to shift register after a number of BXs
  - ?? 16,000 masks?? Where was that??





Detectors

Detector	Number of Channels	Silicon Part of Trigger?	Input Trigger Rate	Largest (Non) Physics Background
CLEO	400,000	No	L1: 72 MHz L2: 1 kHz Tape: <100 Hz	electron pairs
Belle	150,000	Not Yet	L1: 50 MHz L2: 500 Hz Tape: 100 Hz	BhaBha & ??
BaBar	150,000	No	L1: 25 MHz L3: 2 kHz Tape: 100 Hz	BhaBha & ??
H1, ZEUS	500,000	No	L1: 10 MHz L2: 1 kHz L3: 100 Hz Tape: 2-4 Hz	Beam-gas
HERA-B	600,000	Yes (L2)	L1: 10 MHz L2: 50 kHz L3: 500 Hz L4: 50 Hz Tape: 2 Hz	Beam-wire scattering Inelastics
Aleph, Opal, L3, Delphi	250-500k	No	L1: 45 kHz Tape: 15 Hz	beam-gas
CDF (Run 2), **DØ** (Run 2)	1,000,000	Yes (L2)	L1: 7 MHz L2: 10-50 kHz L3: .3-1 kHz Tape: 50 Hz	QCD, pileup, multiple interactions