Stereo XFT Finder

Production Design Proposal

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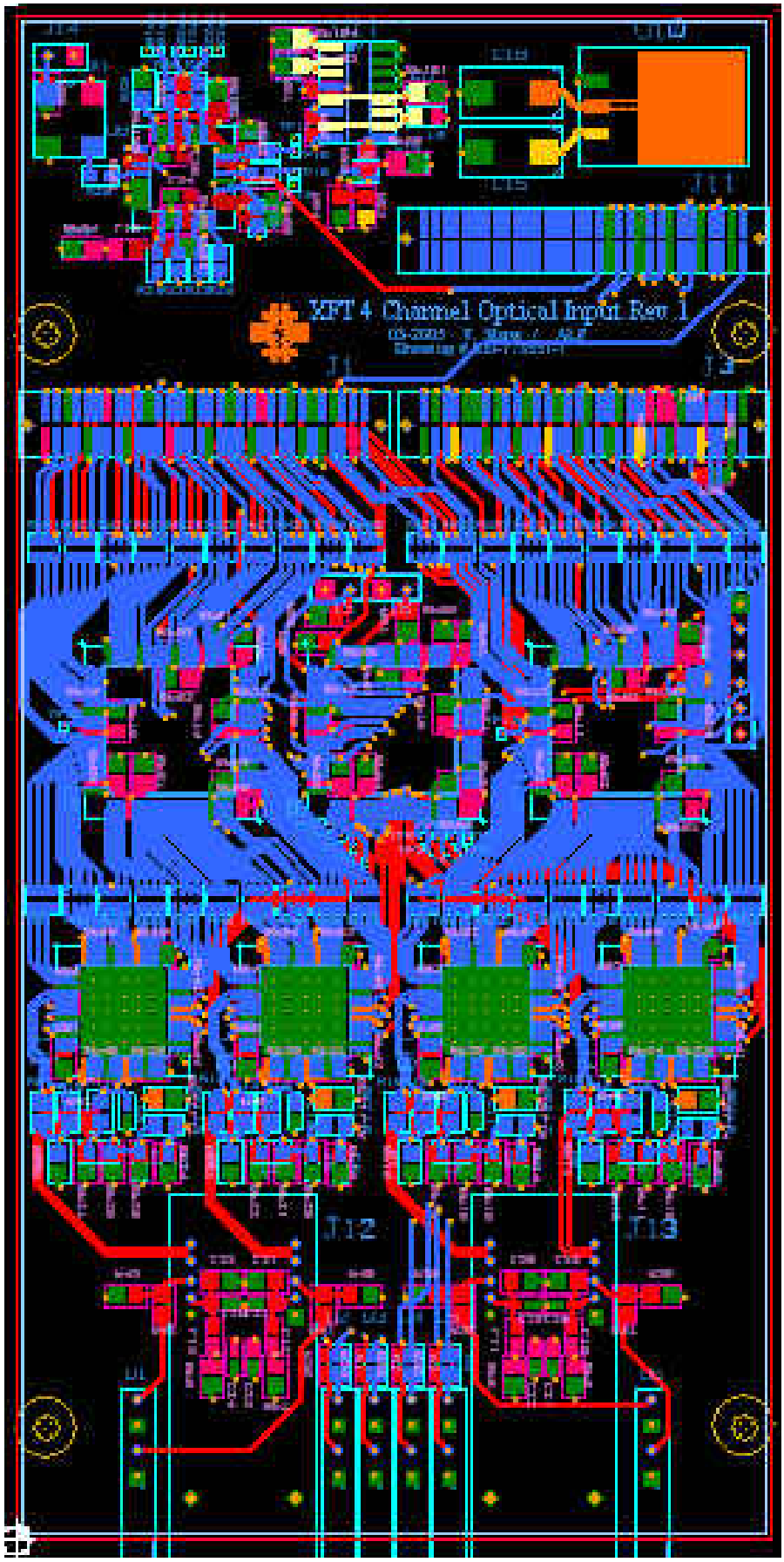
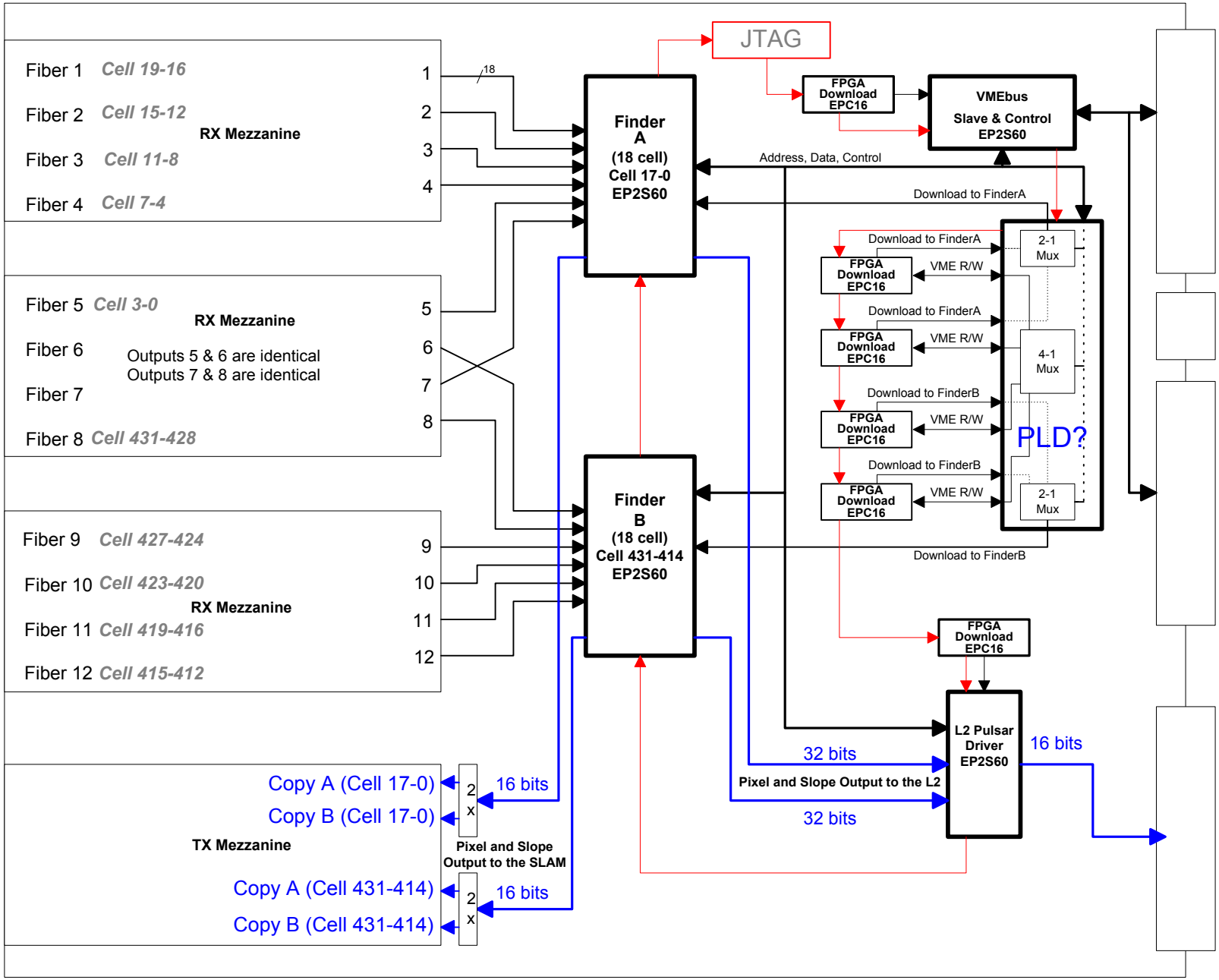
Design changes proposed for Production version of Stereo_XFT_Finder

- New 18-cell Finder FPGAs
- Pixel Driver FPGA no longer needed
- New RX_Mezz reduces need of 2.5V plane under Finder FPGAs ->16 layer board goes to 14 layers
- Get rid of current TX_Mezz and put logic on board to drive 3 copies of each 18-cell pixel output -> gets rid of optical cable splitters
- LED front panel space freed up by moving LEDs to RX_Mezz
- JTAG connector on FP

RX_Mezzanine Rev1

- onboard 5V/2.5V DC/DC converter to take load off Pulsar
- 3.3V logic levels will be driven off board rather than 2.5V (cleaner design with respect to Pulsar)
- CPLDs onboard to allow for volatge level translation, buffering/registering data, data path duplication
- More status LEDs


XFT 4 Channel Optical Input Rev 1
J12
J13


JTAG
Fiber 1 Cell 19-16
Fiber 2 Cell 15-12
RX Mezzanine
Fiber 3 Cell 11-8
Fiber 4 Cell 7-4
1
2
3
4
18
Finder A (18 cell) Cell 17-0 EP2S60
FPGA Download EPC16
VMEbus Slave & Control EP2S60
Address, Data, Control
Download to FinderA
Fiber 5 Cell 3-0
RX Mezzanine
Fiber 6
Outputs 5 & 6 are identical
Outputs 7 & 8 are identical
Fiber 7
Fiber 8 Cell 431-428
5
6
7
8
Download to FinderA
FPGA Download EPC16
VME R/W
2-1 Mux
4-1 Mux
Download to FinderB
PLD?
Finder B (18 cell) Cell 431-414 EP2S60
Fiber 9 Cell 427-424
Fiber 10 Cell 423-420
RX Mezzanine
Fiber 11 Cell 419-416
Fiber 12 Cell 415-412
9
10
11
12
L2 Pulsar Driver EP2S60
32 bits
16 bits
Pixel and Slope Output to the L2
Copy A (Cell 17-0)
Copy B (Cell 17-0)
TX Mezzanine
2 x
Pixel and Slope Output to the SLAM
Copy A (Cell 431-414)
Copy B (Cell 431-414)

FIBER MAPPING to Finder Board

5 Finder FPGA's

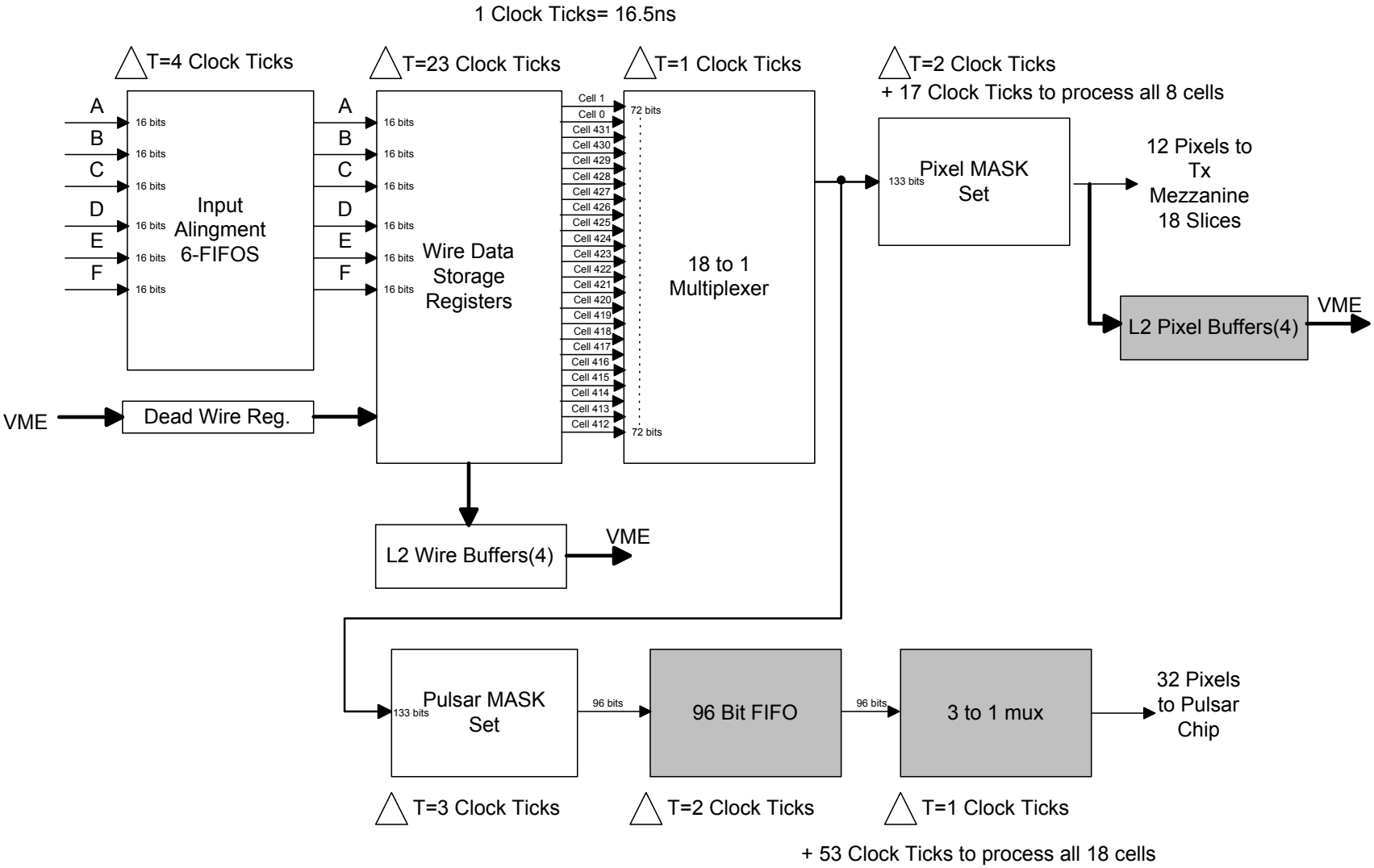
Finder A
X1 - Cell 19, 18, 17, 16
Y1 - Cell 15, 14, 13, 12
Z1 - Cell 11, 10, 9, 8
Finder B
Z1 - Cell 11, 10, 9, 8
X2 - Cell 7, 6, 5, 4
Y2 - Cell 3, 2, 1, 0
Finder C
Y2 - Cell 3, 2, 1, 0
Z2 - Cell 431, 430, 429, 428
X3 - Cell 427, 426, 425, 424
Finder D
X3 - Cell 427, 426, 425, 424
Y3 - Cell 423, 422, 421, 420
Z3 - Cell 419, 418, 417, 416
Finder E
Z3 - Cell 419, 418, 417, 416
Y3 - Cell 415, 414, 413, 412

2 Finder FPGA's

FINDER A
X1 - Cell 19, 18, 17, 16
Y1 - Cell 15, 14, 13, 12
Z1 - Cell 11, 10, 9, 8
X2 - Cell 7, 6, 5, 4
Y2 - Cell 3, 2, 1, 0
Z2 - Cell 431, 430, 429, 428
FINDER B
Y2 - Cell 3, 2, 1, 0
Z2 - Cell 431, 430, 429, 428
X3 - Cell 427, 426, 425, 424
Y3 - Cell 423, 422, 421, 420
Z3 - Cell 419, 418, 417, 416
Y3 - Cell 415, 414, 413, 412

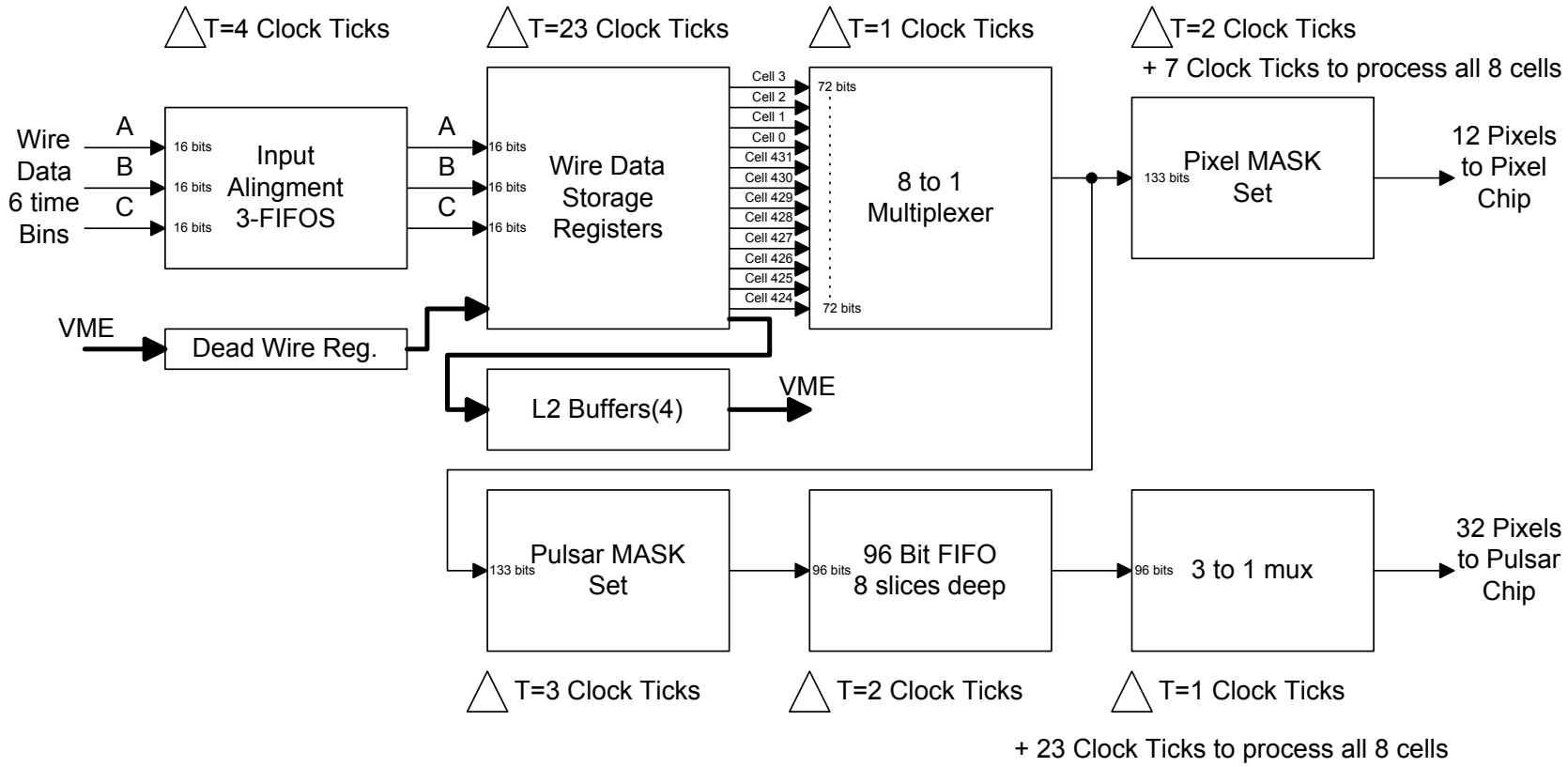
Core cells in blue, neighbors in black

Finder V2 CHIP BLOCK



Finder V1 CHIP BLOCK

1 Clock Ticks= 16.5ns



18 cells vs 8 cells in a Finder Design

- **Advantages:** ROUTING & BOARD COMPLEXITY reduced, COST reduced, TIME savings

- <u>COST</u>
  Saves cost of: 4 EP2S60 devices, 8 EPC16 devices, resistors, capacitors, jumpers, connectors.

- <u>ROUTING & COMPLEXITY</u>
- Removes or reduce nets routing:
- 10 bit Address lines bussed to 4 devices
- 21 bit Address lines bussed to 8 devices
- 48 Control nets less from VME Slave
- 32 bit Data bus lines bussed to 4 devices
- 16 bit Data bus lines bussed to 8 devices
- 3 – 32 bit busses to L2 Pulsar
- 5 – 32 bit busses to Pixel Chip
- 36 nets x 4 devices for configuration
- 4 – 18 bit input data that is shared between Finders
- Reduces clock nets to 4 FPGA's.

- <u>TIME</u>
  Saves the Alignment of pixels coming from the different Finder chips, this is done in the Finder as the pixels are found. This saves 3 clock -16ns clock ticks in timing diagram.

- **Disadvantage:**
- 86 more pins used per Finder(2 more Fibers).
- Multiplexing scheme will be different in the two Finders(same number but with a different order – different design).

- **2 Finder Chips(V2) w/o Pixel chip per Board - Stereo Finder FPGA Design – Report File**

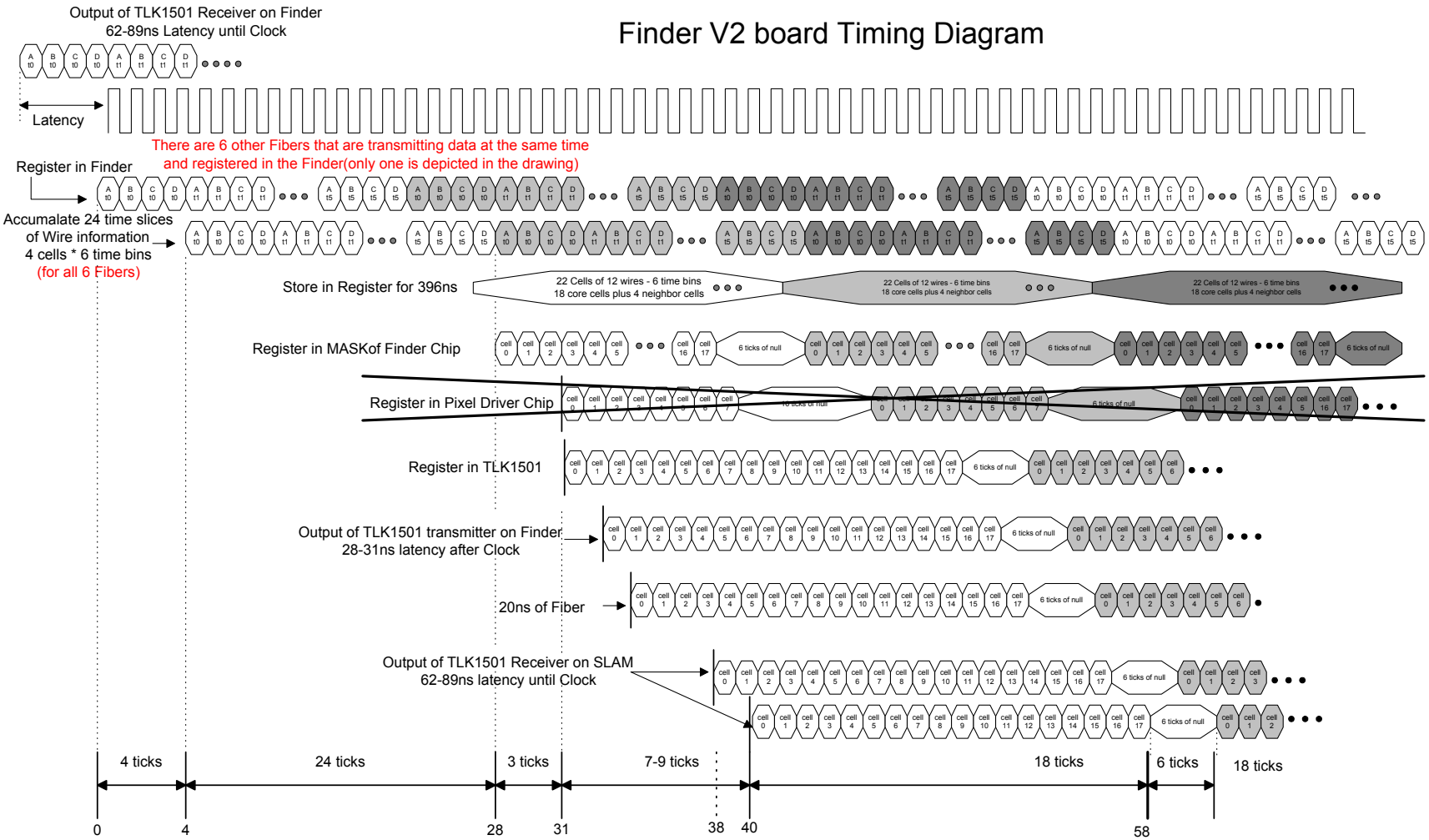
  Design has everything except L2 buffer for Segment and L2-Pulsar Multiplexing

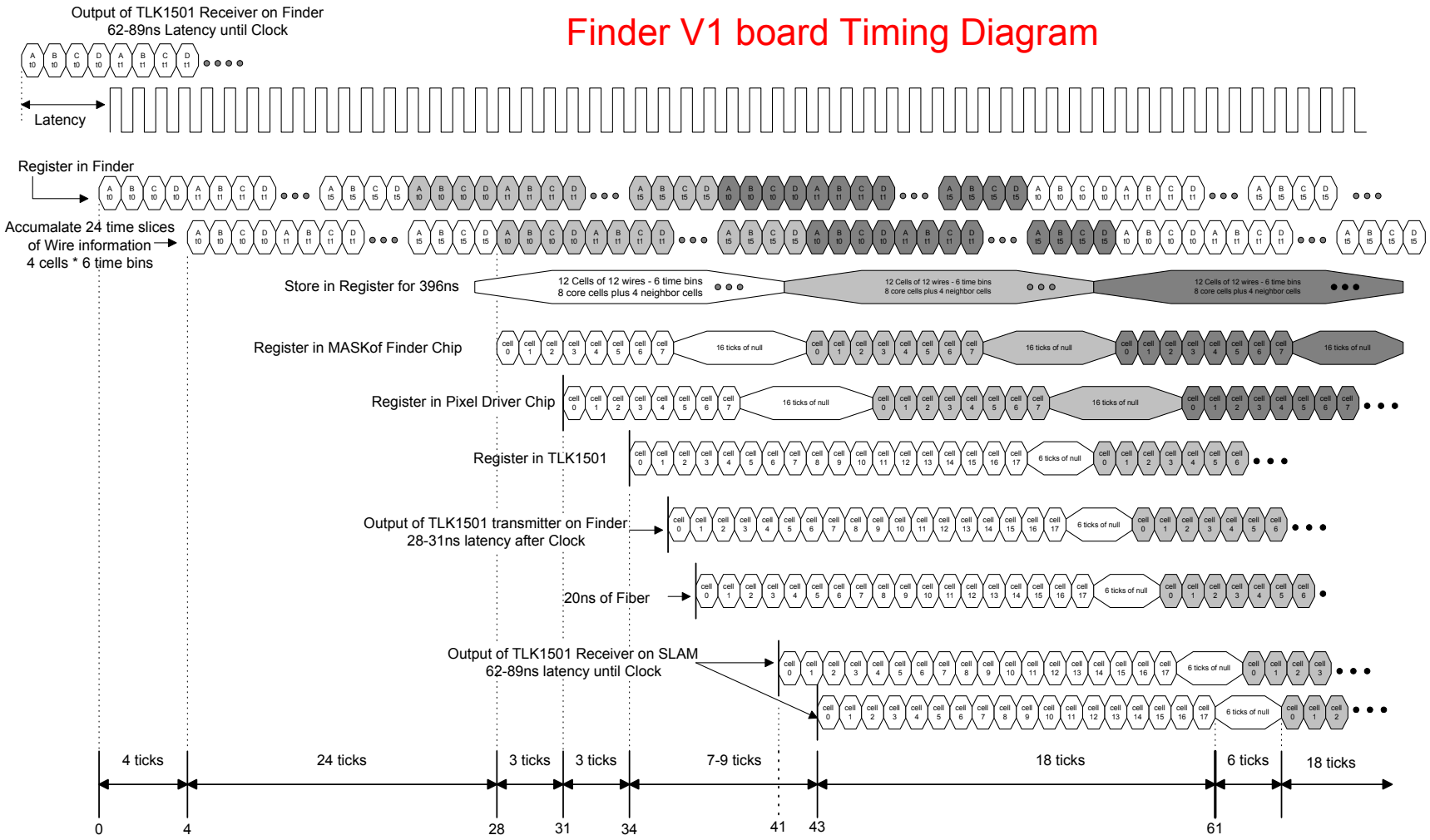
```
+-----------------------------------------------------------------+
; Fitter Summary                                                  ;
+-------------------------+---------------------------------------+
; Fitter Status           ; Successful - Thu Mar 24 14:09:06 2005  ;
; Quartus II Version      ; 4.2 Build 157 12/07/2004 SJ Full Version ;
; Revision Name           ; top_level                             ;
; Top-level Entity Name   ; top_level                             ;
; Family                  ; Stratix II                            ;
; Device                  ; EP2S60F484C5ES                        ;
; Timing Models           ; Preliminary                           ;
; Total ALUTs             ; 17,534 / 48,352 ( 36 % )              ;
; Total pins              ; 281 / 335 ( 83 % )                    ;
; Total virtual pins      ; 0                                     ;
; Total memory bits       ; 111,168 / 2,544,192 ( 4 % )           ;
; DSP block 9-bit elements ; 0 / 288 ( 0 % )                      ;
; Total PLLs              ; 1 / 6 ( 16 % )                        ;
; Total DLLs              ; 0 / 2 ( 0 % )                         ;
+-------------------------+---------------------------------------+
```

- **5 Finder Chips(V1) and Pixel Chip per Board – Stereo Finder FPGA Design – Report File**

```
+-----------------------------------------------------------------+
; Fitter Summary                                                  ;
+-------------------------+---------------------------------------+
; Fitter Status           ; Successful - Fri Feb 04 11:16:39 2005  ;
; Quartus II Version      ; 4.2 Build 157 12/07/2004 SJ Full Version ;
; Revision Name           ; top_level                             ;
; Top-level Entity Name   ; top_level                             ;
; Family                  ; Stratix II                            ;
; Device                  ; EP2S60F484C5ES                        ;
; Timing Models           ; Preliminary                           ;
; Total ALUTs             ; 14,266 / 48,352 ( 29 % )              ;
; Total pins              ; 195 / 335 ( 58 % )                    ;
; Total virtual pins      ; 0                                     ;
; Total memory bits       ; 79,744 / 2,544,192 ( 3 % )            ;
; DSP block 9-bit elements; 0 / 288 ( 0 % )                       ;
; Total PLLs              ; 1 / 6 ( 16 % )                        ;
; Total DLLs              ; 0 / 2 ( 0 % )                         ;
+-------------------------+---------------------------------------+
```

Finder V2 board Timing Diagram



Timing decreases by 3 ticks becuase pixel data isn't sent to the Pixel chip where it is registered and aligned(already done in the Finder)

Finder V1 board Timing Diagram