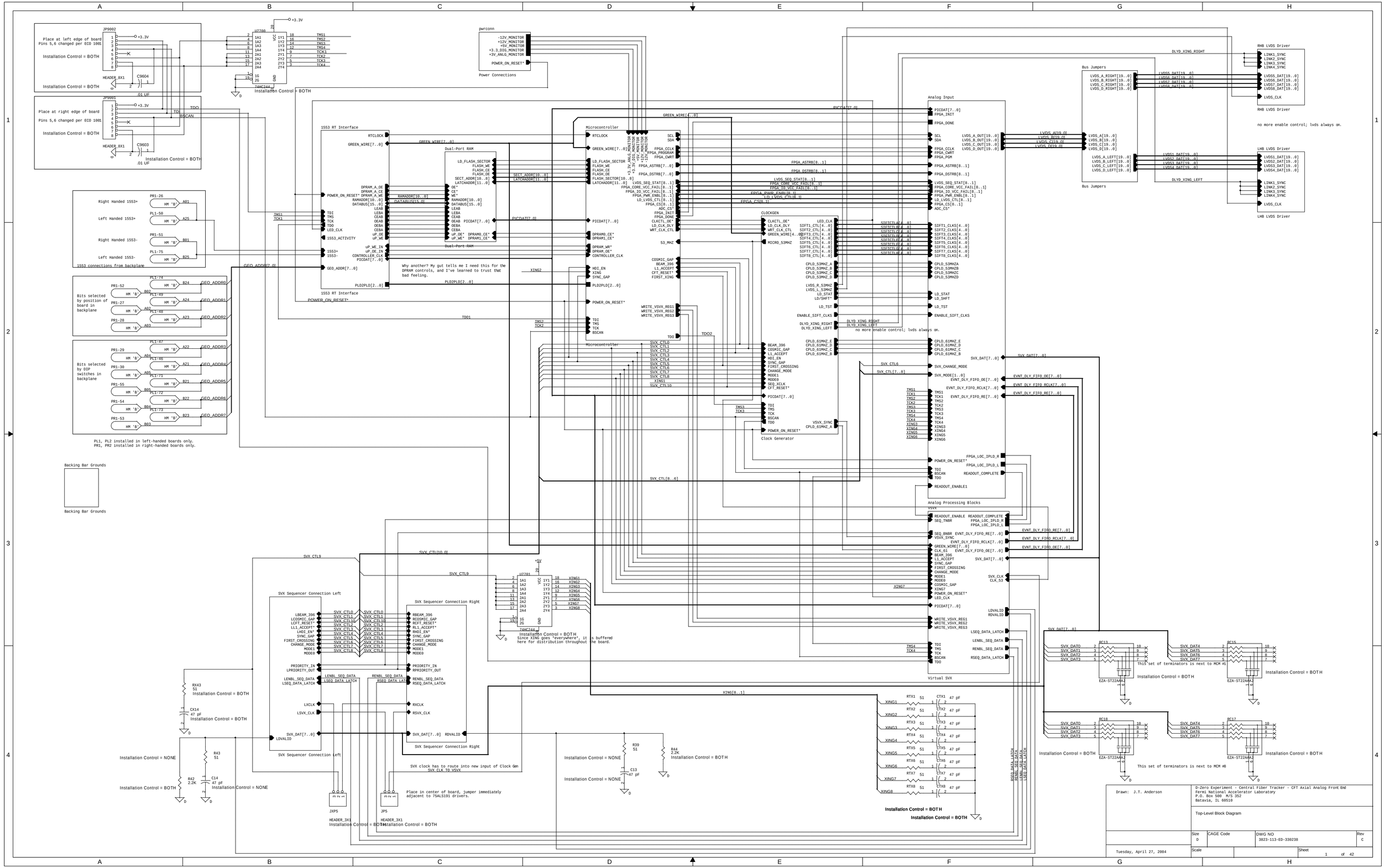
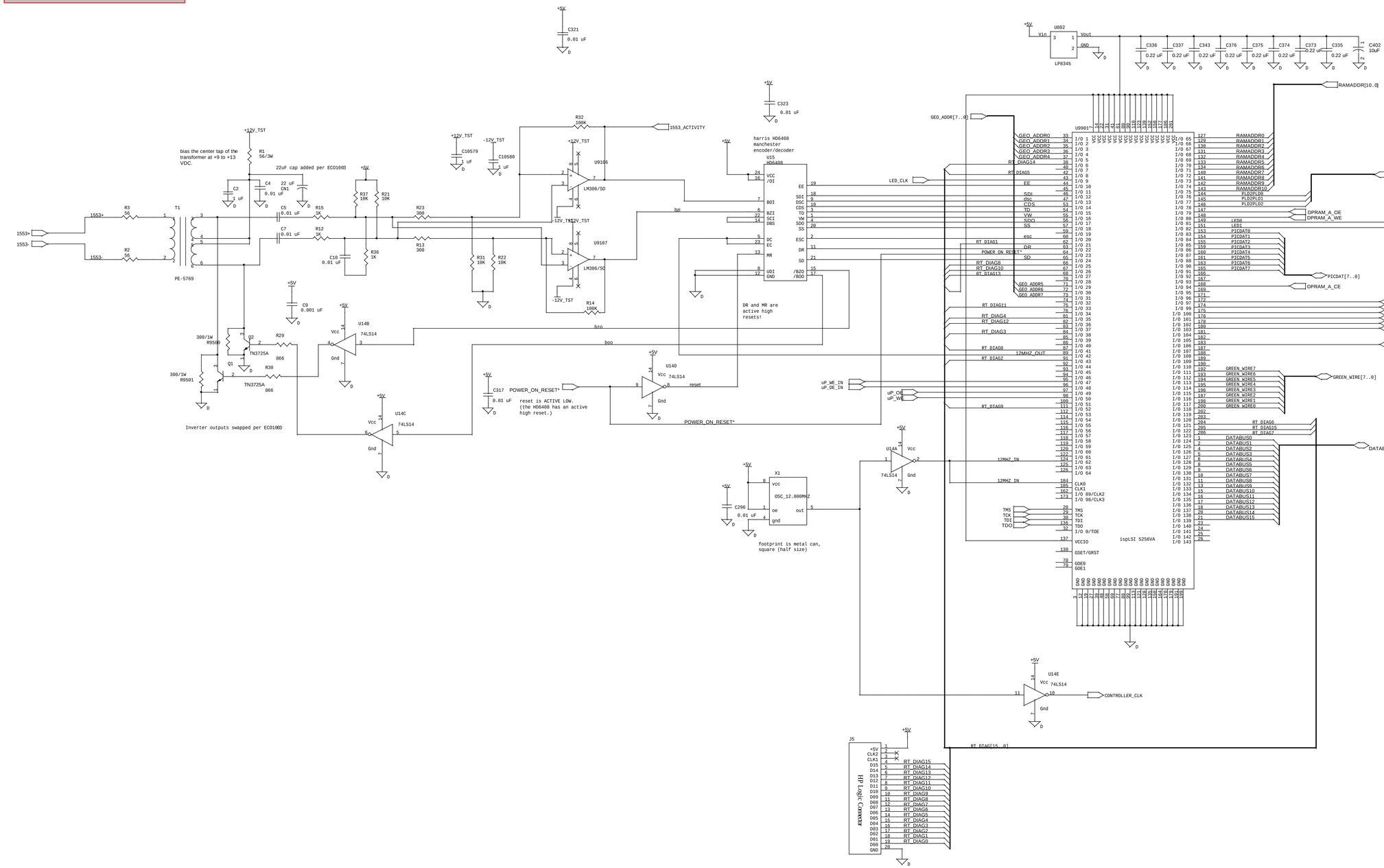

JP9002
Place at left edge of board
Pins 5,6 changed per ECO 1001
Installation Control = BOTH
HEADER_8X1
C9604
.01 UF
JP9001
Place at right edge of board
Pins 5,6 changed per ECO 1001
C9603
U7780
74HC244
Installation Control = BOTH
pwrconn
Power Connections
1553 RT Interface
Dual-Port RAM
Microcontroller
CLOCKGEN
Clock Generator
Analog Input
Analog Processing Blocks
Virtual SVX
Bus Jumpers
RHB LVDS Driver
LHB LVDS Driver
no more enable control; lvds always on.
Right Handed 1553+
Left Handed 1553+
Right Handed 1553-
Left Handed 1553-
1553 connections from backplane
Bits selected by position of board in backplane
Bits selected by DIP switches in backplane
PL1, PL2 installed in left-handed boards only.
PR1, PR2 installed in right-handed boards only.
Backing Bar Grounds
SVX Sequencer Connection Left
SVX Sequencer Connection Right
Why another? My gut tells me I need this for the DPRAM controls, and I've learned to trust that bad feeling.
U7781
Since XING goes "everywhere", it is buffered here for distribution throughout the board.
SVX clock has to route into new input of Clock Gen SVX_CLK_TO_VSVX
Place in center of board, jumper immediately adjacent to 75ALS191 drivers.
JXP5
JP5
This set of terminators is next to MCM #1
This set of terminators is next to MCM #8
EZA-ST22AA4J
Installation Control = NONE
Installation Control = BOTH
Drawn: J.T. Anderson
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Top-Level Block Diagram
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Tuesday, April 27, 2004
Scale
Sheet 1 of 42

All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1



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Batavia, IL 60510

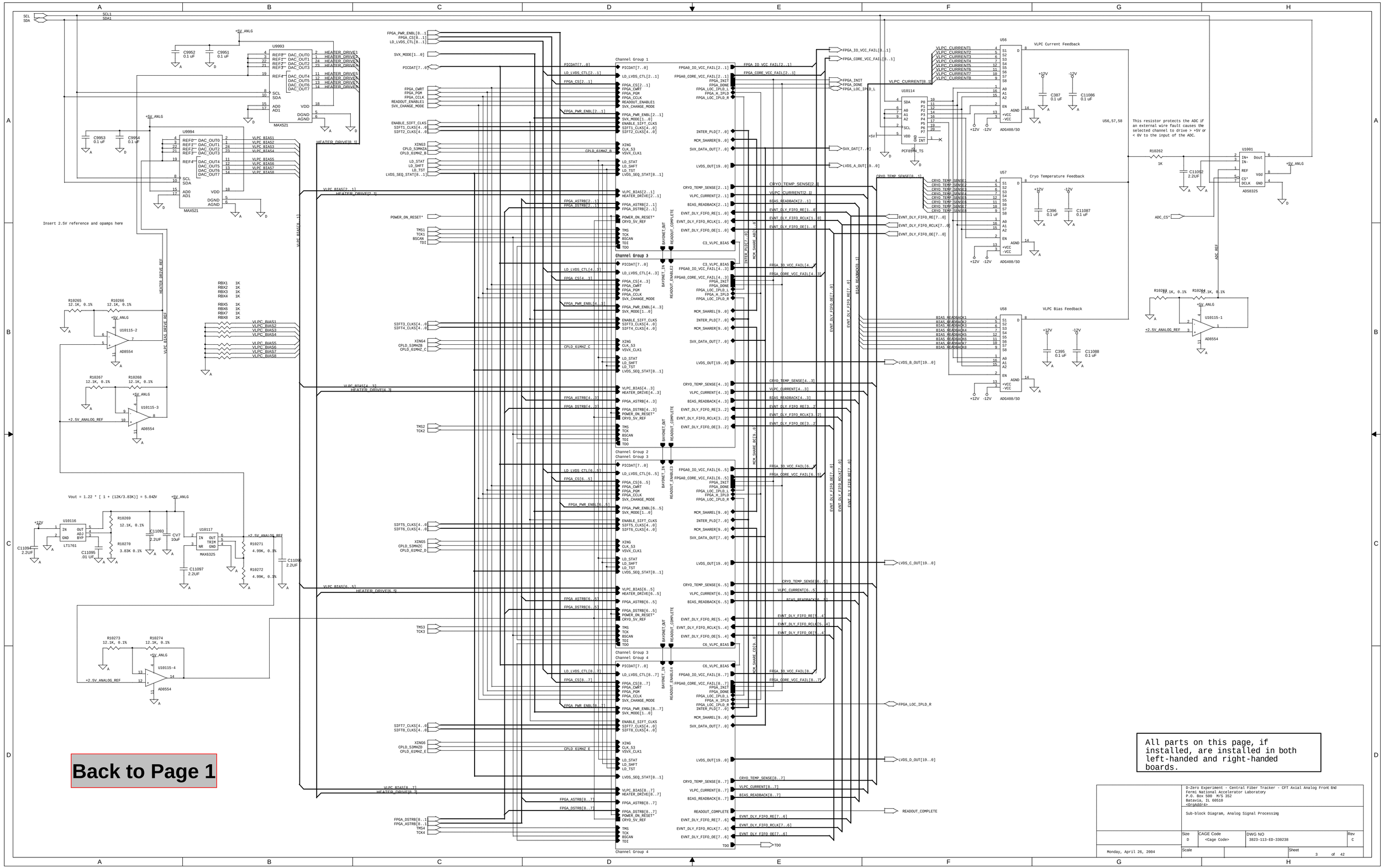
1553 Interface / Remote Terminal

Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Tuesday, April 27, 2004

Scale

Sheet 2 of 42



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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<OrgAddr4>

Sub-block Diagram, Analog Signal Processing

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

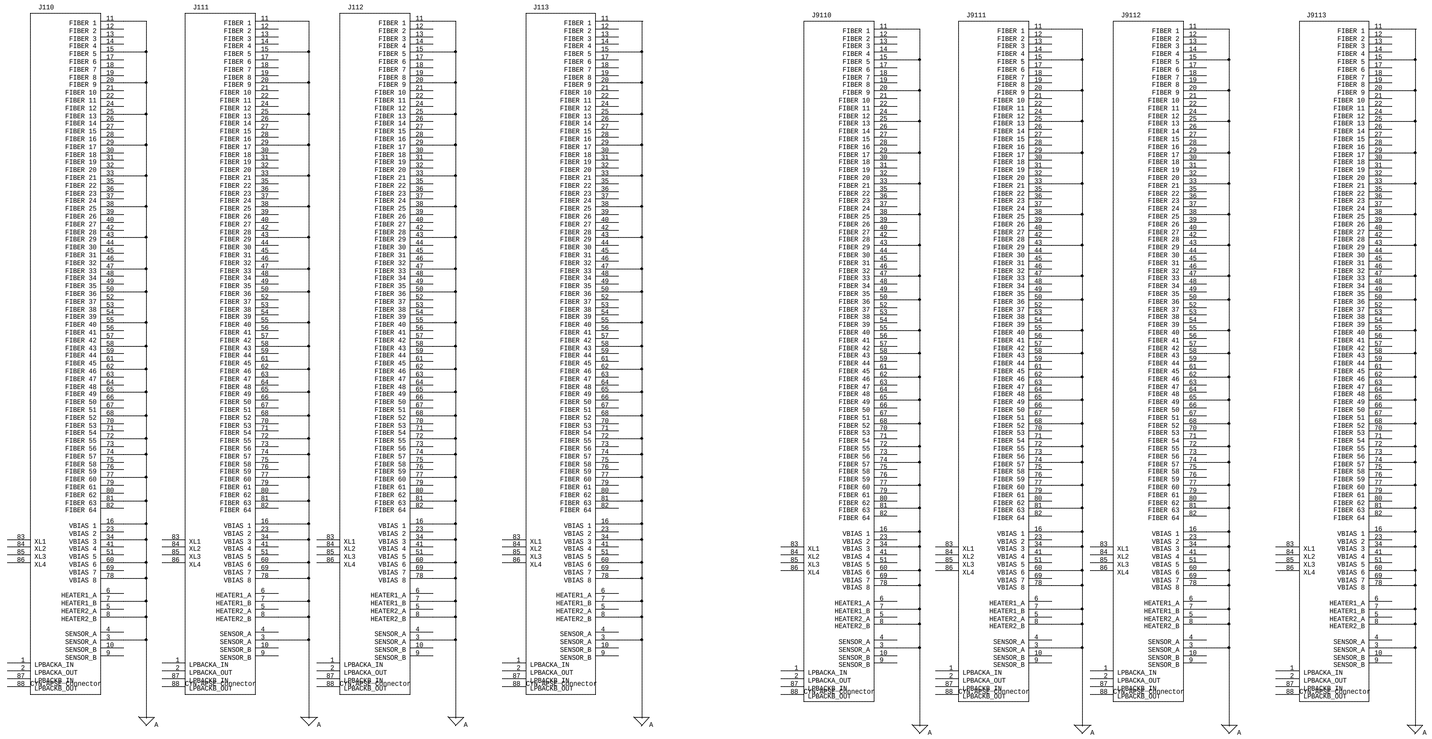
Monday, April 26, 2004

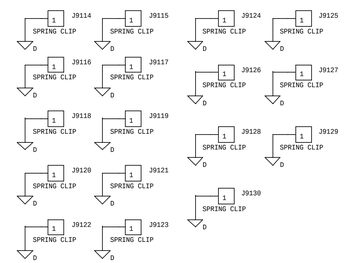
Scale

Sheet 3 of 42

Back to Page 1

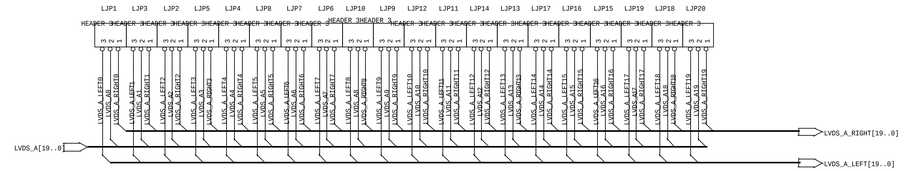
Grounding connections for backing bar. Tie all pins together using TOP SIDE TRACES ONLY. Connect trace sets to AGND using vias at each end of connector only. Do not put any vias inside connector body or along long edges, so as to minimally obstruct charge signals passing underneath.



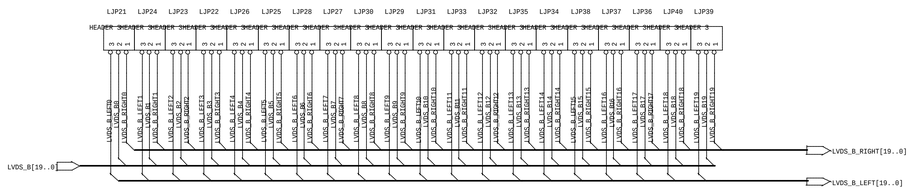


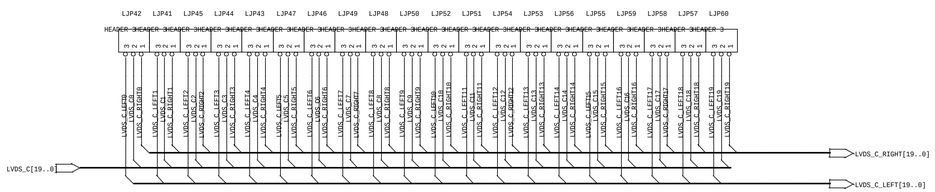
No installable parts on this page; all components are bare-board copper features only.

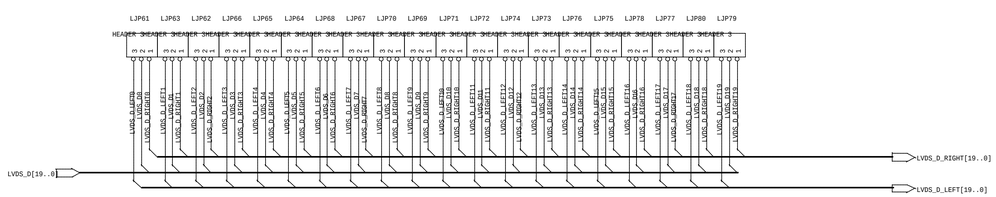
	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <DrgAddr4>		
	Grounding patterns for backing bar		
	Size D	CAGE Code <Cage Code>	DWG NO 3823-113-ED-330238	Rev C
Monday, April 26, 2004	Scale		Sheet 4 of 42



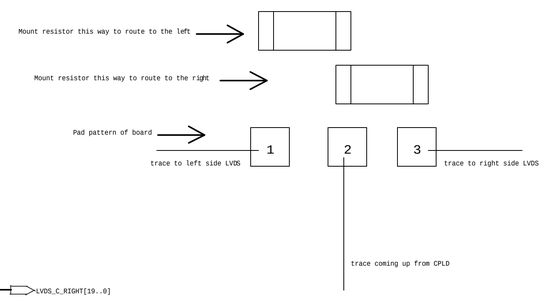
Back to Page 1







Blowup sketch of how this works



All jumpers are actually 3-pin pad arrays designed to allow installation of a low-resistance 0402 resistor either between pads 1 and 2 or pads 3 and 4, manually routing all eighty bits of the bus to the left-side LDVS drivers or to the right side LVDS drivers. This break removes the long stubs to the unused side allowing the unused side to be unstuffed and eliminating reflection possibilities.

Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board
Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board	Bill of Materials Item 0/SM/R_0402 External to PC Board

All parts on this page installed in both left-handed and right-handed boards. POSITION OF COMPONENTS VARIES WITH BOARD HANDEDNESS.

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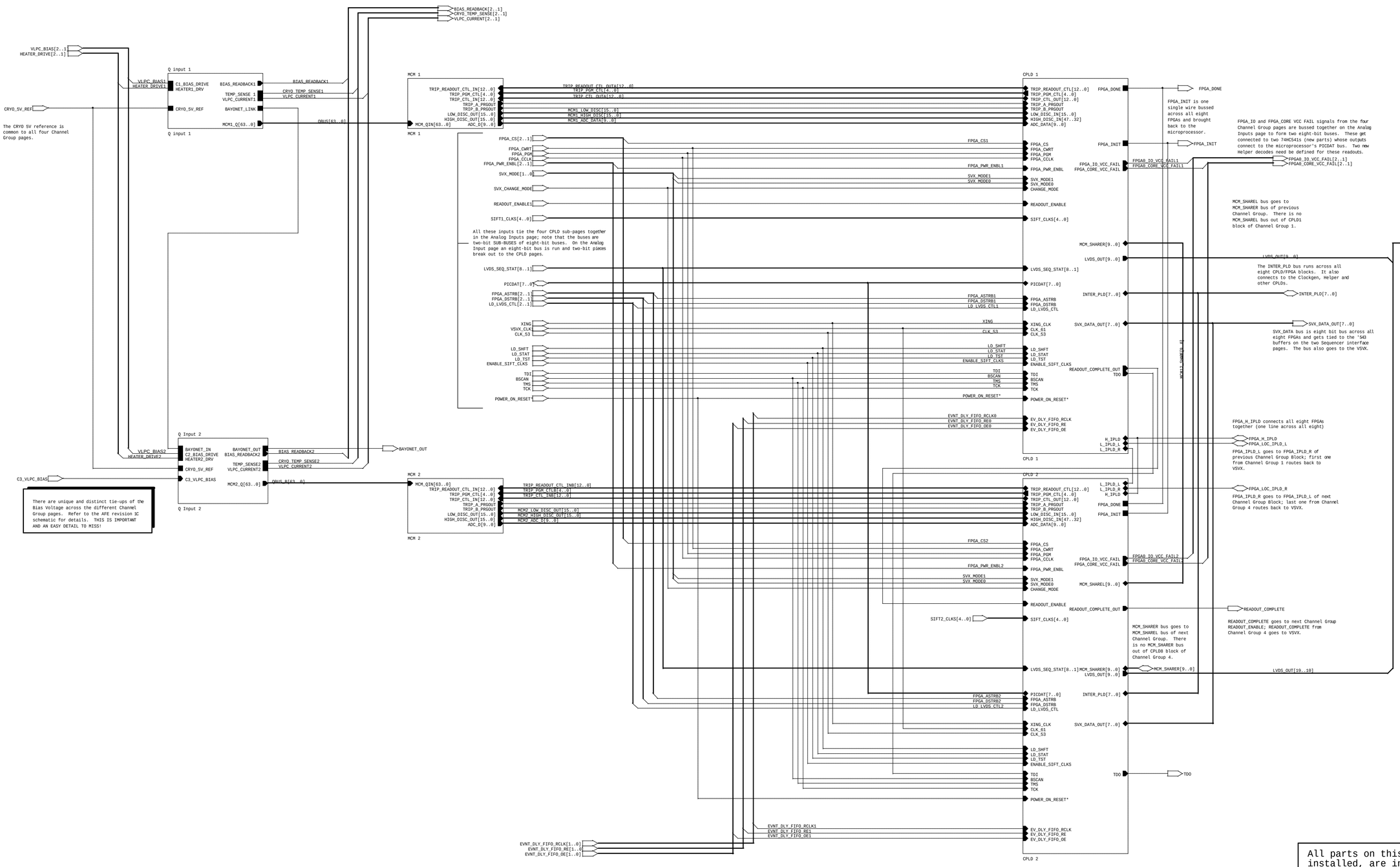
Left/Right bus direction selectors

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

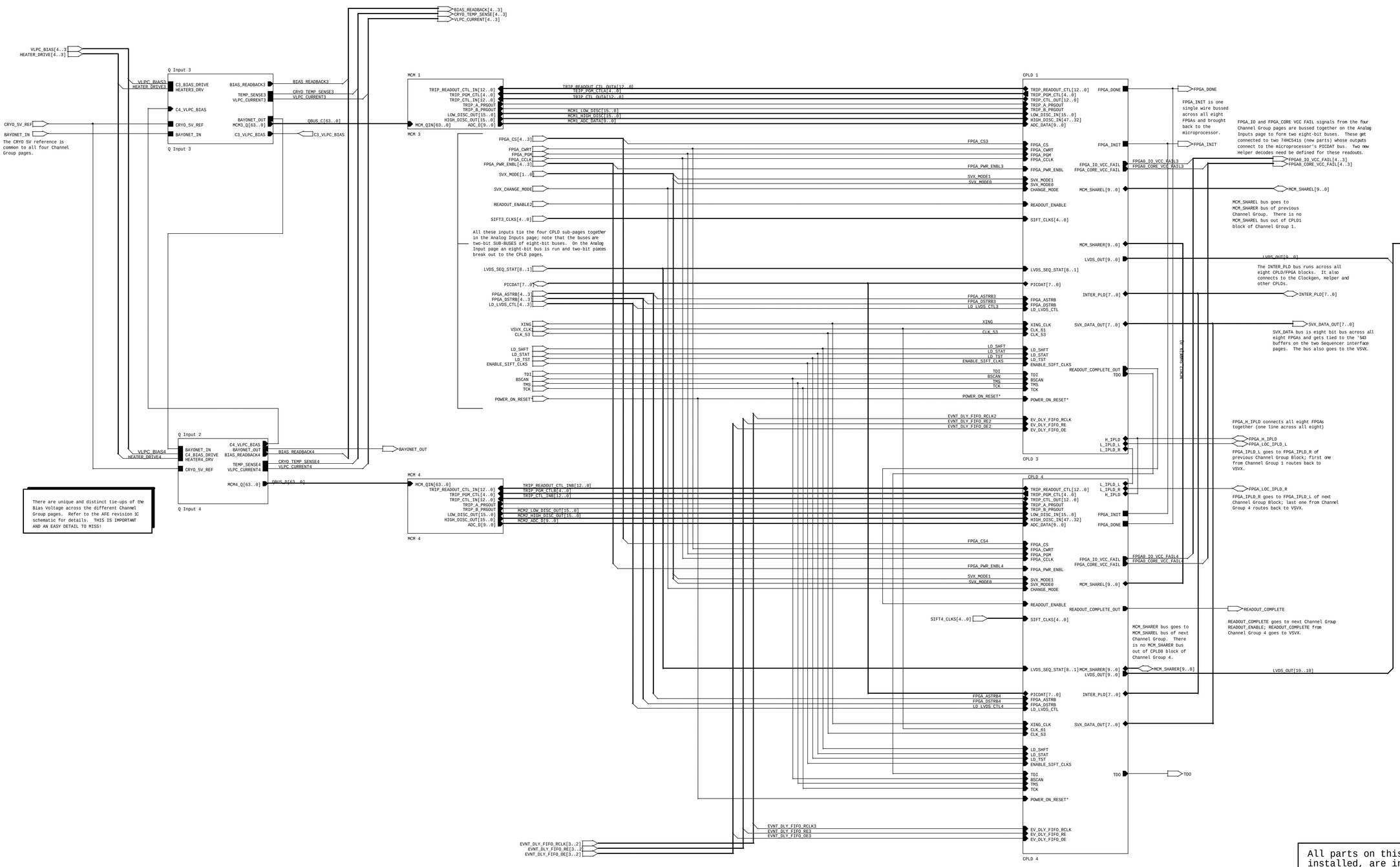
Sheet 5 of 42



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

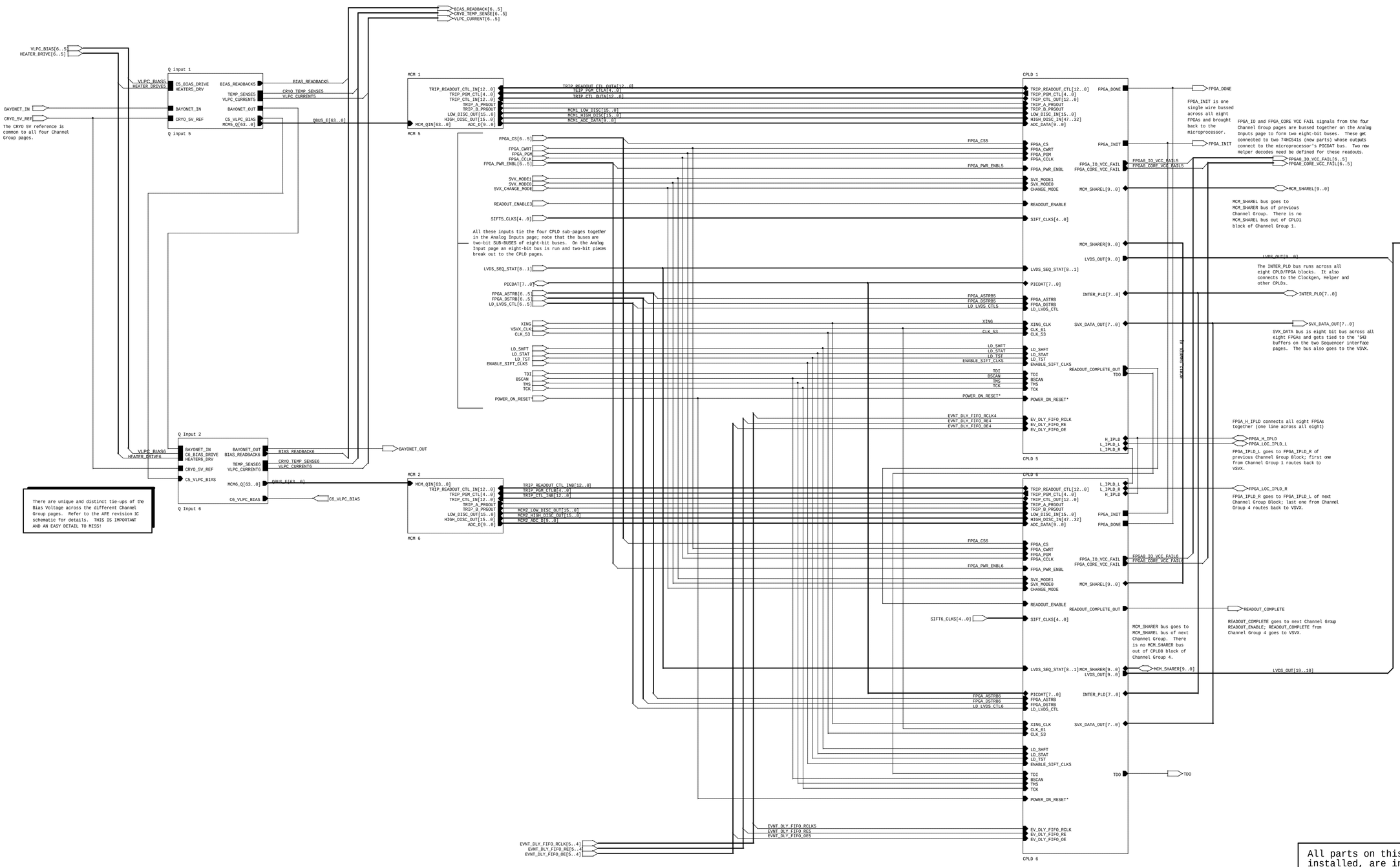
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr4>	
Sub-block Diagram, Qin,MCM,CPLD, #1, #2	
Size: D	CAGE Code: <Cage Code>
DWG NO: 3823-113-ED-330238	Rev: C
Monday, April 26, 2004	Scale
Sheet: 6 of 42	



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510 <OrgAddr4>	
Sub-block Diagram, Qin,MCM,CPLD, #1, #2	
Size: D — CAGE Code: <Cage Code>	DWG NO: 3823-113-ED-330238 — Rev: C
Monday, April 26, 2004	Scale — Sheet: 6 of 42



There are unique and distinct tie-ups of the Bias Voltage across the different Channel Group pages. Refer to the AFE revision 1C schematic for details. THIS IS IMPORTANT AND AN EASY DETAIL TO MISS!

All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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Batavia, IL 60510
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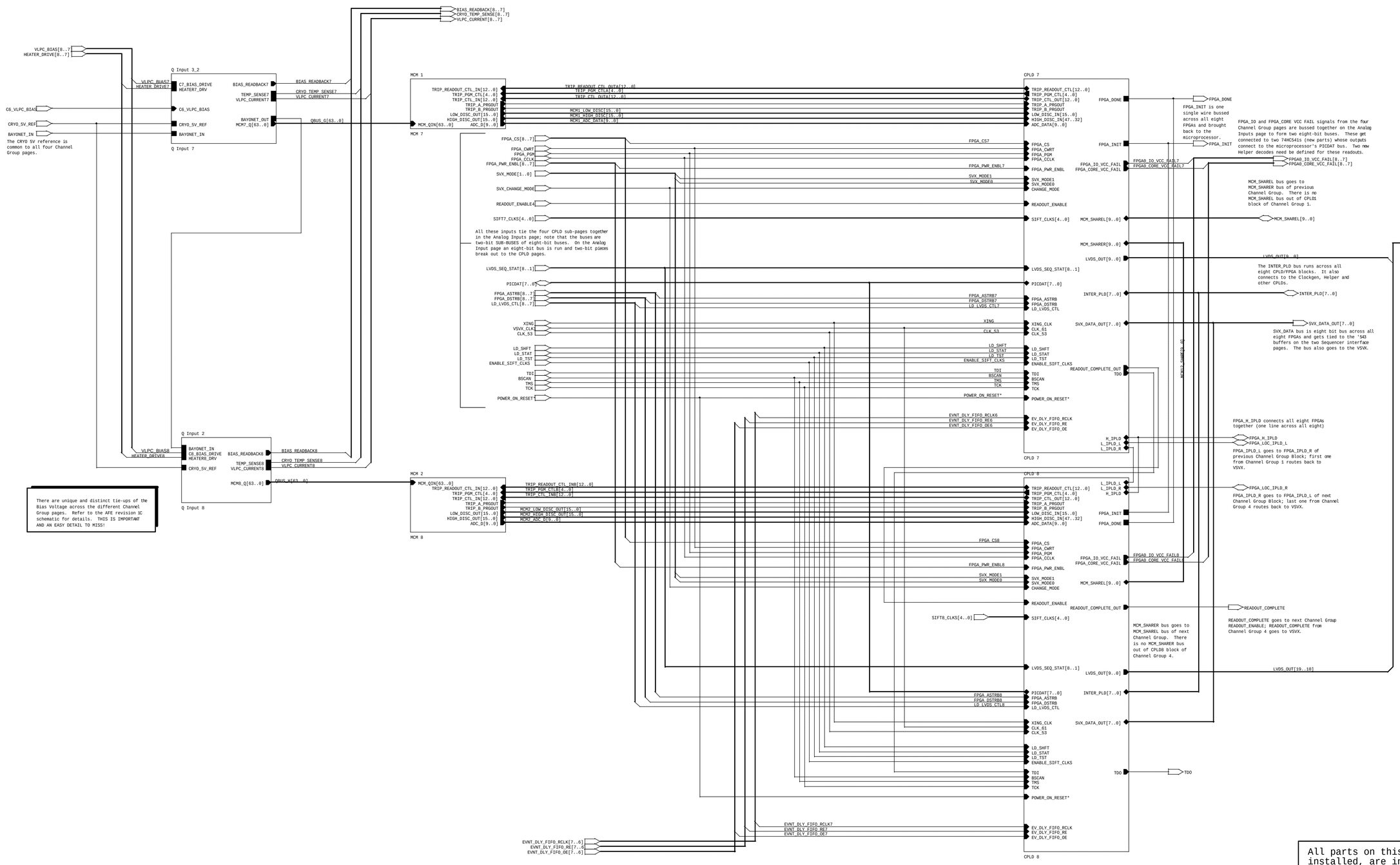
Sub-block Diagram, Qin,MCM,CPLD, #1, #2

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 6 of 42



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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Batavia, IL 60510
<OrgAddr4>

Sub-block Diagram, Qin,MCM,CPLD, #1, #2

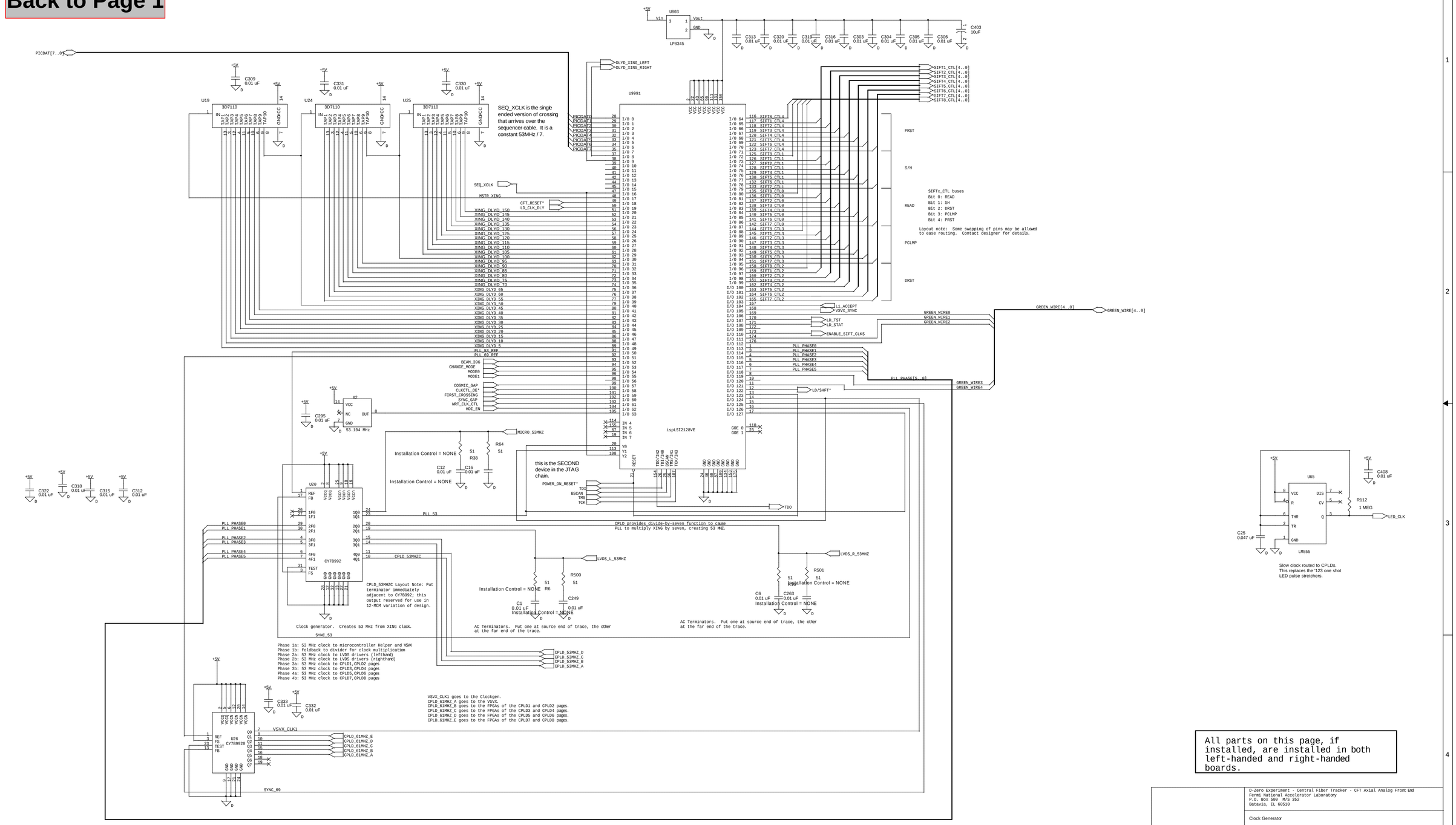
Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 6 of 42

Back to Page 1



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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Batavia, IL 60510

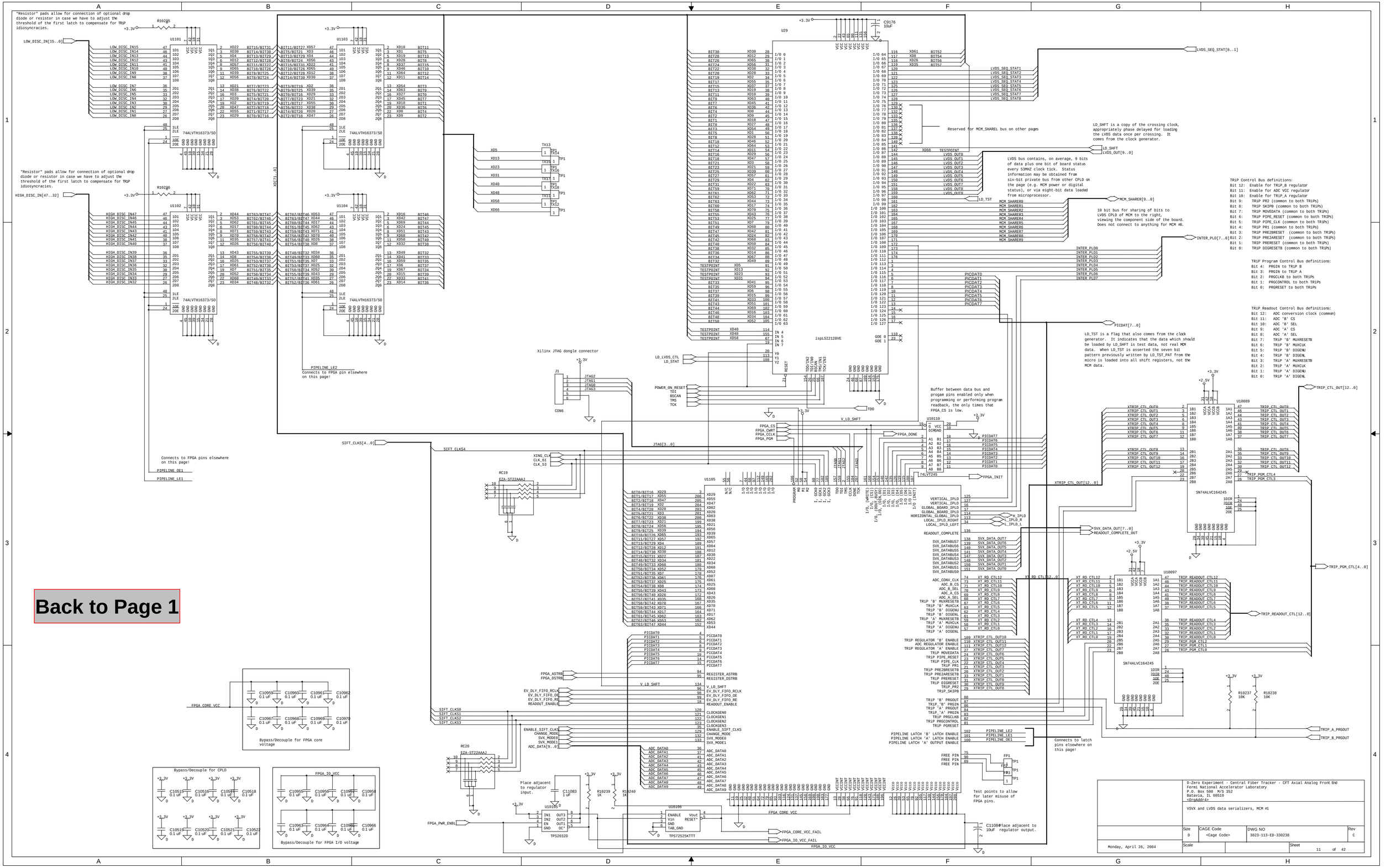
Clock Generator

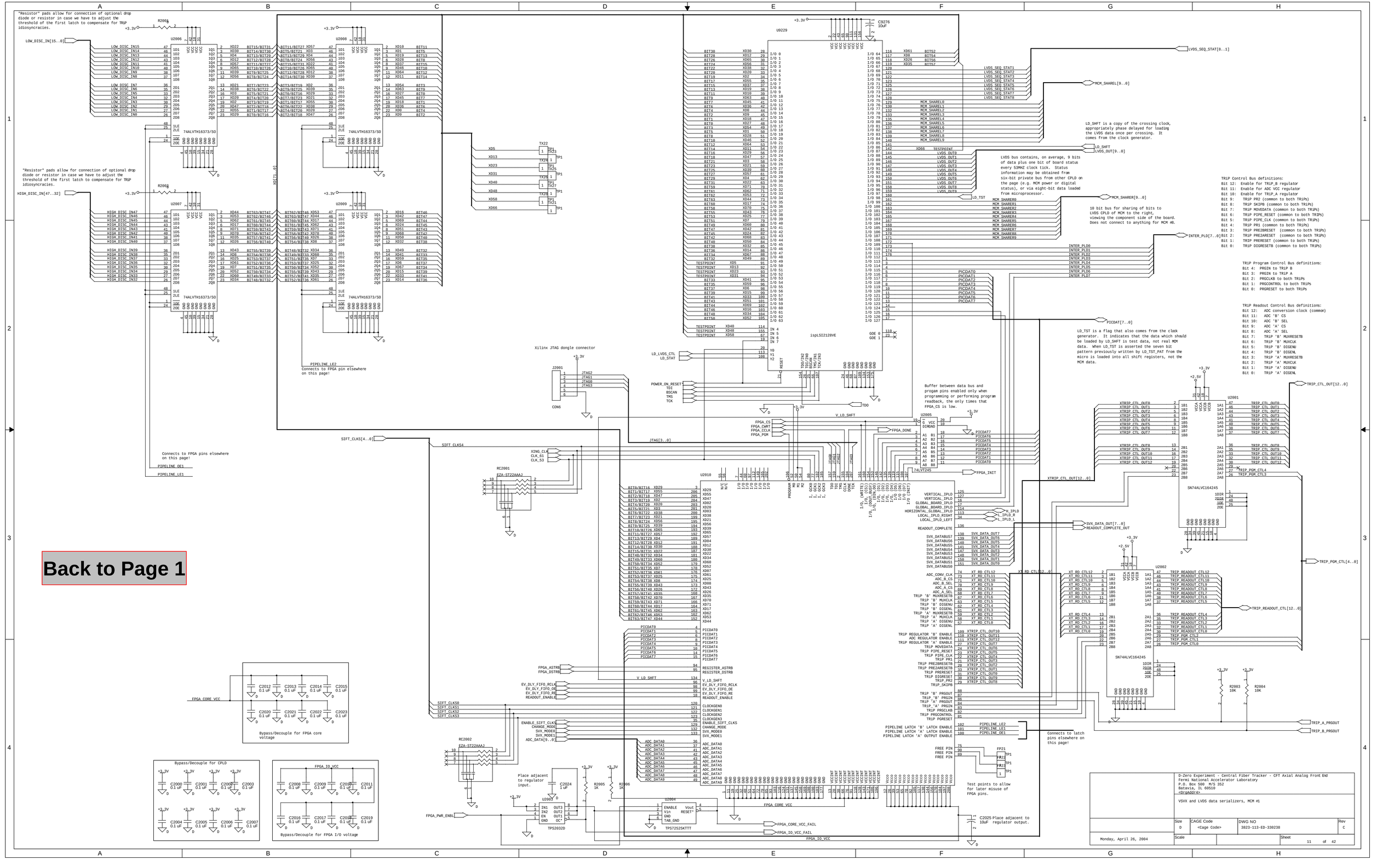
Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

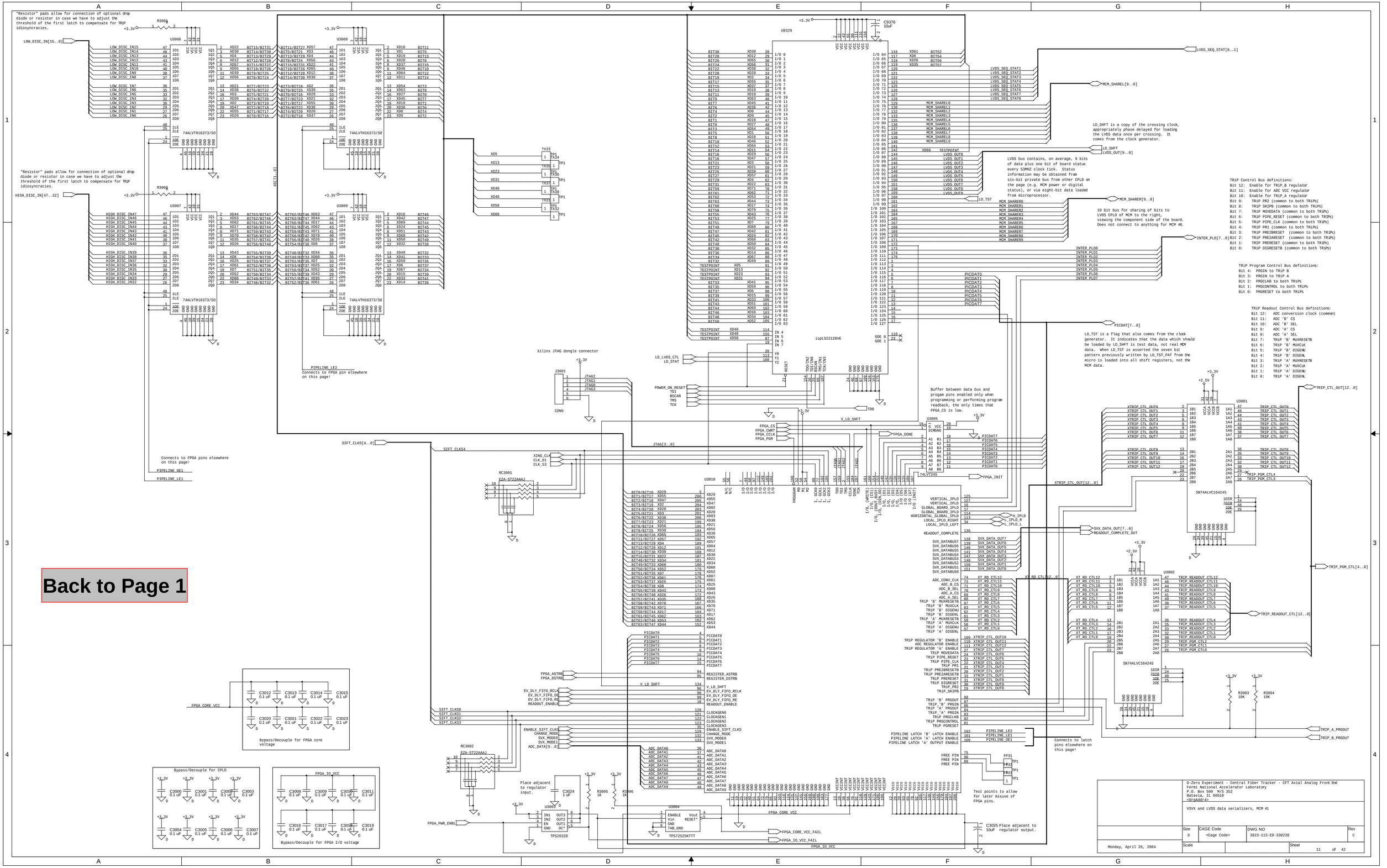
Monday, April 26, 2004

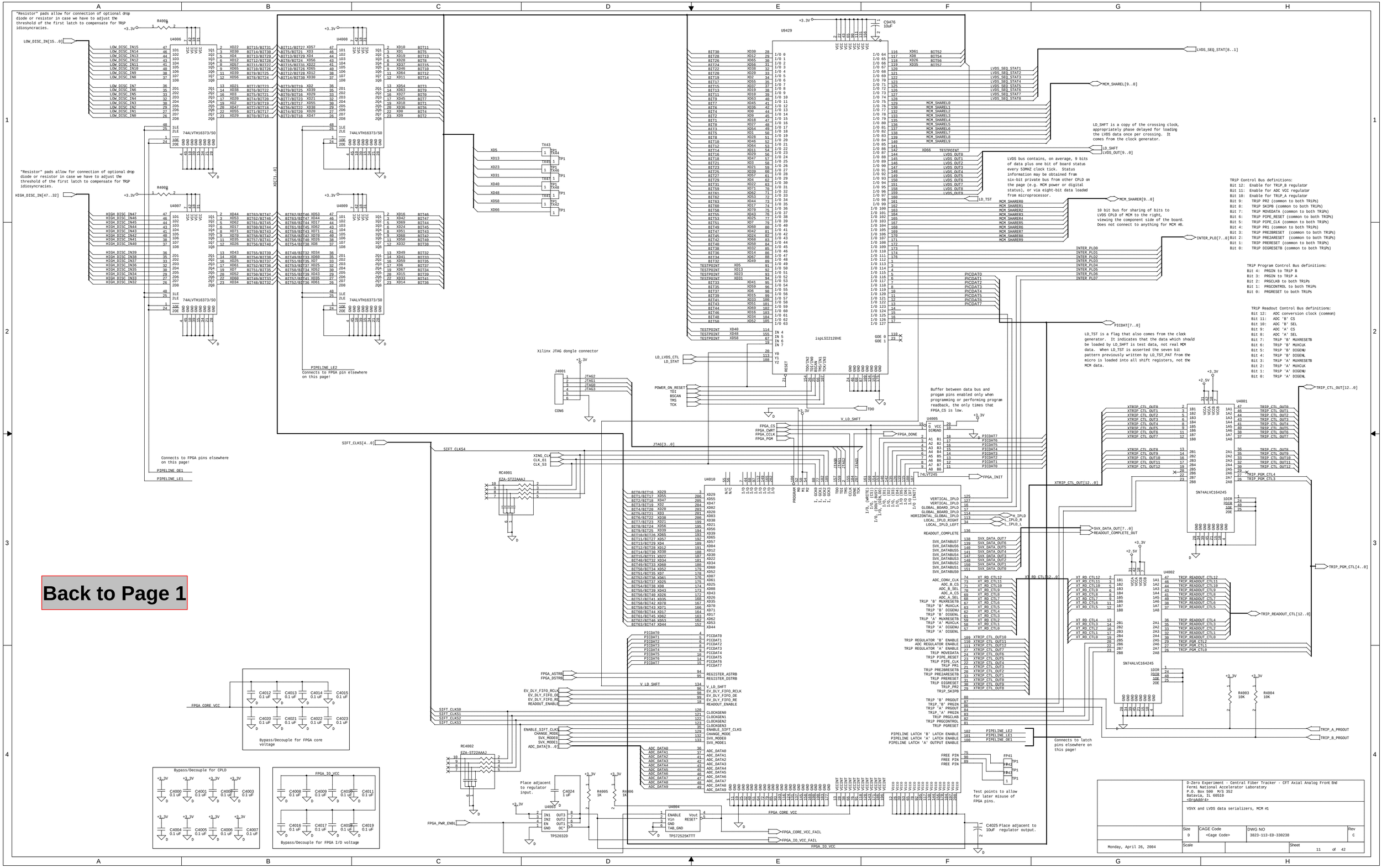
Scale

Sheet 10 of 42

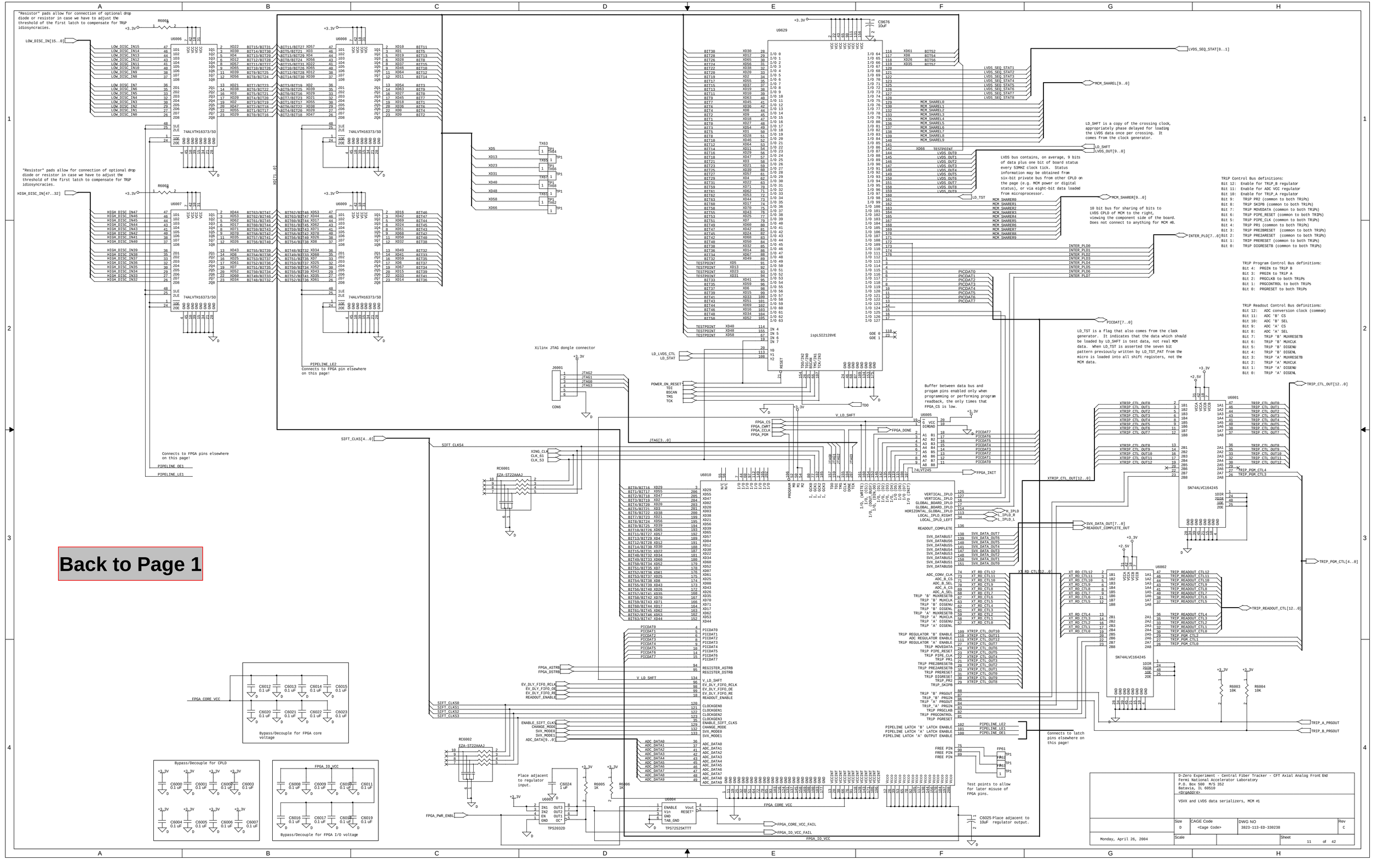

"Resistor" pads allow for connection of optional drop diode or resistor in case we have to adjust the threshold of the first latch to compensate for TRIP idiosyncracies.
LOW_DISC_IN[15..0]
HIGH_DISC_IN[47..32]
U0101
U0102
U0103
U0104
74ALVTH16373/SO
R10225
R10226
XD[71..0]
U29
ispLSI2128VE
C9176 10uF
LVDS_SEQ_STAT[8..1]
Reserved for MCM_SHAREL bus on other pages
LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the clock generator.
LD_SHFT
LVDS_OUT[9..0]
LVDS bus contains, on average, 9 bits of data plus one bit of board status every 53MHZ clock tick. Status information may be obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eight-bit data loaded from microprocessor.
LD_TST
MCM_SHAREB[9..0]
10 bit bus for sharing of bits to LVDS CPLD of MCM 1 when viewing the component side of the board. Does not connect to anything for MCM #8.
INTER_PLD[7..0]
TRIP Control Bus definitions:
Bit 12: Enable for TRIP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRIP_A regulator
Bit 9: TRIP PR2 (common to both TRIPs)
Bit 8: TRIP SKIPB (common to both TRIPs)
Bit 7: TRIP MOVEDATA (common to both TRIPs)
Bit 6: TRIP PIPE_RESET (common to both TRIPs)
Bit 5: TRIP PIPE_CLK (common to both TRIPs)
Bit 4: TRIP PR0 (common to both TRIPs)
Bit 3: TRIP PREZBRESET (common to both TRIPs)
Bit 2: TRIP PREZARESET (common to both TRIPs)
Bit 1: TRIP PRERESET (common to both TRIPs)
Bit 0: TRIP DIGRESETB (common to both TRIPs)
TRIP Program Control Bus definitions:
Bit 4: PRGIN to TRIP B
Bit 3: PRGIN to TRIP A
Bit 2: PRGCLKB to both TRIPs
Bit 1: PRGCONTROL to both TRIPs
Bit 0: PRGRESET to both TRIPs
PICDAT[7..0]
LD_TST is a flag that also comes from the clock generator. It indicates that the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is asserted the seven bit pattern previously written by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.
TRIP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRIP 'B' MUXRESETB
Bit 6: TRIP 'B' MUXCLK
Bit 5: TRIP 'B' DIGENJ
Bit 4: TRIP 'B' DIGEN.
Bit 3: TRIP 'A' MUXRESETB
Bit 2: TRIP 'A' MUXCLK
Bit 1: TRIP 'A' DIGENJ
Bit 0: TRIP 'A' DIGEN.
TRIP_CTL_OUT[12..0]
U10089
SN74ALVC164245
XTRIP_CTL_OUT12..0]
TRIP_PGM_CTL[4..0]
U10097
XT_RD_CTL[12..0]
TRIP_READOUT_CTL[12..0]
Xilinx JTAG dongle connector
J1
CON6
JTAG[3..0]
LD_LVDS_CTL
LD_STAT
POWER_ON_RESET
TDI
BSCAN
TMS
TCK
TDO
V_LD_SHFT
U10110
74LVT245
FPGA_DONE
FPGA_INIT
FPGA_CS
FPGA_CWRT
FPGA_CCLK
FPGA_PGM
PIPELINE_LE2
Connects to FPGA pin elsewhere on this page!
Connects to FPGA pins elsewhere on this page!
PIPELINE_OE1
PIPELINE_LE1
SIFT_CLKS[4..0]
SIFT_CLKS4
XING_CLK
CLK_61
CLK_53
RC19
EZA-ST22AAAJ
U0105
U0106
RC20
FPGA_ASTRB
FPGA_DSTRB
EV_DLY_FIFO_RCLK
EV_DLY_FIFO_OE
EV_DLY_FIFO_RE
READOUT_ENABLE
SIFT_CLKS0
SIFT_CLKS1
SIFT_CLKS2
SIFT_CLKS3
ENABLE_SIFT_CLKS
CHANGE_MODE
SVX_MODE0
SVX_MODE1
ADC_DATA[9..0]
FPGA_PWR_ENBL
Place adjacent to regulator input.
C11083 1 uF
U10108
TPS2032D
R10239 1K
R10240 1K
ENABLE Vout
Vin RESET*
GND
TAB_GND
TPS7525KTTT
FPGA_CORE_VCC
FPGA_CORE_VCC_FAIL
FPGA_IO_VCC_FAIL
FPGA_IO_VCC
Buffer between data bus and progam pins enabled only when programming or performing program readback, the only times that FPGA_CS is low.
Test points to allow for later misuse of FPGA pins.
C11084 10uF
Place adjacent to regulator output.
SVX_DATA_OUT[7..0]
READOUT_COMPLETE_OUT
Connects to latch pins elsewhere on this page!
TRIP_A_PRGOUT
TRIP_B_PRGOUT
R10237 10K
R10238 10K
FPGA_CORE_VCC
C10959 0.1 uF
C10960 0.1 uF
C10961 0.1 uF
C10962 0.1 uF
C10967 0.1 uF
C10968 0.1 uF
C10969 0.1 uF
C10970 0.1 uF
Bypass/Decouple for FPGA core voltage
Bypass/Decouple for CPLD
C10515 0.1 uF
C10516 0.1 uF
C10517 0.1 uF
C10518 0.1 uF
C10519 0.1 uF
C10520 0.1 uF
C10521 0.1 uF
C10522 0.1 uF
FPGA_IO_VCC
C10955 0.1 uF
C10956 0.1 uF
C10957 0.1 uF
C10958 0.1 uF
C10963 0.1 uF
C10964 0.1 uF
C10965 0.1 uF
C10966 0.1 uF
Bypass/Decouple for FPGA I/O voltage
Back to Page 1
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
<QrgAddr4>
VSVX and LVDS data serializers, MCM #1
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Sheet 11 of 42


"Resistor" pads allow for connection of optional drop diode or resistor in case we have to adjust the threshold of the first latch to compensate for TRIP idiosyncracies.
U2006
U2007
U2008
U2009
74ALVTH16373/SO
U9229
ispLSI2128VE
LVDS_SEQ_STAT[8..1]
MCM_SHAREL[9..0]
LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the clock generator.
LVDS bus contains, on average, 9 bits of data plus one bit of board status every 53MHZ clock tick. Status information may be obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eight-bit data loaded from microprocessor.
MCM_SHARER[9..0]
10 bit bus for sharing of bits to LVDS LD of MCM tx chip viewing the component side of the board. Does not connect to anything for MCM #8.
INTER_PLD[7..0]
TRIP Control Bus definitions:
Bit 12: Enable for TRIP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRIP_A regulator
Bit 9: TRIP PR2 (common to both TRIPs)
Bit 8: TRIP SKIP8 (common to both TRIPs)
Bit 7: TRIP MOVEDATA (common to both TRIPs)
Bit 6: TRIP PIPE_RESET (common to both TRIPS)
Bit 5: TRIP PIPE_CLK (common to both TRIPs)
Bit 4: TRIP PR1 (common to both TRIPs)
Bit 3: TRIP PREZBRESET (common to both TRIPs)
Bit 2: TRIP PREZARESET (common to both TRIPs)
Bit 1: TRIP PRERESET (common to both TRIPs)
Bit 0: TRIP DIGRESETB (common to both TRIPs)
TRIP Program Control Bus definitions:
Bit 4: PRGIN to TRIP B
Bit 3: PRGIN to TRIP A
Bit 2: PRGCLKB to both TRIPs
Bit 1: PRGCONTROL to both TRIPs
Bit 0: PRGRESET to both TRIPs
TRIP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRIP 'B' MUXRESETB
Bit 6: TRIP 'B' MUXCLK
Bit 5: TRIP 'B' DIGENJ
Bit 4: TRIP 'B' DIGEN.
Bit 3: TRIP 'A' MUXRESETB
Bit 2: TRIP 'A' MUXCLK
Bit 1: TRIP 'A' DIGENJ
Bit 0: TRIP 'A' DIGEN.
LD_TST is a flag that also comes from the clock generator. It indicates that the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is asserted the seven bit pattern previously written by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.
Buffer between data bus and progam pins enabled only when programming or performing program readback, the only times that FPGA_CS is low.
Xilinx JTAG dongle connector
J2001
CON6
U2005
74LVT245
U2001
SN74ALVC164245
U2002
U2010
RC2001
EZA-ST22AAAJ
RC2002
U2004
TPS2032D
TPS7525KTTT
C2012 0.1 uF
C2013 0.1 uF
C2014 0.1 uF
C2015 0.1 uF
C2020 0.1 uF
C2021 0.1 uF
C2022 0.1 uF
C2023 0.1 uF
Bypass/Decouple for FPGA core voltage
Bypass/Decouple for CPLD
Bypass/Decouple for FPGA I/O voltage
Place adjacent to regulator input.
C2024 1 uF
R2005 1K
R2006 1K
R2003 10K
R2004 10K
C2025 Place adjacent to 10uF regulator output.
Test points to allow for later misuse of FPGA pins.
Connects to FPGA pins elsewhere on this page!
Connects to latch pins elsewhere on this page!
PIPELINE_LE2
Connects to FPGA pin elsewhere on this page!
PIPELINE_OE1
PIPELINE_LE1
Back to Page 1
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
VSVX and LVDS data serializers, MCM #1
Monday, April 26, 2004
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
Rev C
Scale
Sheet 11 of 42


"Resistor" pads allow for connection of optional drop diode or resistor in case we have to adjust the threshold of the first latch to compensate for TRIP idiosyncracies.
LOW_DISC_IN[15..0]
HIGH_DISC_IN[47..32]
U3006
U3008
U3007
U3009
74ALVTH16373/SO
U3329
ispLSI2128VE
C9376 10uF
LVDS_SEQ_STAT[8..1]
MCM_SHAREL[9..0]
LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the clock generator.
LVDS bus contains, on average, 9 bits of data plus one bit of board status every 53MHZ clock tick. Status information may be obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eight-bit data loaded from microprocessor.
MCM_SHARER[9..0]
10 bit bus for sharing of bits to LVDS LD of MCM tracker. Viewing the component side of the board. Does not connect to anything for MCM #8.
INTER_PLD[7..0]
TRIP Control Bus definitions:
Bit 12: Enable for TRIP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRIP_A regulator
Bit 9: TRIP PR2 (common to both TRIPs)
Bit 8: TRIP SKIPB (common to both TRIPs)
Bit 7: TRIP MOVEDATA (common to both TRIPs)
Bit 6: TRIP PIPE_RESET (common to both TRIPs)
Bit 5: TRIP PIPE_CLK (common to both TRIPs)
Bit 4: TRIP PR1 (common to both TRIPs)
Bit 3: TRIP PRE2BRESET (common to both TRIPs)
Bit 2: TRIP PRE2ARESET (common to both TRIPs)
Bit 1: TRIP PRERESET (common to both TRIPs)
Bit 0: TRIP DIGRESETB (common to both TRIPs)
TRIP Program Control Bus definitions:
Bit 4: PRGIN to TRIP B
Bit 3: PRGIN to TRIP A
Bit 2: PRGCLKB to both TRIPs
Bit 1: PRGCONTROL to both TRIPs
Bit 0: PRGRESET to both TRIPs
TRIP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRIP 'B' MUXRESETB
Bit 6: TRIP 'B' MUXCLK
Bit 5: TRIP 'B' DIGENJ
Bit 4: TRIP 'B' DIGEN.
Bit 3: TRIP 'A' MUXRESETB
Bit 2: TRIP 'A' MUXCLK
Bit 1: TRIP 'A' DIGENJ
Bit 0: TRIP 'A' DIGEN.
LD_TST is a flag that also comes from the clock generator. It indicates that the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is asserted the seven bit pattern previously written by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.
Buffer between data bus and progam pins enabled only when programming or performing program readback, the only times that FPGA_CS is low.
Xilinx JTAG dongle connector
J3001
CON6
RC3001
EZA-ST22AAAJ
RC3002
U3010
U3001
U3002
SN74ALVC164245
74LVT245
U3005
U3004
TPS2032D
TPS7525KTTT
Place adjacent to regulator input.
Connects to FPGA pins elsewhere on this page!
PIPELINE OE1
PIPELINE LE1
PIPELINE LE2
Connects to FPGA pin elsewhere on this page!
Connects to latch pins elsewhere on this page!
Test points to allow for later misuse of FPGA pins.
C3025 Place adjacent to 10uF regulator output.
Back to Page 1
Bypass/Decouple for FPGA core voltage
Bypass/Decouple for CPLD
Bypass/Decouple for FPGA I/O voltage
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
VSVX and LVDS data serializers, MCM #1
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Sheet 11 of 42


"Resistor" pads allow for connection of optional drop diode or resistor in case we have to adjust the threshold of the first latch to compensate for TRIP idiosyncracies.
U4006
U4007
U4008
U4009
74ALVTH16373/SO
LOW_DISC_IN[15..0]
HIGH_DISC_IN[47..32]
XD[71..0]
PIPELINE_LE2
Connects to FPGA pin elsewhere on this page!
PIPELINE_OE1
PIPELINE_LE1
U9429
ispLSI2128VE
C9476 10uF
LVDS_SEQ_STAT[8..1]
MCM_SHAREL[9..0]
LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the clock generator.
LVDS bus contains, on average, 9 bits of data plus one bit of board status every 53MHZ clock tick. Status information may be obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eight-bit data loaded from microprocessor.
MCM_SHARER[9..0]
10 bit bus for sharing of bits to LVDS CPLD of MCM that is viewing the component side of the board. Does not connect to anything for MCM #8.
INTER_PLD[7..0]
TRIP Control Bus definitions:
Bit 12: Enable for TRIP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRIP_A regulator
Bit 9: TRIP PR2 (common to both TRIPs)
Bit 8: TRIP SKIPB (common to both TRIPs)
Bit 7: TRIP MOVEDATA (common to both TRIPs)
Bit 6: TRIP PIPE_RESET (common to both TRIPs)
Bit 5: TRIP PIPE_CLK (common to both TRIPs)
Bit 4: TRIP PR1 (common to both TRIPs)
Bit 3: TRIP PRE2BRESET (common to both TRIPs)
Bit 2: TRIP PRE2ARESET (common to both TRIPs)
Bit 1: TRIP PRERESET (common to both TRIPs)
Bit 0: TRIP DIGRESETB (common to both TRIPs)
TRIP Program Control Bus definitions:
Bit 4: PRGIN to TRIP B
Bit 3: PRGIN TRIP A
Bit 2: PRGCLKB to both TRIPs
Bit 1: PRGCONTROL to both TRIPs
Bit 0: PRGRESET to both TRIPs
TRIP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRIP 'B' MUXRESETB
Bit 6: TRIP 'B' MUXCLK
Bit 5: TRIP 'B' DIGENJ
Bit 4: TRIP 'B' DIGEN.
Bit 3: TRIP 'A' MUXRESETB
Bit 2: TRIP 'A' MUXCLK
Bit 1: TRIP 'A' DIGENJ
Bit 0: TRIP 'A' DIGEN.
LD_TST is a flag that also comes from the clock generator. It indicates that the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is asserted the seven bit pattern previously written by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.
TRIP_CTL_OUT[12..0]
TRIP_PGM_CTL[4..0]
TRIP_READOUT_CTL[12..0]
TRIP_A_PRGOUT
TRIP_B_PRGOUT
Xilinx JTAG dongle connector
J4001
CON6
JTAG[3..0]
SIFT_CLKS[4..0]
SIFT_CLKS4
RC4001
EZA-ST22AAAJ
RC4002
XING_CLK
CLK_61
CLK_53
Buffer between data bus and progam pins enabled only when programming or performing program readback, the only times that FPGA_CS is low.
U4005
74LVT245
FPGA_INIT
FPGA_DONE
V_LD_SHFT
LD_LVDS_CTL
LD_STAT
POWER_ON_RESET
TDI
BSCAN
TMS
TCK
TDO
U4010
U4002
SN74ALVC164245
Connects to FPGA pins elsewhere on this page!
PIPELINE_OE1
PIPELINE_LE1
Connects to latch pins elsewhere on this page!
Test points to allow for later misuse of FPGA pins.
C4025 Place adjacent to 10uF regulator output.
FPGA_ASTRB
FPGA_DSTRB
EV_DLY_FIFO_RCLK
EV_DLY_FIFO_OE
EV_DLY_FIFO_RE
READOUT_ENABLE
SIFT_CLKS0
SIFT_CLKS1
SIFT_CLKS2
SIFT_CLKS3
ENABLE_SIFT_CLKS
CHANGE_MODE
SVX_MODE0
SVX_MODE1
ADC_DATA[9..0]
FPGA_PWR_ENBL
FPGA_CORE_VCC
FPGA_CORE_VCC_FAIL
FPGA_IO_VCC_FAIL
FPGA_IO_VCC
Place adjacent to regulator input.
C4024 1 uF
U4003
TPS2032D
R4005 1K
R4006 1K
U4004
TPS7525KTTT
R4003 10K
R4004 10K
Bypass/Decouple for FPGA core voltage
Bypass/Decouple for CPLD
Bypass/Decouple for FPGA I/O voltage
Back to Page 1
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
<QrgAddr4>
VSVX and LVDS data serializers, MCM #1
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Sheet 11 of 42

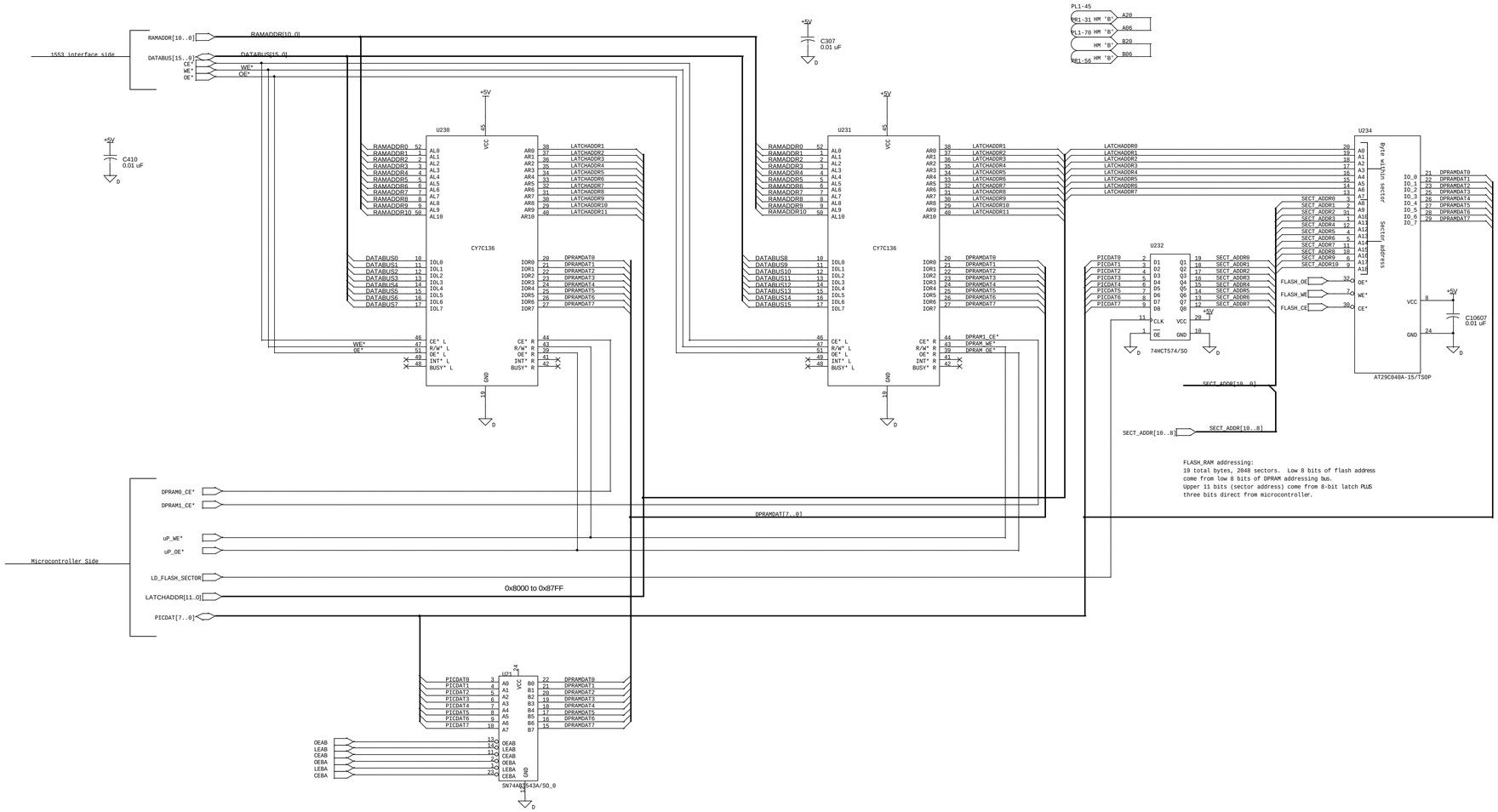
"Resistor" pads allow for connection of optional drop diode or resistor in case we have to adjust the threshold of the first latch to compensate for TRIP idiosyncracies.
U5006
U5008
U5007
U5009
74ALVTH16373/SO
U9529
C9576 10uF
ispLSI2128VE
Xilinx JTAG dongle connector
J5001
CON6
PIPELINE_LE2
Connects to FPGA pin elsewhere on this page!
PIPELINE_OE1
PIPELINE_LE1
RC5001
EZA-ST22AAAJ
RC5002
U5005
74LVT245
U5010
U5001
SN74ALVC164245
U5002
U5004
TPS2032D
TPS7525KTTT
C5012 0.1 uF
C5013 0.1 uF
C5014 0.1 uF
C5015 0.1 uF
C5020 0.1 uF
C5021 0.1 uF
C5022 0.1 uF
C5023 0.1 uF
Bypass/Decouple for FPGA core voltage
Bypass/Decouple for CPLD
C5000 0.1 uF
C5001 0.1 uF
C5002 0.1 uF
C5003 0.1 uF
C5004 0.1 uF
C5005 0.1 uF
C5006 0.1 uF
C5007 0.1 uF
FPGA_IO_VCC
C5008 0.1 uF
C5009 0.1 uF
C5010 0.1 uF
C5011 0.1 uF
C5016 0.1 uF
C5017 0.1 uF
C5018 0.1 uF
C5019 0.1 uF
Bypass/Decouple for FPGA I/O voltage
Place adjacent to regulator input.
C5024 1 uF
R5005 1K
R5006 1K
C5025 Place adjacent to 10uF regulator output.
Test points to allow for later misuse of FPGA pins.
Buffer between data bus and progam pins enabled only when programming or performing program readback, the only times that FPGA_CS is low.
LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the clock generator.
LVDS bus contains, on average, 9 bits of data plus one bit of board status every 53MHZ clock tick. Status information may be obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eight-bit data loaded from microprocessor.
10 bit bus for sharing of bits to LVDS CPLD of MCM that is viewing the component side of the board. Does not connect to anything for MCM #8.
LD_TST is a flag that also comes from the clock generator. It indicates that the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is asserted the seven bit pattern previously written by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.
TRIP Control Bus definitions:
Bit 12: Enable for TRIP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRIP_A regulator
Bit 9: TRIP PR2 (common to both TRIPs)
Bit 8: TRIP SKIPB (common to both TRIPs)
Bit 7: TRIP MOVEDATA (common to both TRIPs)
Bit 6: TRIP PIPE_RESET (common to both TRIPs)
Bit 5: TRIP PIPE_CLK (common to both TRIPs)
Bit 4: TRIP PR1 (common to both TRIPs)
Bit 3: TRIP PREZBRESET (common to both TRIPs)
Bit 2: TRIP PREZARESET (common to both TRIPs)
Bit 1: TRIP PRERESET (common to both TRIPs)
Bit 0: TRIP DIGRESETB (common to both TRIPs)
TRIP Program Control Bus definitions:
Bit 4: PRGIN to TRIP B
Bit 3: PRGIN to TRIP A
Bit 2: PRGCLKB to both TRIPs
Bit 1: PRGCONTROL to both TRIPs
Bit 0: PRGRESET to both TRIPs
TRIP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRIP 'B' MUXRESETB
Bit 6: TRIP 'B' MUXCLK
Bit 5: TRIP 'B' DIGENJ
Bit 4: TRIP 'B' DIGEN.
Bit 3: TRIP 'A' MUXRESETB
Bit 2: TRIP 'A' MUXCLK
Bit 1: TRIP 'A' DIGENJ
Bit 0: TRIP 'A' DIGEN.
Back to Page 1
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
VSVX and LVDS data serializers, MCM #1
Monday, April 26, 2004
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Sheet 11 of 42


"Resistor" pads allow for connection of optional drop diode or resistor in case we have to adjust the threshold of the first latch to compensate for TRIP idiosyncracies.
U6006
U6008
U6007
U6009
74ALVTH16373/SO
U9629
ispLSI2128VE
C9676 10uF
LVDS_SEQ_STAT[8..1]
MCM_SHAREL[9..0]
LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the clock generator.
LD_SHFT
LVDS_OUT[9..0]
LVDS bus contains, on average, 9 bits of data plus one bit of board status every 53MHZ clock tick. Status information may be obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eight-bit data loaded from microprocessor.
LD_TST
MCM_SHARER[9..0]
10 bit bus for sharing of bits to LVDS LD of MCM tx chip viewing the component side of the board. Does not connect to anything for MCM #8.
INTER_PLD[7..0]
TRIP Control Bus definitions:
Bit 12: Enable for TRIP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRIP_A regulator
Bit 9: TRIP PR2 (common to both TRIPs)
Bit 8: TRIP SKIPB (common to both TRIPs)
Bit 7: TRIP MOVEDATA (common to both TRIPs)
Bit 6: TRIP PIPE_RESET (common to both TRIPs)
Bit 5: TRIP PIPE_CLK (common to both TRIPs)
Bit 4: TRIP PR1 (common to both TRIPs)
Bit 3: TRIP PREZBRESET (common to both TRIPs)
Bit 2: TRIP PREZARESET (common to both TRIPs)
Bit 1: TRIP PRERESET (common to both TRIPs)
Bit 0: TRIP DIGRESETB (common to both TRIPs)
TRIP Program Control Bus definitions:
Bit 4: PRGIN to TRIP B
Bit 3: PRGIN to TRIP A
Bit 2: PRGCLKB to both TRIPs
Bit 1: PRGCONTROL to both TRIPs
Bit 0: PRGRESET to both TRIPs
TRIP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRIP 'B' MUXRESETB
Bit 6: TRIP 'B' MUXCLK
Bit 5: TRIP 'B' DIGENJ
Bit 4: TRIP 'B' DIGEN.
Bit 3: TRIP 'A' MUXRESETB
Bit 2: TRIP 'A' MUXCLK
Bit 1: TRIP 'A' DIGENJ
Bit 0: TRIP 'A' DIGEN.
LD_TST is a flag that also comes from the clock generator. It indicates that the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is asserted the seven bit pattern previously written by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.
TRIP_CTL_OUT[12..0]
U6001
SN74ALVC164245
TRIP_PGM_CTL[4..0]
TRIP_READOUT_CTL[12..0]
TRIP_A_PRGOUT
TRIP_B_PRGOUT
Xilinx JTAG dongle connector
J6001
CON6
PIPELINE_LE2
Connects to FPGA pin elsewhere on this page!
Connects to FPGA pins elsewhere on this page!
PIPELINE_OE1
PIPELINE_LE1
SIFT_CLKS[4..0]
SIFT_CLKS4
RC6001
EZA-ST22AAAJ
U6010
U6005
74LVT245
FPGA_INIT
FPGA_DONE
V_LD_SHFT
JTAG[3..0]
SVX_DATA_OUT[7..0]
READOUT_COMPLETE_OUT
XT_RD_CTL[12..0]
Buffer between data bus and progam pins enabled only when programming or performing program readback, the only times that FPGA_CS is low.
Connects to latch pins elsewhere on this page!
Test points to allow for later misuse of FPGA pins.
C6025 Place adjacent to 10uF regulator output.
Back to Page 1
FPGA_CORE_VCC
Bypass/Decouple for FPGA core voltage
Bypass/Decouple for CPLD
FPGA_IO_VCC
Bypass/Decouple for FPGA I/O voltage
RC6002
Place adjacent to regulator input.
C6024 1uF
U6003
TPS2032D
U6004
TPS7525KTTT
FPGA_PWR_ENBL
FPGA_CORE_VCC_FAIL
FPGA_IO_VCC_FAIL
FPGA_IO_VCC
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
VSVX and LVDS data serializers, MCM #1
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Sheet 11 of 42

"Resistor" pads allow for connection of optional drop diode or resistor in case we have to adjust the threshold of the first latch to compensate for TRIP idiosyncracies.
U7006
U7008
74ALVTH16373/SO
U7007
U7009
U9729
ispLSI2128VE
C9776 10uF
LVDS_SEQ_STAT[8..1]
MCM_SHAREL[9..0]
LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the clock generator.
LVDS bus contains, on average, 9 bits of data plus one bit of board status every 53MHZ clock tick. Status information may be obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eight-bit data loaded from microprocessor.
MCM_SHARER[9..0]
10 bit bus for sharing of bits to LVDS CPLD of MCM that is viewing the component side of the board. Does not connect to anything for MCM #8.
INTER_PLD[7..0]
TRIP Control Bus definitions:
Bit 12: Enable for TRIP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRIP_A regulator
Bit 9: TRIP PR2 (common to both TRIPs)
Bit 8: TRIP SKIPB (common to both TRIPs)
Bit 7: TRIP MOVEDATA (common to both TRIPs)
Bit 6: TRIP PIPE_RESET (common to both TRIPS)
Bit 5: TRIP PIPE_CLK (common to both TRIPs)
Bit 4: TRIP PR1 (common to both TRIPs)
Bit 3: TRIP PREZBRESET (common to both TRIPs)
Bit 2: TRIP PREZARESET (common to both TRIPs)
Bit 1: TRIP PRERESET (common to both TRIPs)
Bit 0: TRIP DIGRESETB (common to both TRIPs)
TRIP Program Control Bus definitions:
Bit 4: PRGIN to TRIP B
Bit 3: PRGIN to TRIP A
Bit 2: PRGCLKB to both TRIPs
Bit 1: PRGCONTROL to both TRIPs
Bit 0: PRGRESET to both TRIPs
TRIP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRIP 'B' MUXRESETB
Bit 6: TRIP 'B' MUXCLK
Bit 5: TRIP 'B' DIGENJ
Bit 4: TRIP 'B' DIGEN.
Bit 3: TRIP 'A' MUXRESETB
Bit 2: TRIP 'A' MUXCLK
Bit 1: TRIP 'A' DIGENJ
Bit 0: TRIP 'A' DIGEN.
LD_TST is a flag that also comes from the clock generator. It indicates that the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is asserted the seven bit pattern previously written by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.
Buffer between data bus and progam pins enabled only when programming or performing program readback, the only times that FPGA_CS is low.
Xilinx JTAG dongle connector
J7001
CON6
PIPELINE_LE2
Connects to FPGA pin elsewhere on this page!
Connects to FPGA pins elsewhere on this page!
PIPELINE_OE1
PIPELINE_LE1
RC7001
EZA-ST22AAAJ
RC7002
U7010
U7001
U7002
SN74ALVC164245
74LVT245
Connects to latch pins elsewhere on this page!
Test points to allow for later misuse of FPGA pins.
C7025 Place adjacent to 10uF regulator output.
Place adjacent to regulator input.
U7003
TPS2032D
U7004
TPS7525KTTT
Back to Page 1
Bypass/Decouple for FPGA core voltage
Bypass/Decouple for CPLD
Bypass/Decouple for FPGA I/O voltage
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
VSVX and LVDS data serializers, MCM #1
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Sheet 11 of 42

"Resistor" pads allow for connection of optional drop diode or resistor in case we have to adjust the threshold of the first latch to compensate for TRIP idiosyncracies.
LOW_DISC_IN[15..0]
HIGH_DISC_IN[47..32]
U8006
U8007
U8008
U8009
74ALVTH16373/SO
U9829
ispLSI2128VE
C9876 10uF
LVDS_SEQ_STAT[8..1]
MCM_SHAREL[9..0]
LD_SHFT is a copy of the crossing clock, appropriately phase delayed for loading the LVDS data once per crossing. It comes from the clock generator.
LD_SHFT
LVDS_OUT[9..0]
LVDS bus contains, on average, 9 bits of data plus one bit of board status every 53MHZ clock tick. Status information may be obtained from six-bit private bus from other CPLD on the page (e.g. MCM power or digital status), or via eight-bit data loaded from microprocessor.
LD_TST
INTER_PLD[7..0]
TRIP Control Bus definitions:
Bit 12: Enable for TRIP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRIP_A regulator
Bit 9: TRIP PR2 (common to both TRIPs)
Bit 8: TRIP SKIPB (common to both TRIPs)
Bit 7: TRIP MOVEDATA (common to both TRIPs)
Bit 6: TRIP PIPE_RESET (common to both TRIPS)
Bit 5: TRIP PIPE_CLK (common to both TRIPs)
Bit 4: TRIP PR1 (common to both TRIPS)
Bit 3: TRIP PREZBRESET (common to both TRIPs)
Bit 2: TRIP PREZARESET (common to both TRIPs)
Bit 1: TRIP PRERESET (common to both TRIPs)
Bit 0: TRIP DIGRESETB (common to both TRIPs)
TRIP Program Control Bus definitions:
Bit 4: PRGIN to TRIP B
Bit 3: PRGIN to TRIP A
Bit 2: PRGCLKB to both TRIPs
Bit 1: PRGCONTROL to both TRIPs
Bit 0: PRGRESET to both TRIPs
TRIP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRIP 'B' MUXRESETB
Bit 6: TRIP 'B' MUXCLK
Bit 5: TRIP 'B' DIGENJ
Bit 4: TRIP 'B' DIGEN.
Bit 3: TRIP 'A' MUXRESETB
Bit 2: TRIP 'A' MUXCLK
Bit 1: TRIP 'A' DIGENJ
Bit 0: TRIP 'A' DIGEN.
PICDAT[7..0]
LD_TST is a flag that also comes from the clock generator. It indicates that the data which should be loaded by LD_SHFT is test data, not real MCM data. When LD_TST is asserted the seven bit pattern previously written by LD_TST_PAT from the micro is loaded into all shift registers, not the MCM data.
TRIP_CTL_OUT[12..0]
U8001
SN74ALVC164245
XTRIP_CTL_OUT[12..0]
TRIP_PGM_CTL[4..0]
U8002
XT_RD_CTL[12..0]
TRIP_READOUT_CTL[12..0]
TRIP_A_PRGOUT
TRIP_B_PRGOUT
Xilinx JTAG dongle connector
J8001
CON6
JTAG[3..0]
LD_LVDS_CTL
LD_STAT
POWER_ON_RESET
TDI
BSCAN
TMS
TCK
TDO
V_LD_SHFT
FPGA_CS
FPGA_CWRT
FPGA_CCLK
FPGA_PGM
FPGA_DONE
FPGA_INIT
Buffer between data bus and progam pins enabled only when programming or performing program readback, the only times that FPGA_CS is low.
PIPELINE_LE2
Connects to FPGA pin elsewhere on this page!
Connects to FPGA pins elsewhere on this page!
PIPELINE_OE1
PIPELINE_LE1
SIFT_CLKS[4..0]
SIFT_CLKS4
XING_CLK
CLK_61
CLK_53
RC8001
EZA-ST22AAAJ
U8010
VERTICAL_IPLD
GLOBAL_BOARD_IPLD
HORIZONTAL_GLOBAL_IPLD
LOCAL_IPLD_RIGHT
LOCAL_IPLD_LEFT
H_IPLD
L_IPLD_R
L_IPLD_L
READOUT_COMPLETE
SVX_DATA_OUT[7..0]
READOUT_COMPLETE_OUT
SVX_DATA_OUT7
SVX_DATA_OUT6
SVX_DATA_OUT5
SVX_DATA_OUT4
SVX_DATA_OUT3
SVX_DATA_OUT2
SVX_DATA_OUT1
SVX_DATA_OUT0
ADC_CONV_CLK
ADC_B_CS
ADC_B_SEL
ADC_A_CS
ADC_A_SEL
TRIP 'B' MUXRESETB
TRIP 'B' MUXCLK
TRIP 'B' DIGENJ
TRIP 'B' DIGEN.
TRIP 'A' MUXRESETB
TRIP 'A' MUXCLK
TRIP 'A' DIGENJ
TRIP 'A' DIGEN.
TRIP REGULATOR 'B' ENABLE
ADC REGULATOR ENABLE
TRIP REGULATOR 'A' ENABLE
TRIP MOVEDATA
TRIP PIPE_RESET
TRIP PIPE_CLK
TRIP PR1
TRIP PREZBRESETB
TRIP PREZARESETB
TRIP PRERESET
TRIP DIGRESETB
TRIP_PR2
TRIP_SKIPB
TRIP 'B' PRGOUT
TRIP_'B' PRGIN
TRIP 'A' PRGOUT
TRIP_'A' PRGIN
TRIP PRGCLKB
TRIP PRGCONTROL
TRIP PGRESET
PIPELINE LATCH 'B' LATCH ENABLE
PIPELINE LATCH 'A' LATCH ENABLE
PIPELINE LATCH 'A' OUTPUT ENABLE
FREE PIN
Test points to allow for later misuse of FPGA pins.
FPGA_ASTRB
FPGA_DSTRB
REGISTER_ASTRB
REGISTER_DSTRB
EV_DLY_FIFO_RCLK
EV_DLY_FIFO_OE
EV_DLY_FIFO_RE
READOUT_ENABLE
SIFT_CLKS0
SIFT_CLKS1
SIFT_CLKS2
SIFT_CLKS3
CLOCKGEN0
CLOCKGEN1
CLOCKGEN2
CLOCKGEN3
ENABLE_SIFT_CLKS
CHANGE_MODE
SVX_MODE0
SVX_MODE1
ADC_DATA[9..0]
ADC_DATA0
ADC_DATA1
ADC_DATA2
ADC_DATA3
ADC_DATA4
ADC_DATA5
ADC_DATA6
ADC_DATA7
ADC_DATA8
ADC_DATA9
RC8002
FPGA_PWR_ENBL
Place adjacent to regulator input.
C8024 1uF
U8003
TPS2032D
R8005 1K
R8006 1K
U8004
TPS7525KTTT
FPGA_CORE_VCC
FPGA_CORE_VCC_FAIL
FPGA_IO_VCC_FAIL
FPGA_IO_VCC
C8025 Place adjacent to 10uF regulator output.
R8003 10K
R8004 10K
Back to Page 1
FPGA_CORE_VCC
C8012 0.1 uF
C8013 0.1 uF
C8014 0.1 uF
C8015 0.1 uF
C8020 0.1 uF
C8021 0.1 uF
C8022 0.1 uF
C8023 0.1 uF
Bypass/Decouple for FPGA core voltage
Bypass/Decouple for CPLD
C8000 0.1 uF
C8001 0.1 uF
C8002 0.1 uF
C8003 0.1 uF
C8004 0.1 uF
C8005 0.1 uF
C8006 0.1 uF
C8007 0.1 uF
FPGA_IO_VCC
C8008 0.1 uF
C8009 0.1 uF
C8010 0.1 uF
C8011 0.1 uF
C8016 0.1 uF
C8017 0.1 uF
C8018 0.1 uF
C8019 0.1 uF
Bypass/Decouple for FPGA I/O voltage
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
<QrgAddr4>
VSVX and LVDS data serializers, MCM #1
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Sheet 11 of 42

Back to Page 1



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

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Batavia, IL 60510

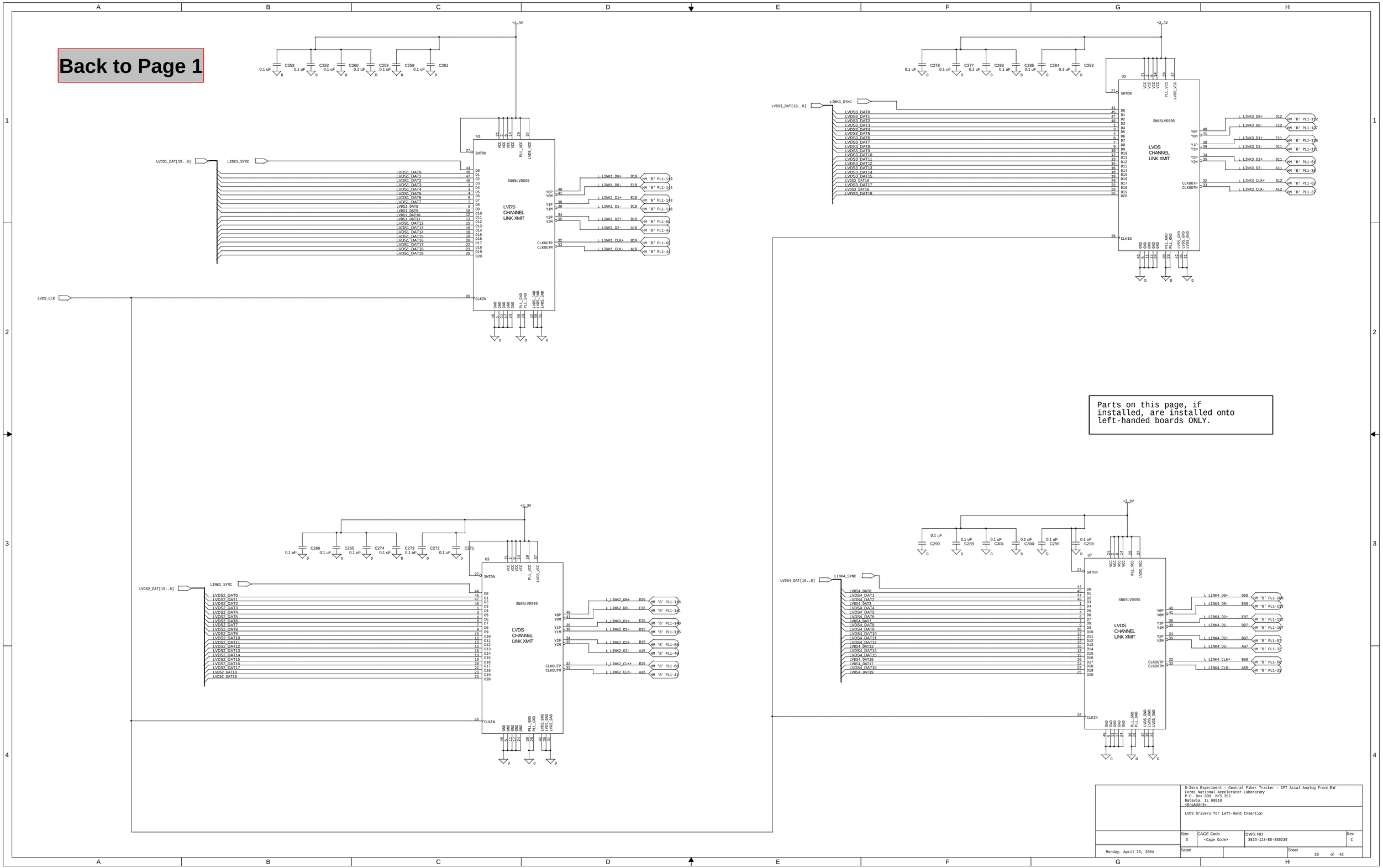
Dual-Port RAM

Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 19 of 42


Back to Page 1
LVDS CHANNEL LINK XMIT
SN65LVDS95
Parts on this page, if installed, are installed onto left-handed boards ONLY.
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
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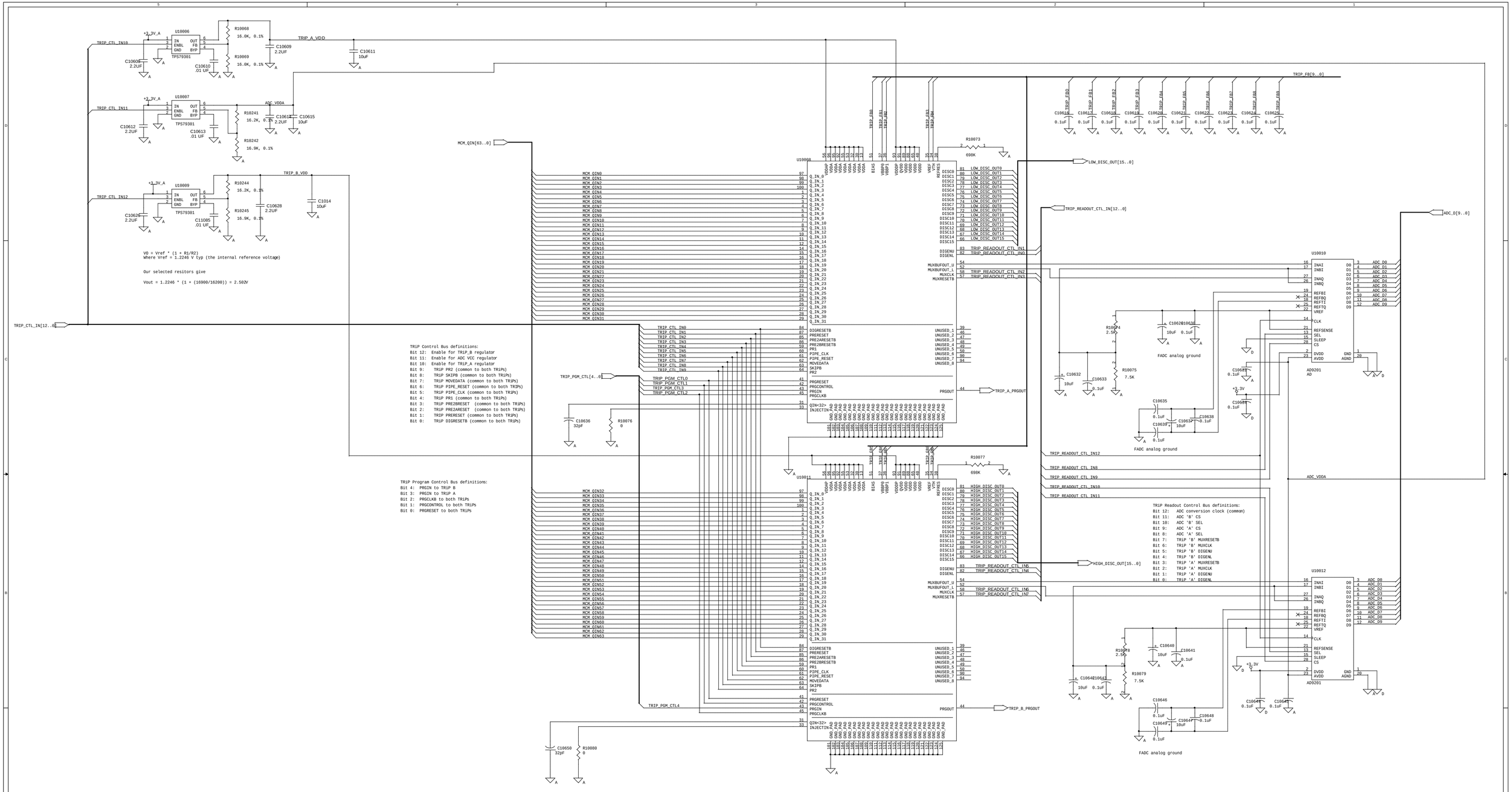
Batavia, IL 60510
<OrgAddr4>
LVDS Drivers for Left-Hand Insertion
Size D
CAGE Code <Cage Code>
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Scale
Sheet 20 of 42



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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Batavia, IL 60510
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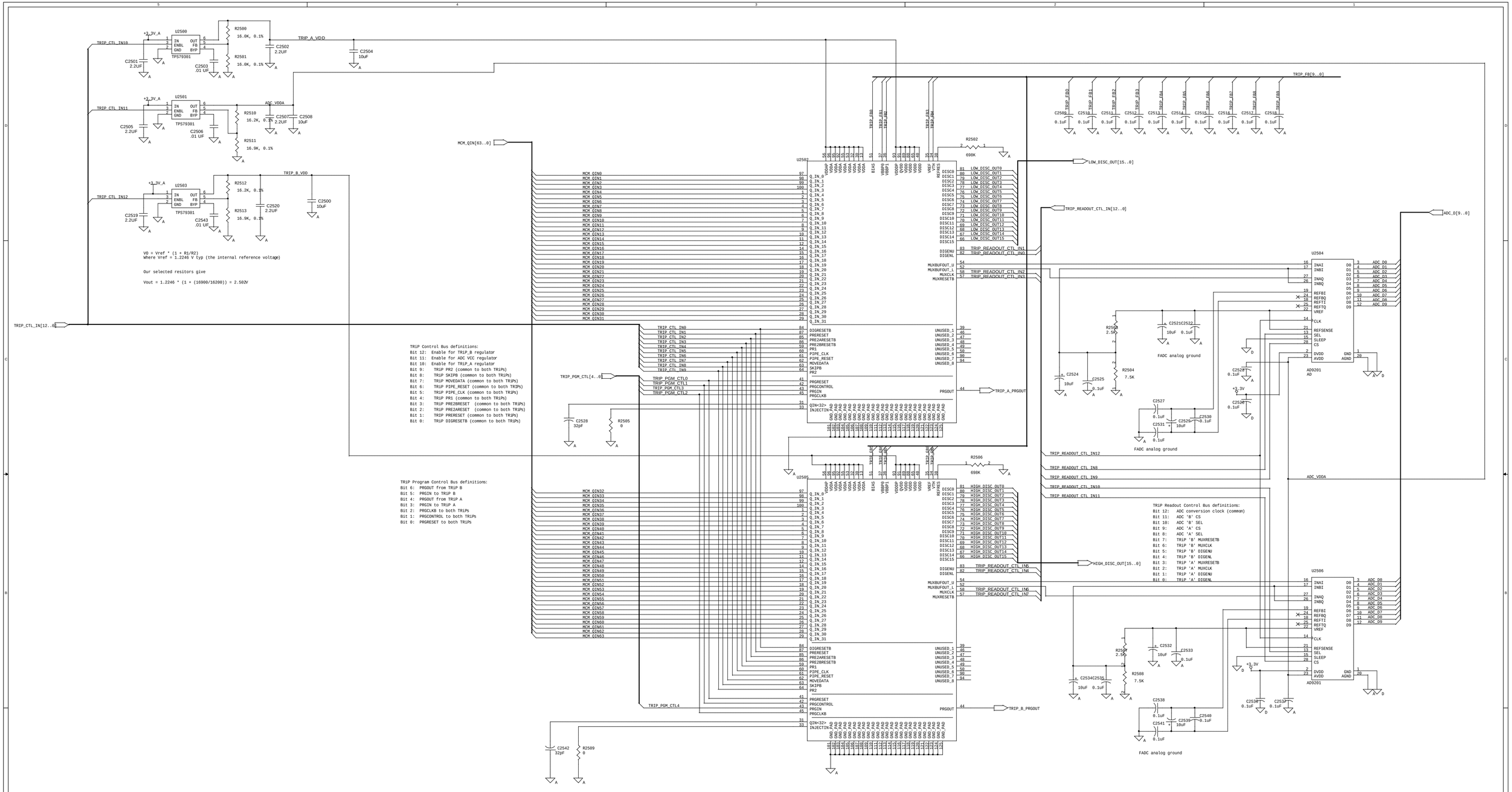
Packaged MCM 1and support circuitry

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 21 of 42



V0 = Vref * (1 + R1/R2)
Where Vref = 1.2246 V typ (the internal reference voltage)

Our selected resitors give

Vout = 1.2246 * (1 + (16900/16200)) = 2.502V

TRIP Control Bus definitions:
Bit 12: Enable for TRIP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRIP_A regulator
Bit 9: TRIP PR2 (common to both TRIPs)
Bit 8: TRIP SKIPB (common to both TRIPs)
Bit 7: TRIP MOVEDATA (common to both TRIPs)
Bit 6: TRIP PIPE_RESET (common to both TRIPs)
Bit 5: TRIP PIPE_CLK (common to both TRIPs)
Bit 4: TRIP PR1 (common to both TRIPs)
Bit 3: TRIP PRE2RRESET (common to both TRIPs)
Bit 2: TRIP PRE2ARESET (common to both TRIPs)
Bit 1: TRIP PRERESET (common to both TRIPs)
Bit 0: TRIP DIGRESETB (common to both TRIPs)

TRIP Program Control Bus definitions:
Bit 6: PRGOUT from TRIP B
Bit 5: PRGIN to TRIP B
Bit 4: PRGOUT from TRIP A
Bit 3: PRGIN to TRIP A
Bit 2: PRGCLKB to both TRIPs
Bit 1: PRGCONTROL to both TRIPs
Bit 0: PRGRESET to both TRIPs

TRIP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRIP 'B' MUXRESETB
Bit 6: TRIP 'B' MUXCLK
Bit 5: TRIP 'B' DIGENJ
Bit 4: TRIP 'B' DIGENL
Bit 3: TRIP 'A' MUXRESETB
Bit 2: TRIP 'A' MUXCLK
Bit 1: TRIP 'A' DIGENJ
Bit 0: TRIP 'A' DIGENL

All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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Batavia, IL 60510
<OrgAddr4>

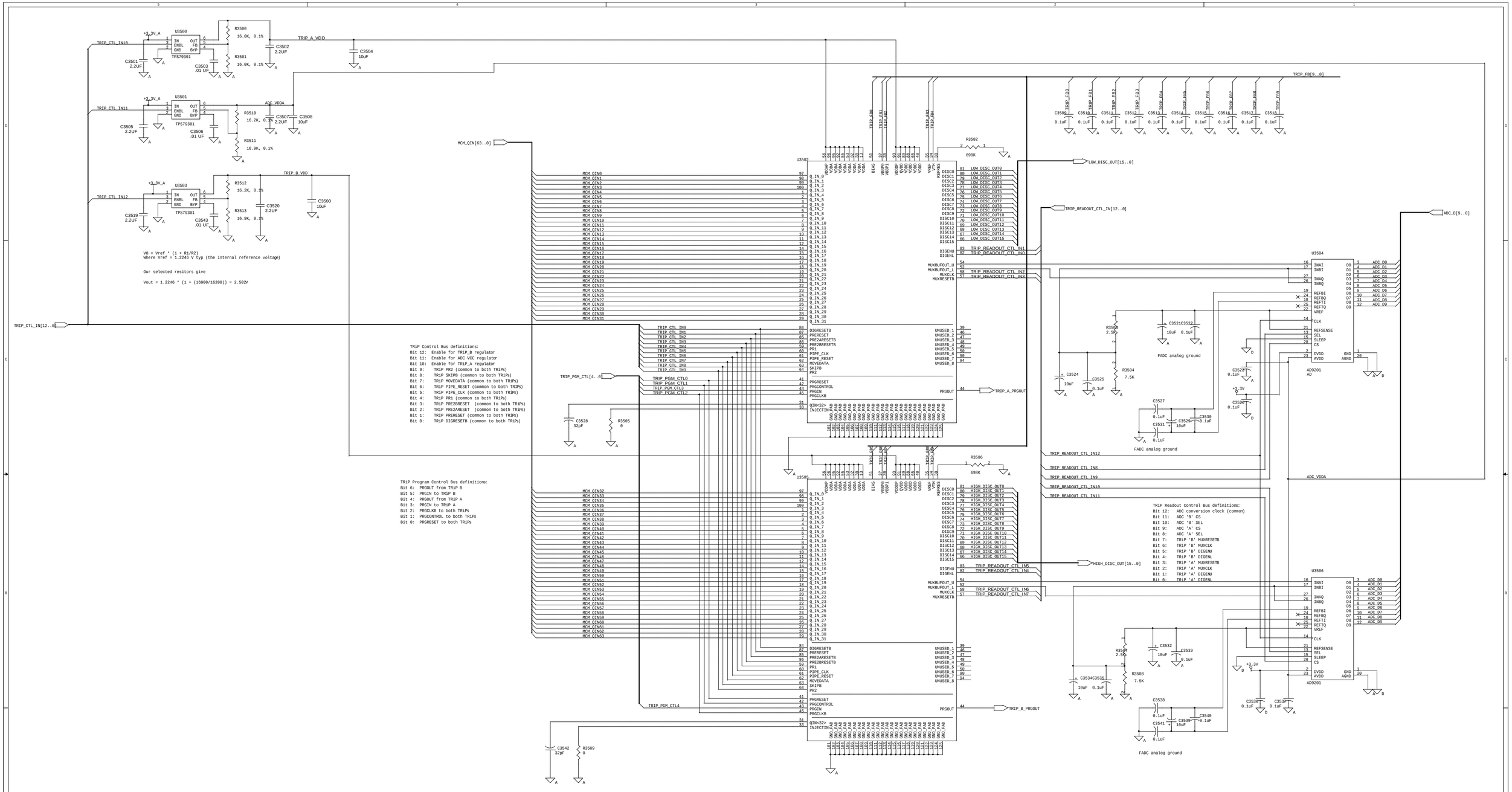
Packaged MCM 1and support circuitry

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 21 of 42



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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Batavia, IL 60510
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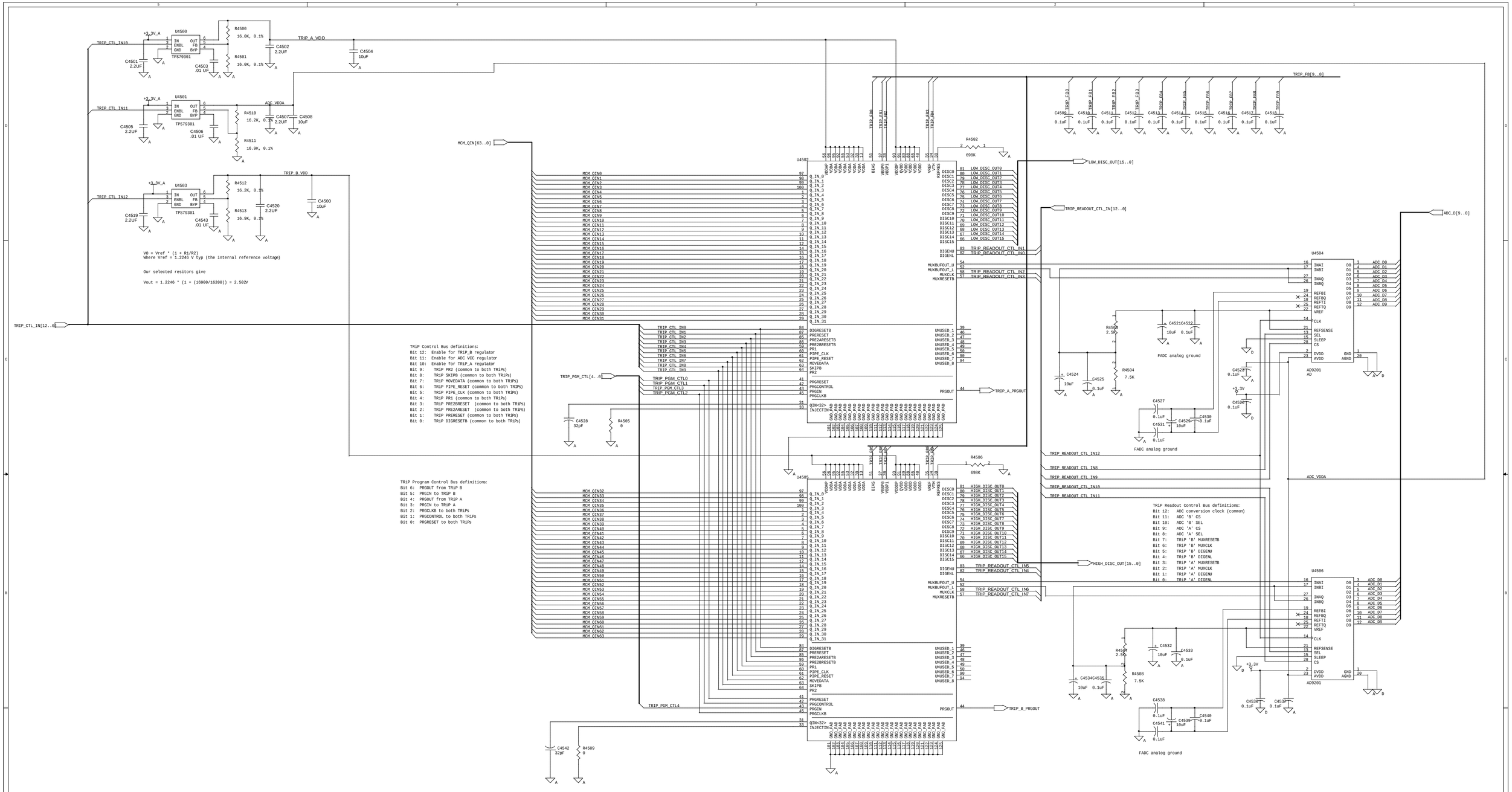
Packaged MCM 1and support circuitry

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 21 of 42



V0 = Vref * (1 + R1/R2)
Where Vref = 1.2246 V typ (the internal reference voltage)

Our selected resitors give

Vout = 1.2246 * (1 + (16900/16200)) = 2.502V

TRiP Control Bus definitions:
Bit 12: Enable for TRiP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRiP_A regulator
Bit 9: TRiP PR2 (common to both TRiPs)
Bit 8: TRiP SKIPB (common to both TRiPs)
Bit 7: TRiP MOVEDATA (common to both TRiPs)
Bit 6: TRiP PIPE_RESET (common to both TRiPs)
Bit 5: TRiP PIPE_CLK (common to both TRiPs)
Bit 4: TRiP PR1 (common to both TRiPs)
Bit 3: TRiP PRE2RRESET (common to both TRiPs)
Bit 2: TRiP PRE2ARESET (common to both TRiPs)
Bit 1: TRiP PRERESET (common to both TRiPs)
Bit 0: TRiP DIGRESETB (common to both TRiPs)

TRiP Program Control Bus definitions:
Bit 6: PRGOUT from TRiP B
Bit 5: PRGIN to TRiP B
Bit 4: PRGOUT from TRiP A
Bit 3: PRGIN to TRiP A
Bit 2: PRGCLKB to both TRiPs
Bit 1: PRGCONTROL to both TRiPs
Bit 0: PRGRESET to both TRiPs

TRiP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRiP 'B' MUXRESETB
Bit 6: TRiP 'B' MUXCLK
Bit 5: TRiP 'B' DIGENJ
Bit 4: TRiP 'B' DIGENL
Bit 3: TRiP 'A' MUXRESETB
Bit 2: TRiP 'A' MUXCLK
Bit 1: TRiP 'A' DIGENJ
Bit 0: TRiP 'A' DIGENL

All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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<OrgAddr4>

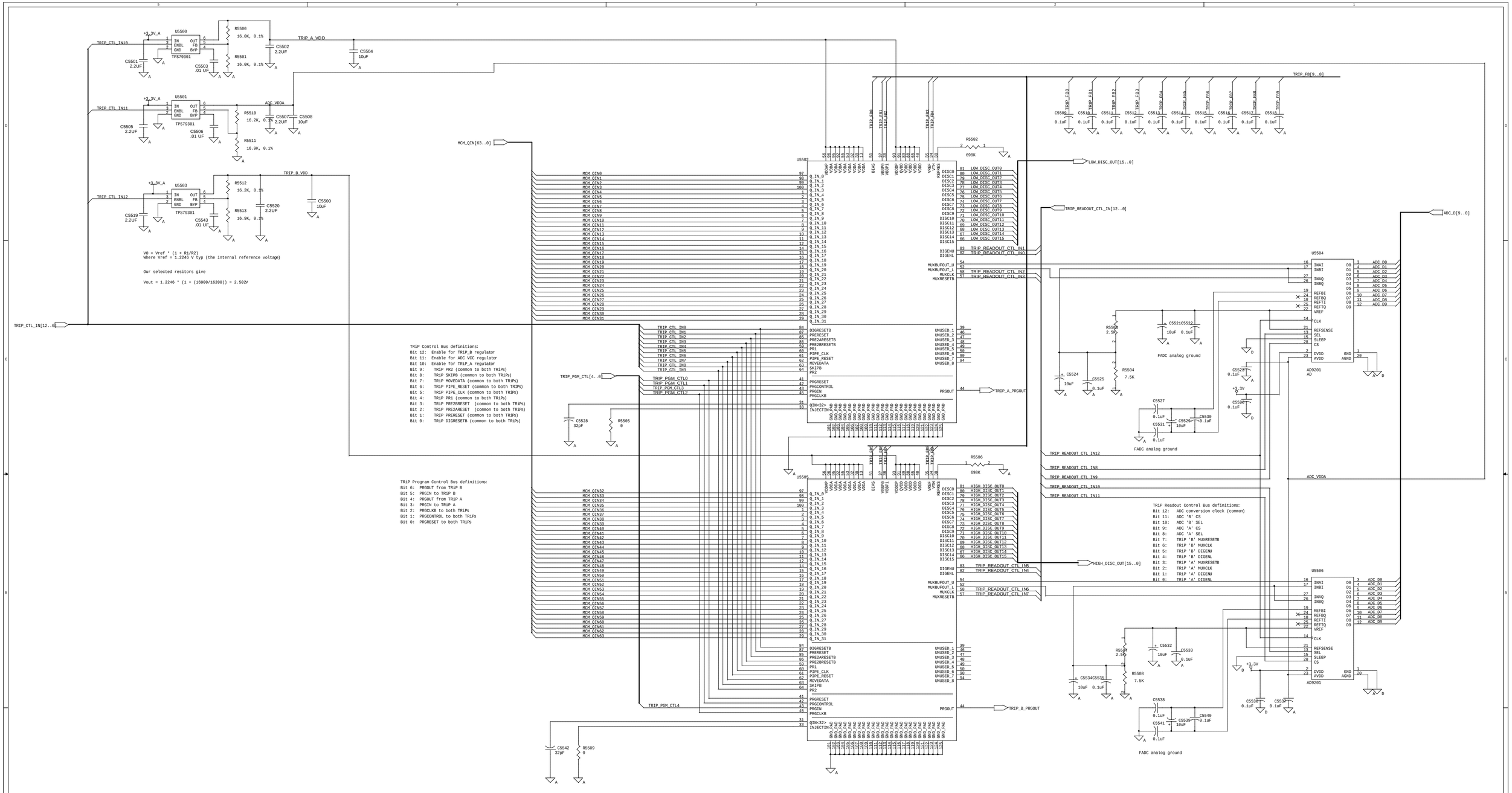
Packaged MCM 1and support circuitry

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 21 of 42



TRiP Control Bus definitions:
Bit 12: Enable for TRiP_B regulator
Bit 11: Enable for ADC VCC regulator
Bit 10: Enable for TRiP_A regulator
Bit 9: TRiP PR2 (common to both TRiPs)
Bit 8: TRiP SKIPB (common to both TRiPs)
Bit 7: TRiP MOVEDATA (common to both TRiPs)
Bit 6: TRiP PIPE_RESET (common to both TRiPs)
Bit 5: TRiP PIPE_CLK (common to both TRiPs)
Bit 4: TRiP PR1 (common to both TRiPs)
Bit 3: TRiP PRE2RRESET (common to both TRiPs)
Bit 2: TRiP PRE2ARESET (common to both TRiPs)
Bit 1: TRiP PRERESET (common to both TRiPs)
Bit 0: TRiP DIGRESETB (common to both TRiPs)

TRiP Program Control Bus definitions:
Bit 6: PRGOUT from TRiP B
Bit 5: PRGIN to TRiP B
Bit 4: PRGOUT from TRiP A
Bit 3: PRGIN to TRiP A
Bit 2: PRGCLKB to both TRiPs
Bit 1: PRGCONTROL to both TRiPs
Bit 0: PRGRESET to both TRiPs

TRiP Readout Control Bus definitions:
Bit 12: ADC conversion clock (common)
Bit 11: ADC 'B' CS
Bit 10: ADC 'B' SEL
Bit 9: ADC 'A' CS
Bit 8: ADC 'A' SEL
Bit 7: TRiP 'B' MUXRESETB
Bit 6: TRiP 'B' MUXCLK
Bit 5: TRiP 'B' DIGENU
Bit 4: TRiP 'B' DIGENL
Bit 3: TRiP 'A' MUXRESETB
Bit 2: TRiP 'A' MUXCLK
Bit 1: TRiP 'A' DIGENU
Bit 0: TRiP 'A' DIGENL

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Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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P.O. Box 500 M/S 352
Batavia, IL 60510
<OrgAddr4>

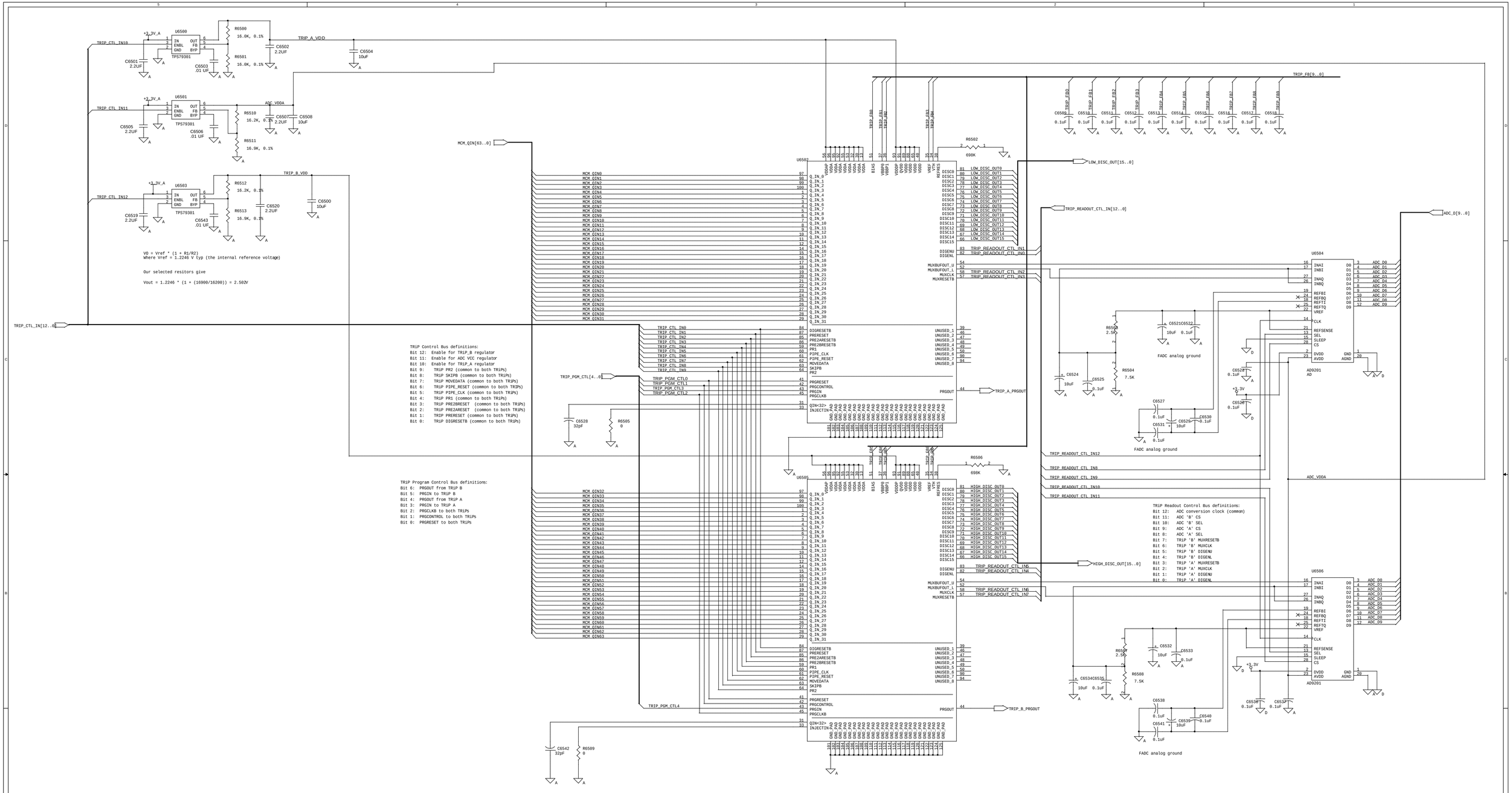
Packaged MCM 1and support circuitry

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 21 of 42



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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Batavia, IL 60510
<OrgAddr4>

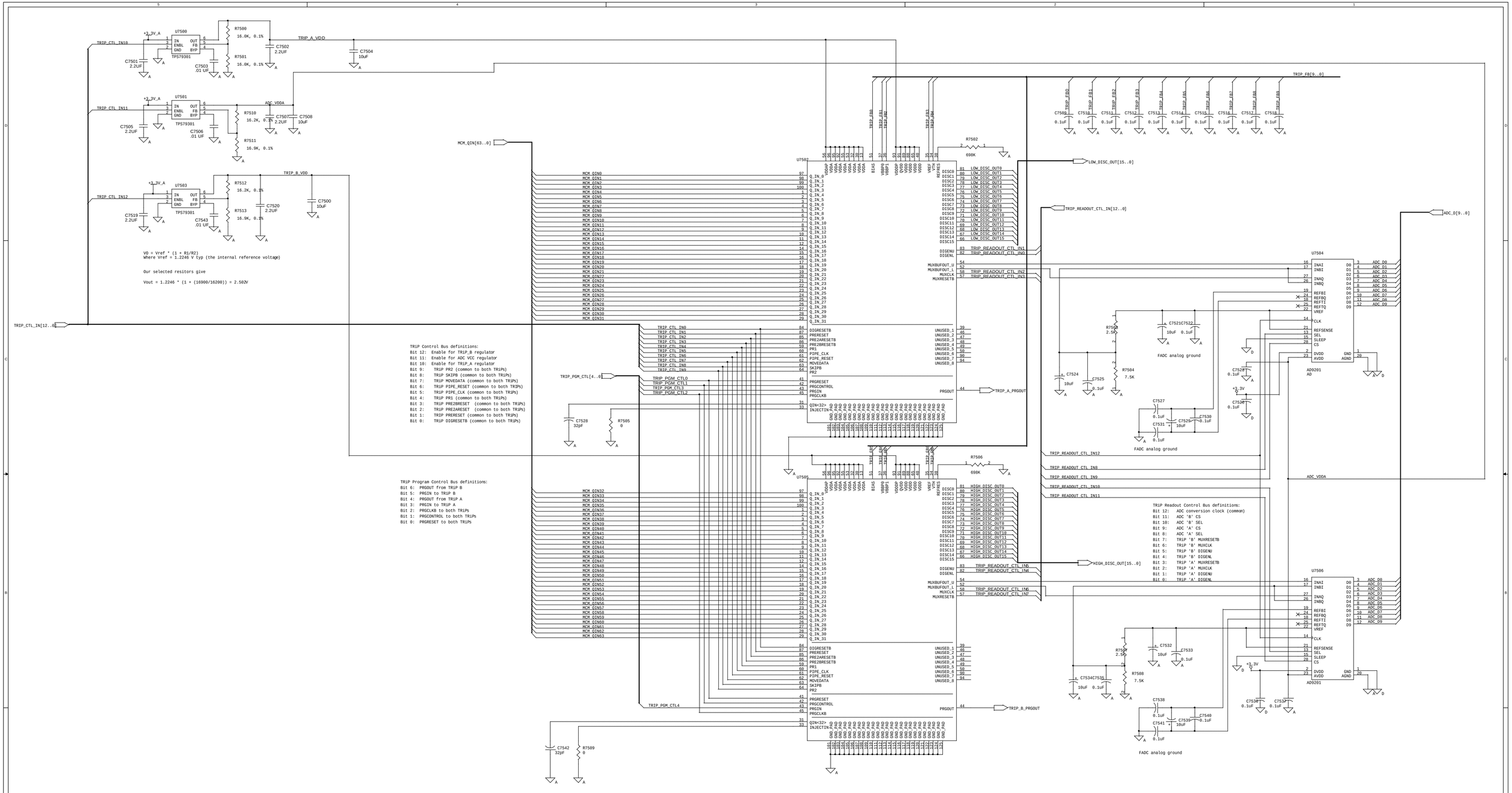
Packaged MCM 1and support circuitry

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 21 of 42



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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P.O. Box 500 M/S 352
Batavia, IL 60510
<OrgAddr4>

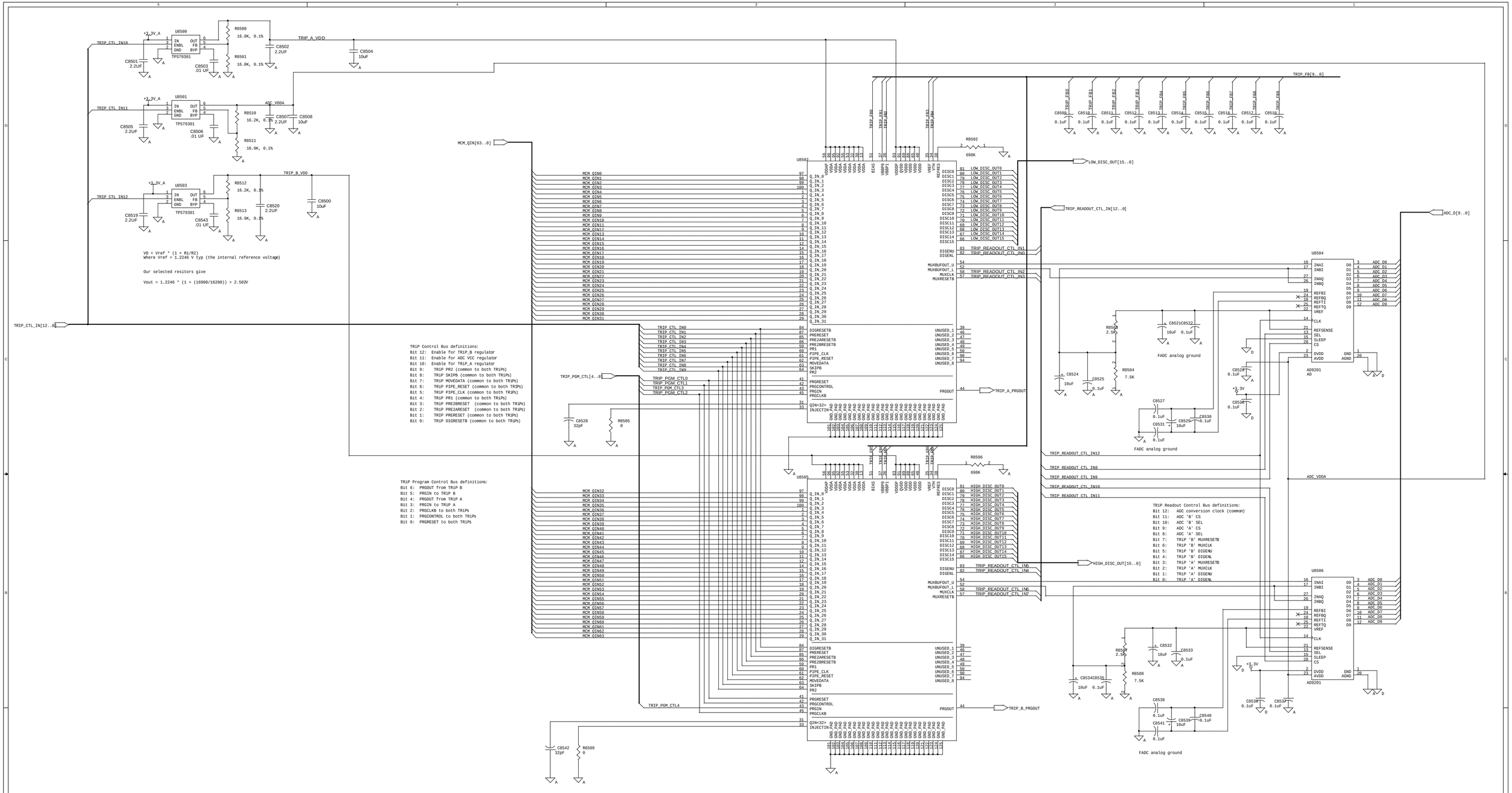
Packaged MCM 1and support circuitry

Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 21 of 42



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

Back to Page 1

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
<OrgAddr4>

Packaged MCM 1and support circuitry

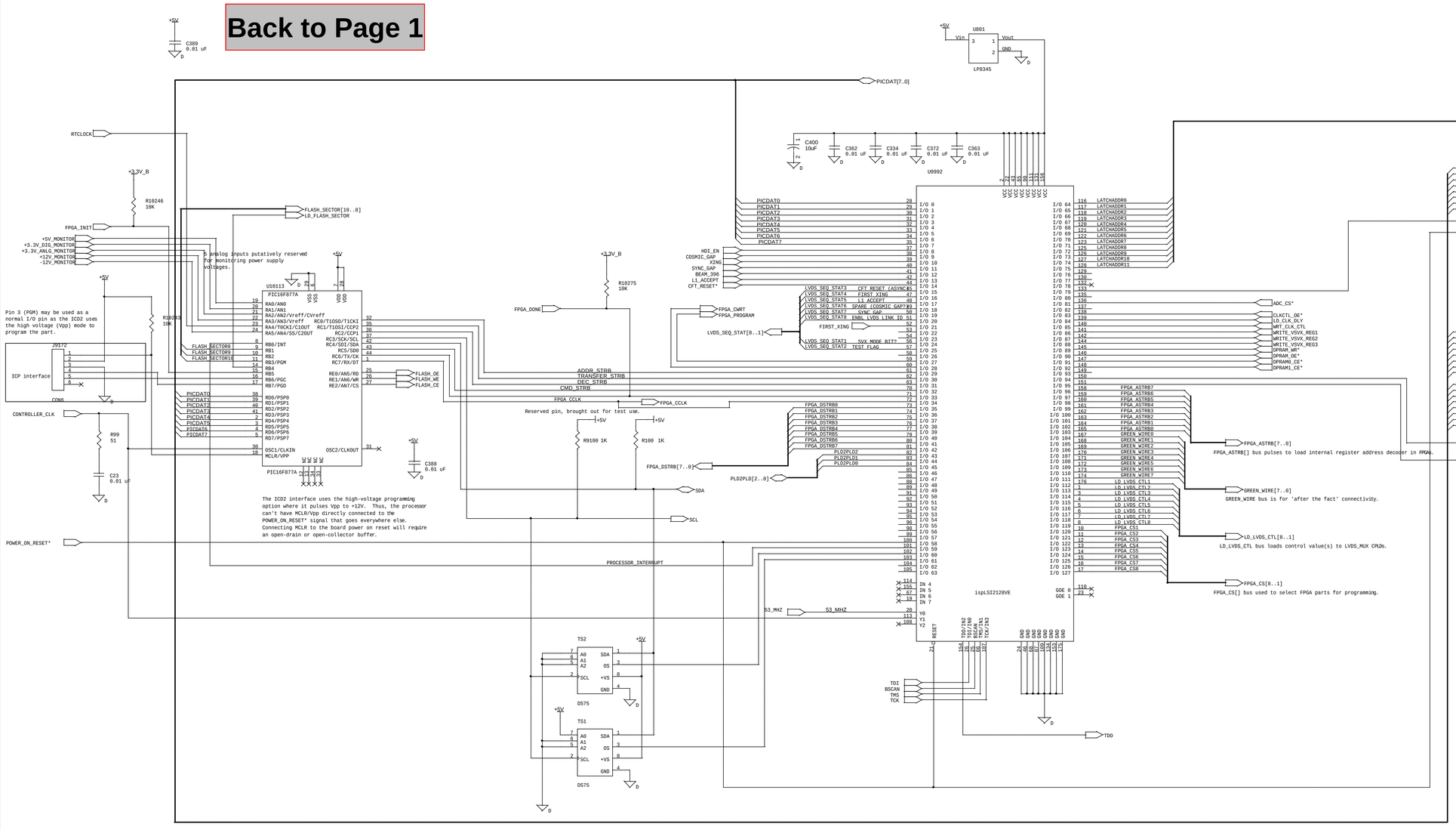
Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 21 of 42

Back to Page 1



All parts on this page, if installed, are installed in both left-handed and right-handed boards.

D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510

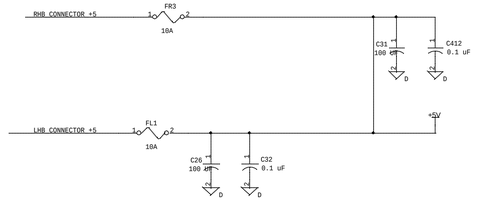
Microcontroller and Flash RAM

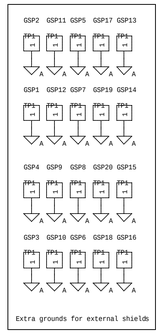
Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

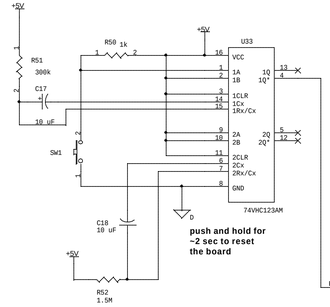
Tuesday, April 27, 2004

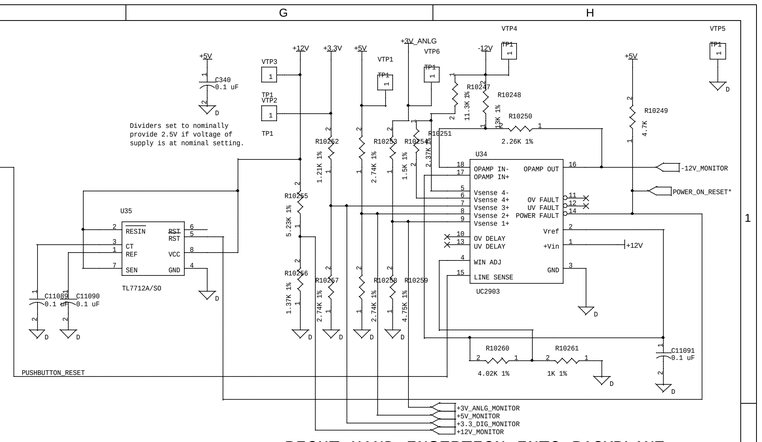
Scale

Sheet 29 of 42

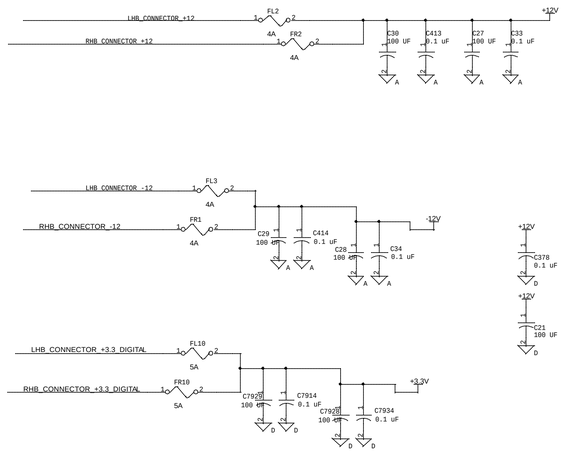


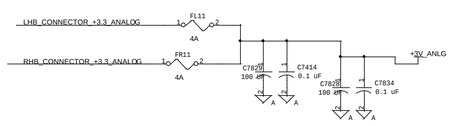


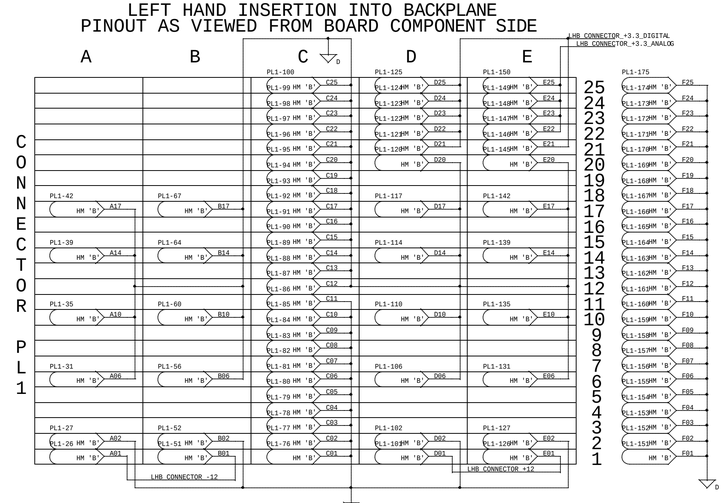


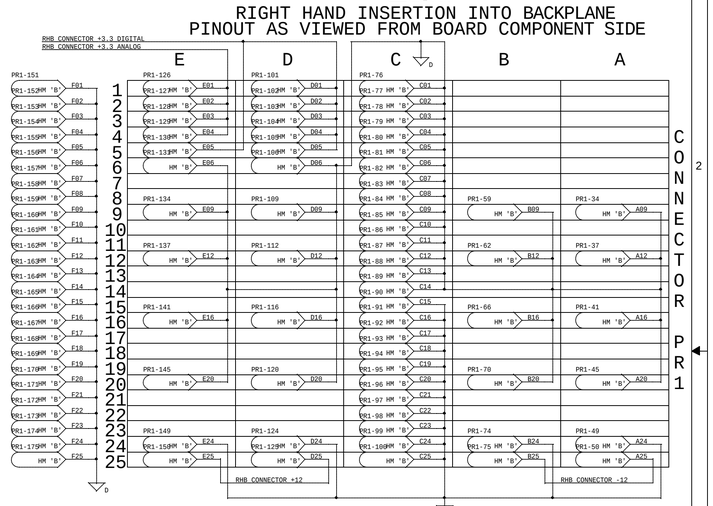


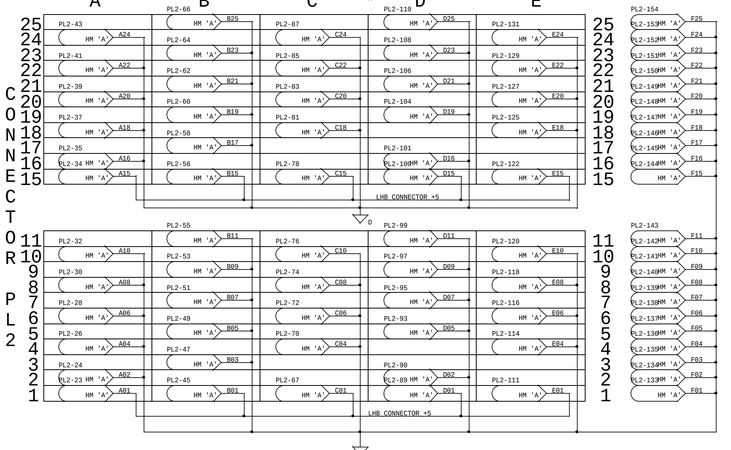
Back to Page 1

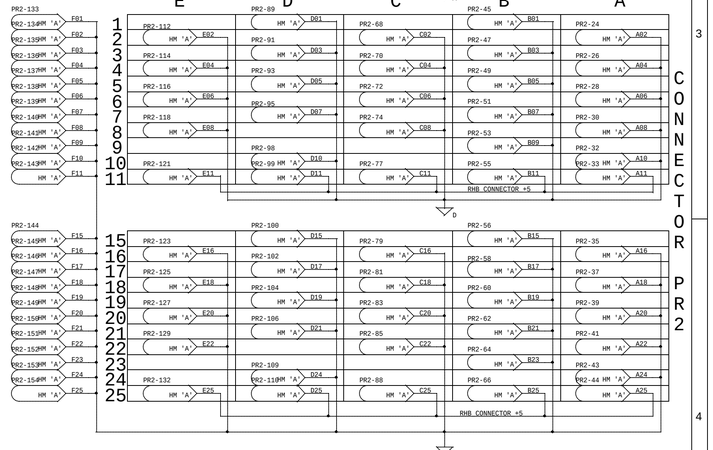


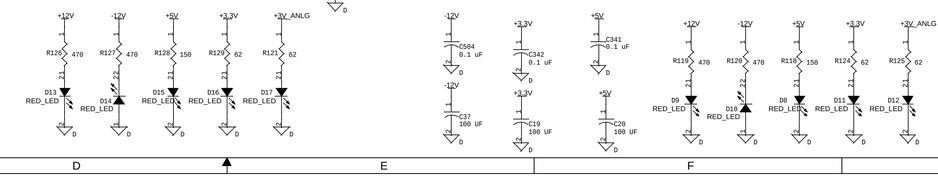












D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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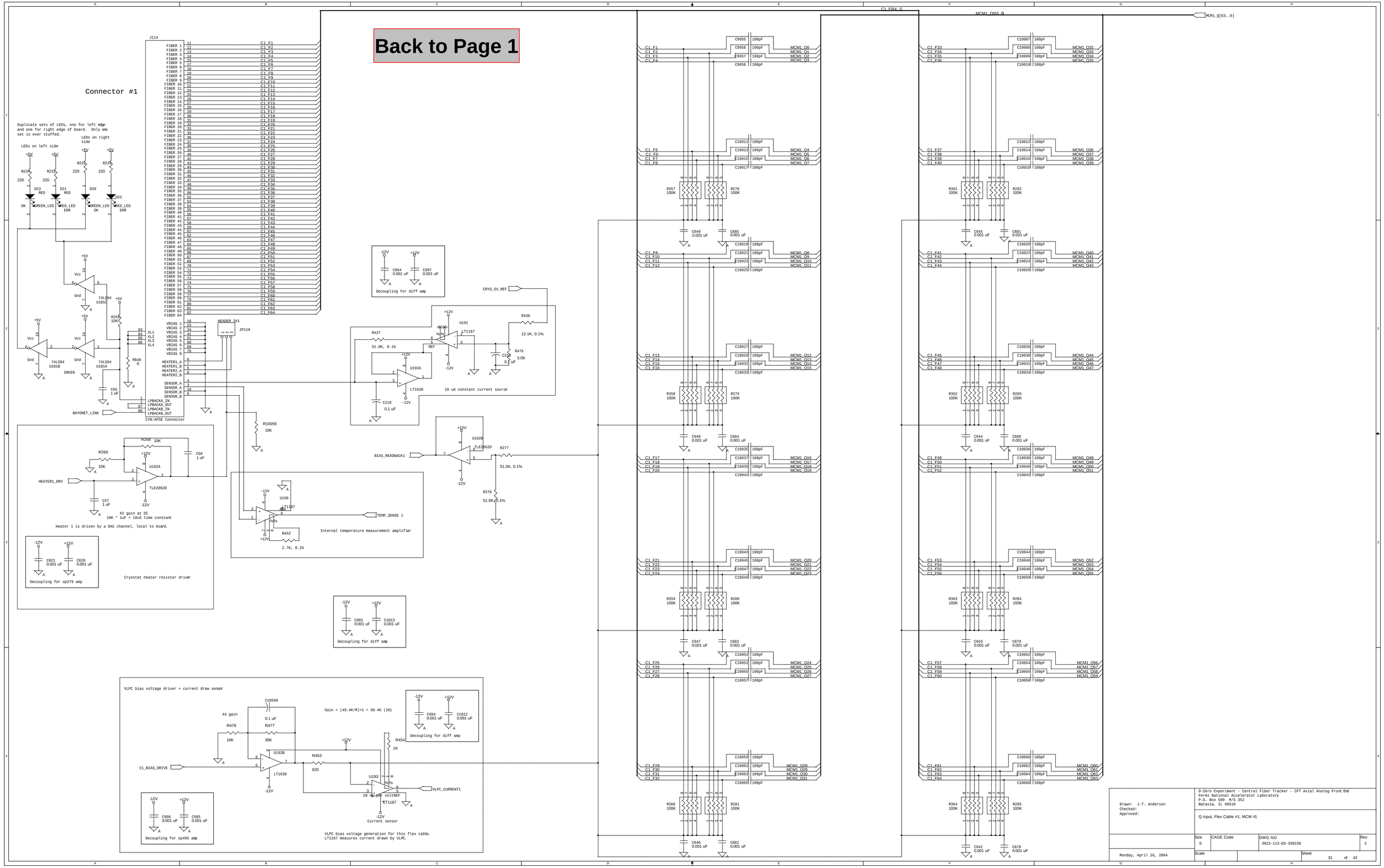
Power Connections

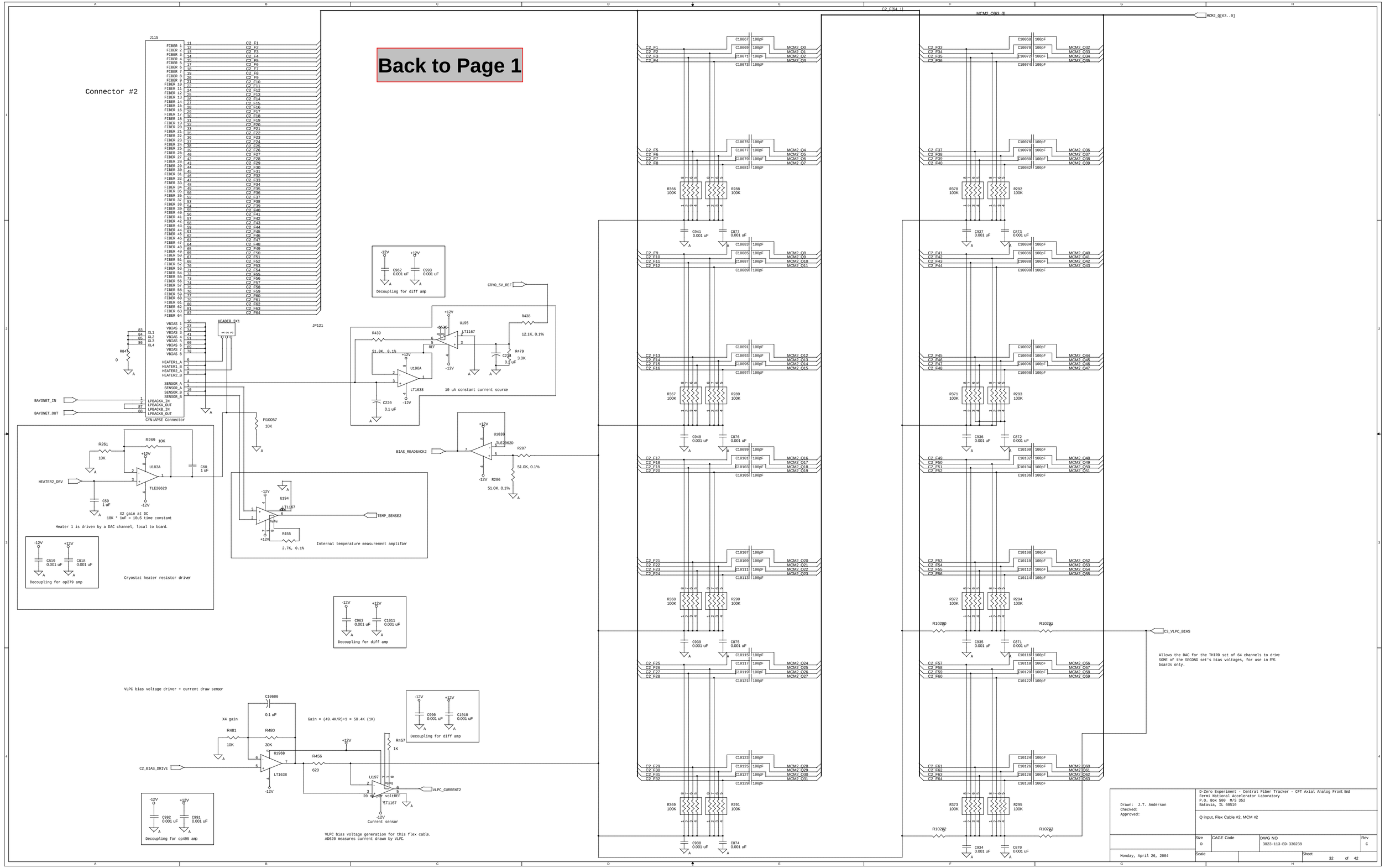
Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

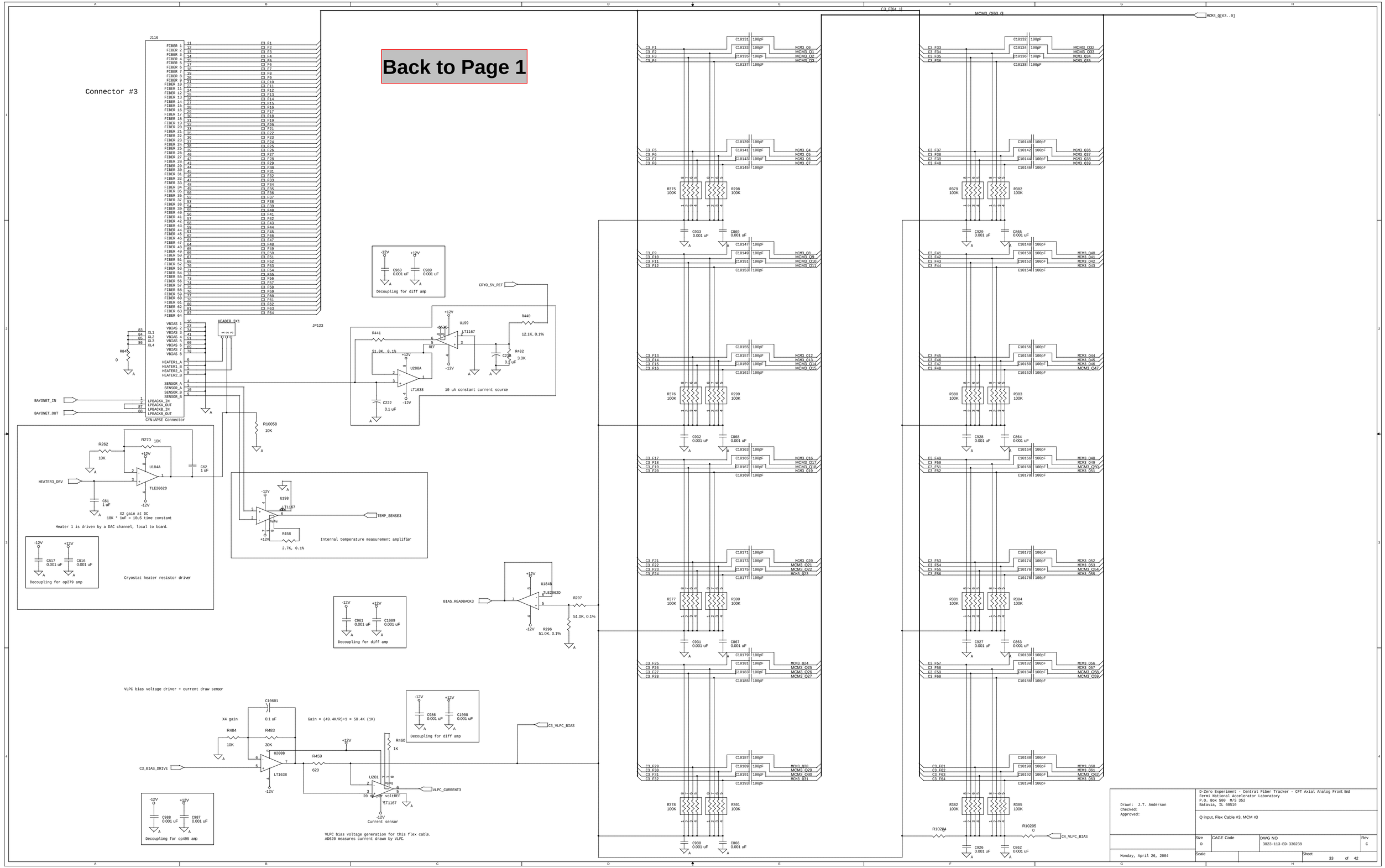
Monday, April 26, 2004

Scale

Sheet 30 of 42


Back to Page 1
Connector #1
J114
CYN:APSE Connector
Duplicate sets of LEDs, one for left edge and one for right edge of board. Only one set is ever stuffed.
LEDs on left side
LEDs on right side
BAYONET_LINK
Decoupling for diff amp
CRYO_5V_REF
10 uA constant current source
BIAS_READBACK1
TEMP_SENSE 1
Internal temperature measurement amplifier
HEATER1_DRV
X2 gain at DC
10K * 1uF = 10uS time constant
Heater 1 is driven by a DAC channel, local to board.
Decoupling for op279 amp
Cryostat heater resistor driver
VLPC bias voltage driver + current draw sensor
C1_BIAS_DRIVE
X4 gain
Gain = (49.4K/R)+1 = 50.4K (1K)
Decoupling for op495 amp
VLPC_CURRENT1
Current sensor
VLPC bias voltage generation for this flex cable.
LT1167 measures current drawn by VLPC.
MCM1_Q[63..0]
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #1, MCM #1
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Scale
Sheet 31 of 42


Back to Page 1
Connector #2
J115
JP121
CYN:APSE Connector
HEADER_3X1
BAYONET_IN
BAYONET_OUT
CRYO_5V_REF
BIAS_READBACK2
HEATER2_DRV
TEMP_SENSE2
VLPC_CURRENT2
C2_BIAS_DRIVE
C3_VLPC_BIAS
Decoupling for diff amp
10 uA constant current source
X2 gain at DC
10K * 1uF = 10uS time constant
Heater 1 is driven by a DAC channel, local to board.
Internal temperature measurement amplifier
Decoupling for op279 amp
Cryostat heater resistor driver
VLPC bias voltage driver + current draw sensor
X4 gain
Gain = (49.4K/R)+1 = 50.4K (1K)
Current sensor
VLPC bias voltage generation for this flex cable.
AD620 measures current drawn by VLPC.
Decoupling for op495 amp
Allows the DAC for the THIRD set of 64 channels to drive
SOME of the SECOND set's bias voltages, for use in FPS
boards only.
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #2, MCM #2
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Scale
Sheet 32 of 42



Drawn: J.T. Anderson
Checked:
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D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
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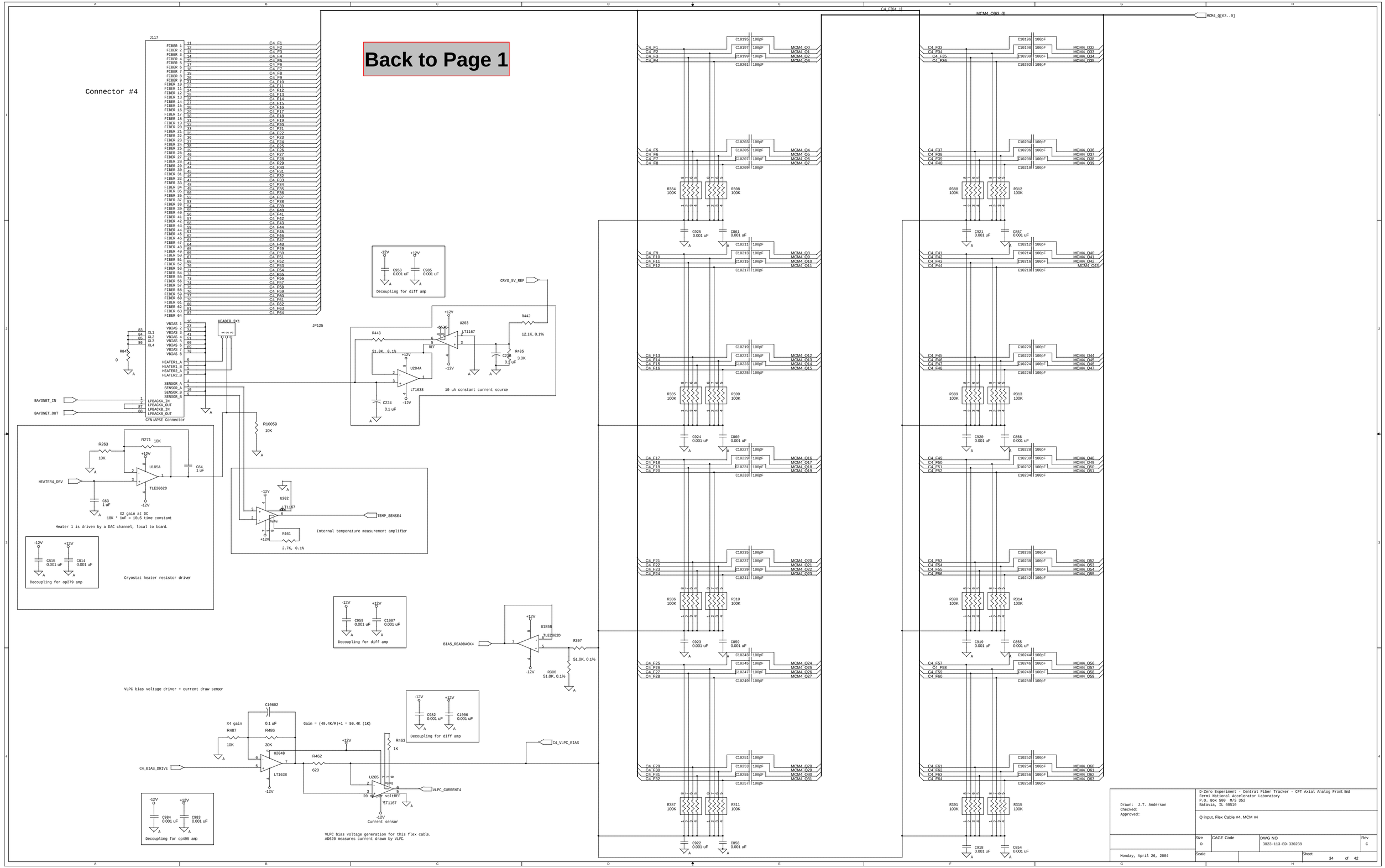
Q input, Flex Cable #3, MCM #3

Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 33 of 42


Back to Page 1
Connector #4
J117
JP125
CYN:APSE Connector
HEADER_3X1
BAYONET_IN
BAYONET_OUT
HEATER4_DRV
X2 gain at DC
10K * 1uF = 10uS time constant
Heater 1 is driven by a DAC channel, local to board.
Decoupling for op279 amp
Cryostat heater resistor driver
Decoupling for diff amp
CRYO_5V_REF
10 uA constant current source
Internal temperature measurement amplifier
TEMP_SENSE4
BIAS_READBACK4
VLPC bias voltage driver + current draw sensor
X4 gain
Gain = (49.4K/R)+1 = 50.4K (1K)
C4_BIAS_DRIVE
C4_VLPC_BIAS
VLPC_CURRENT4
Current sensor
VLPC bias voltage generation for this flex cable.
AD620 measures current drawn by VLPC.
Decoupling for op495 amp
MCM4_Q[63..0]
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
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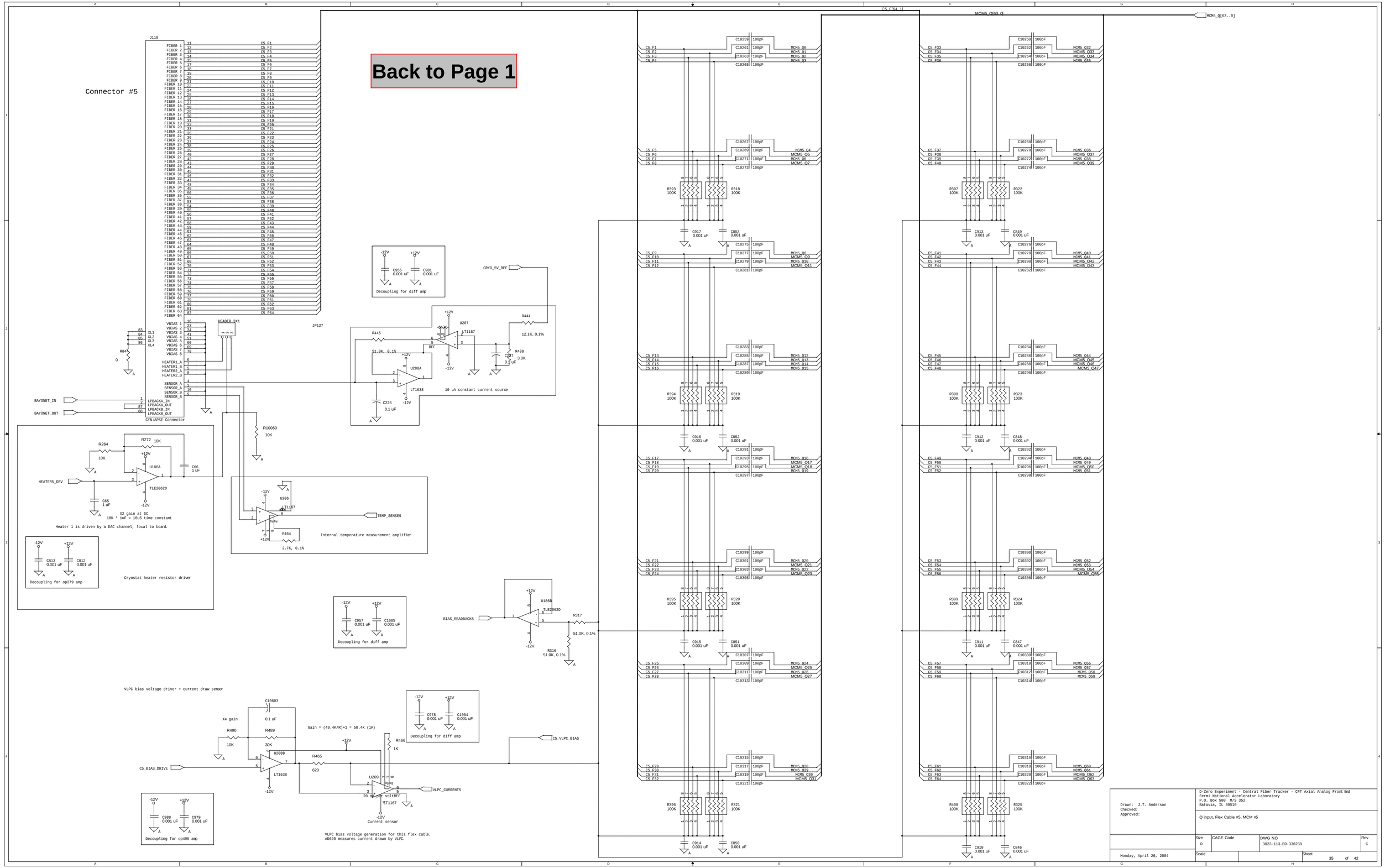
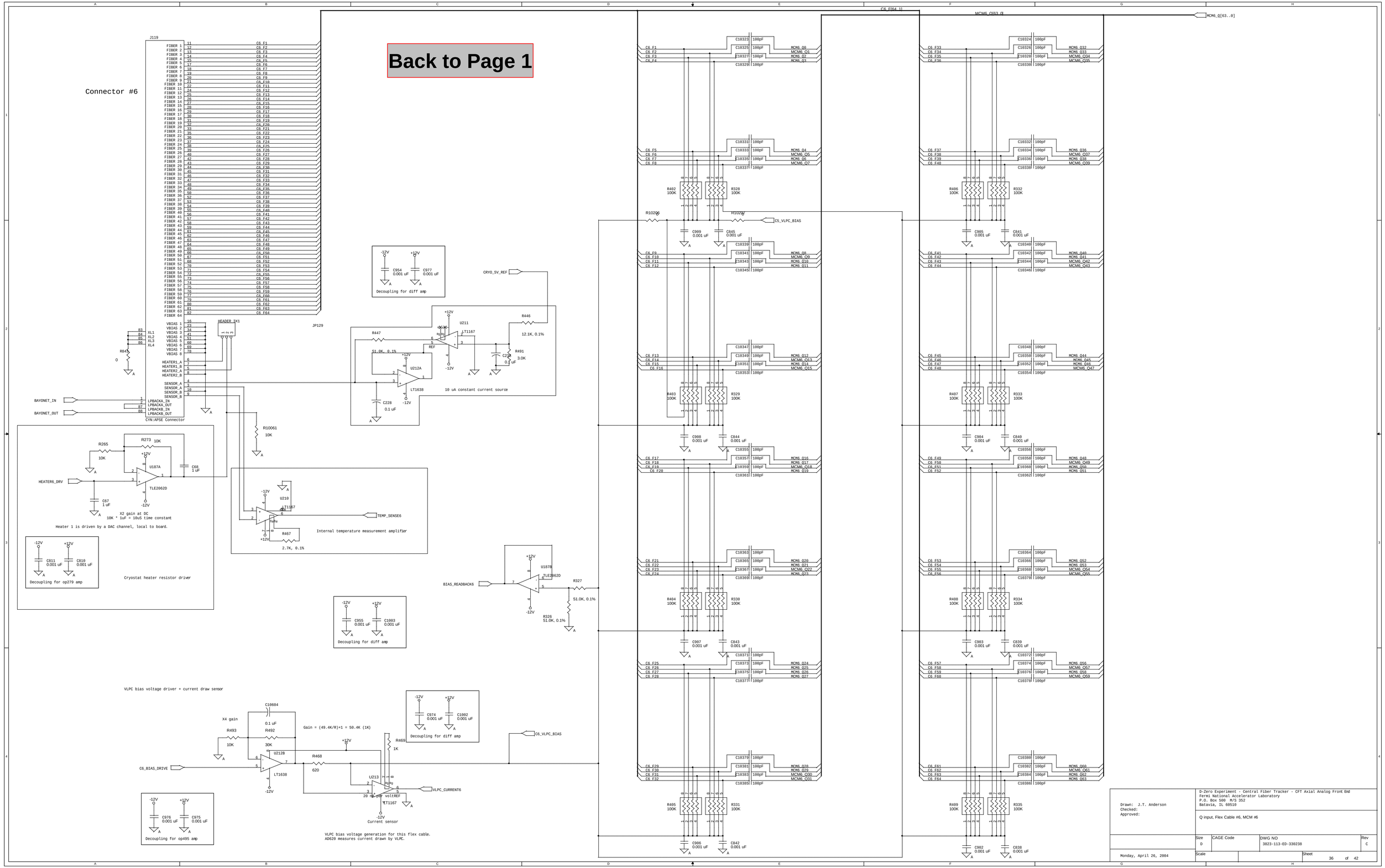
Batavia, IL 60510
Q input, Flex Cable #4, MCM #4
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Scale
Sheet 34 of 42


Back to Page 1
Connector #5
J118
JP127
CYN:APSE Connector
HEADER_3X1
BAYONET_IN
BAYONET_OUT
CRYO_5V_REF
Decoupling for diff amp
10 uA constant current source
LT1167
LT1638
U207
U208A
R445
51.0K, 0.1%
R444
12.1K, 0.1%
R488
3.0K
R10060
10K
HEATERS_DRV
U186A
TLE2062D
X2 gain at DC
10K * 1uF = 10uS time constant
Heater 1 is driven by a DAC channel, local to board.
Decoupling for op279 amp
Cryostat heater resistor driver
U206
TEMP_SENSE5
R464
2.7K, 0.1%
Internal temperature measurement amplifier
Decoupling for diff amp
BIAS_READBACK5
U186B
R317
51.0K, 0.1%
R316
51.0K, 0.1%
VLPC bias voltage driver + current draw sensor
X4 gain
Gain = (49.4K/R)+1 = 50.4K (1K)
C5_BIAS_DRIVE
U208B
LT1638
R465
620
R466
1K
U209
20 ma per voltREF
LT1167
Current sensor
VLPC_CURRENT5
C5_VLPC_BIAS
Decoupling for op495 amp
VLPC bias voltage generation for this flex cable.
AD620 measures current drawn by VLPC.
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #5, MCM #5
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Scale
Sheet 35 of 42



Drawn: J.T. Anderson
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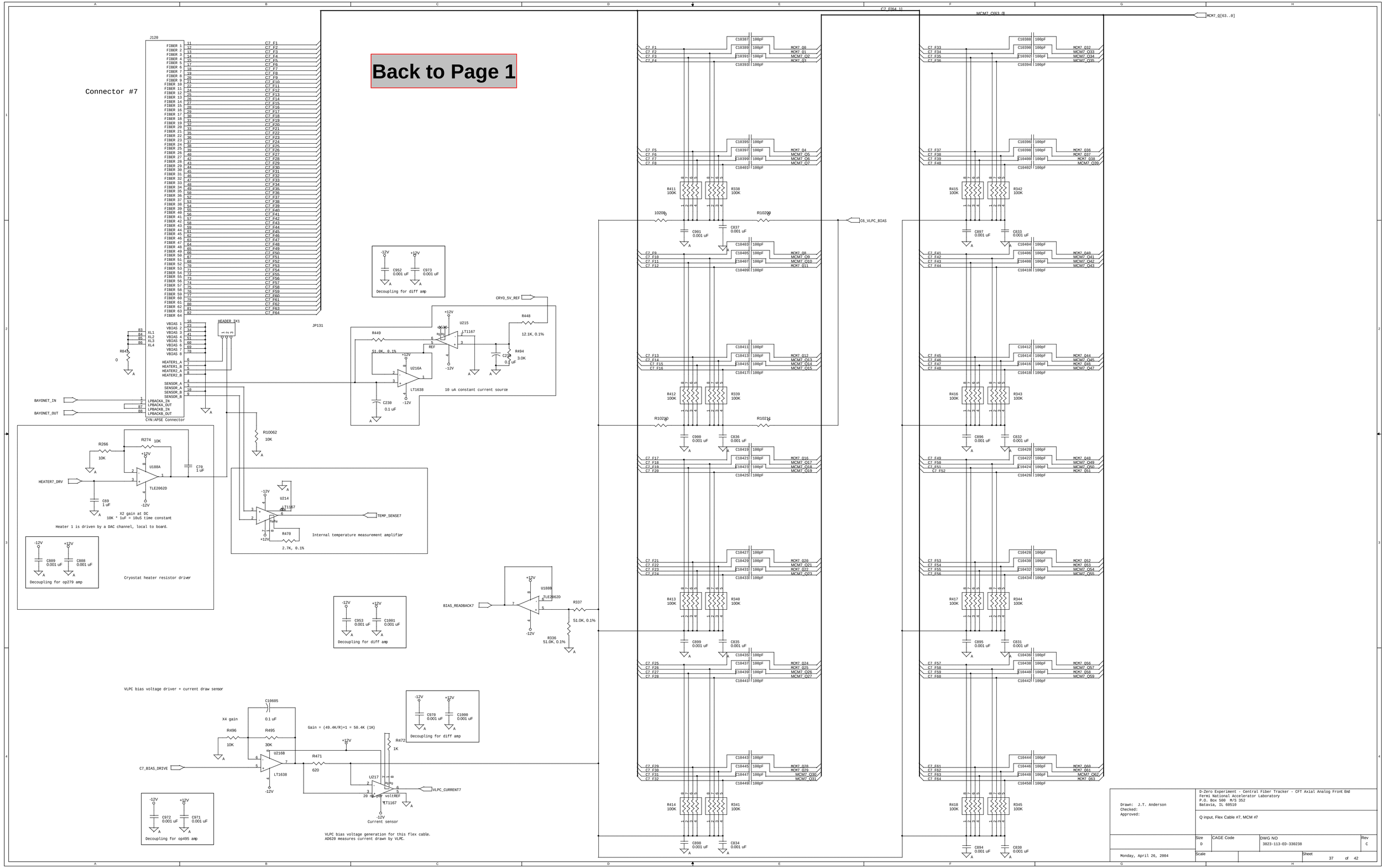
Q input, Flex Cable #6, MCM #6

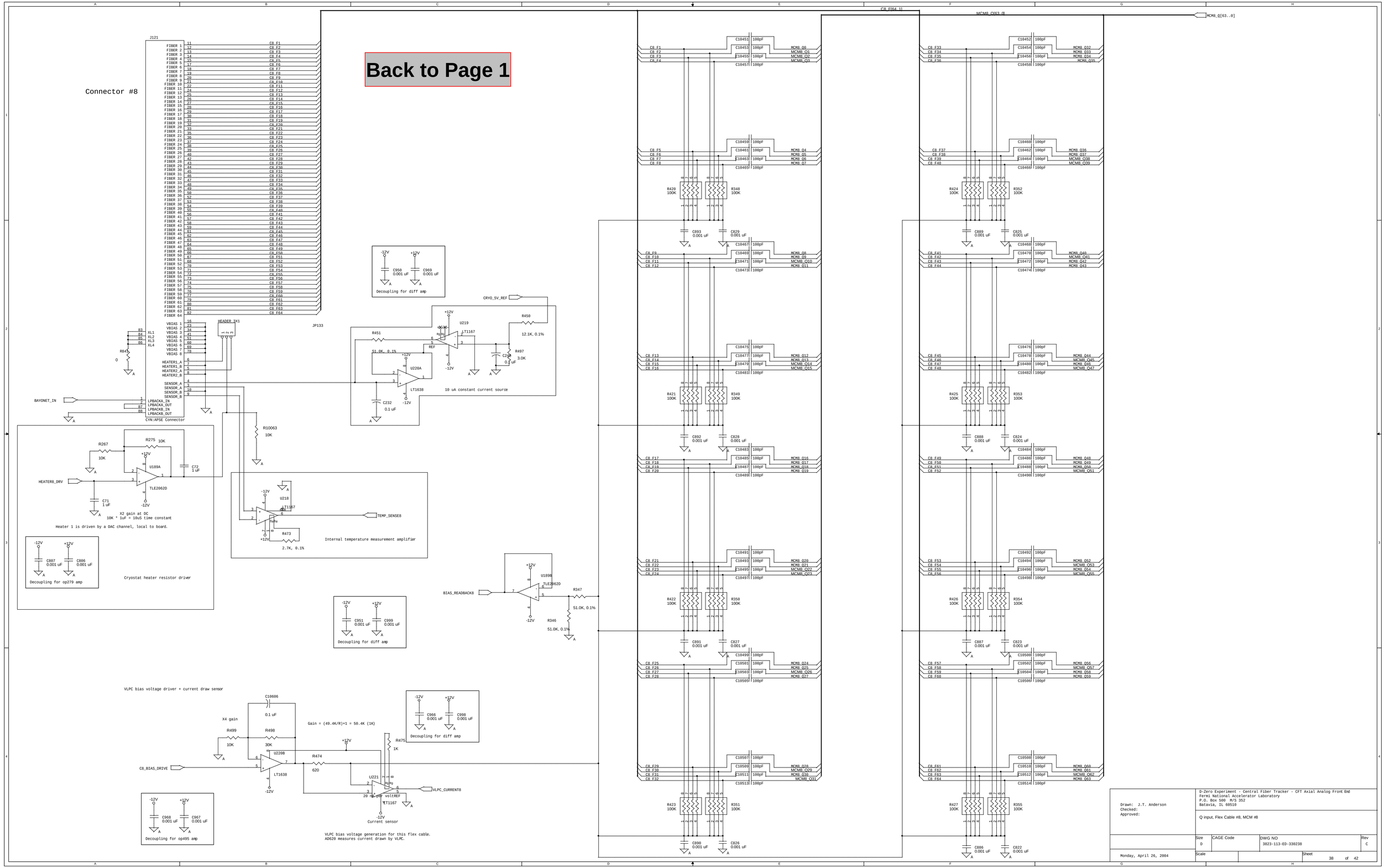
Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Monday, April 26, 2004

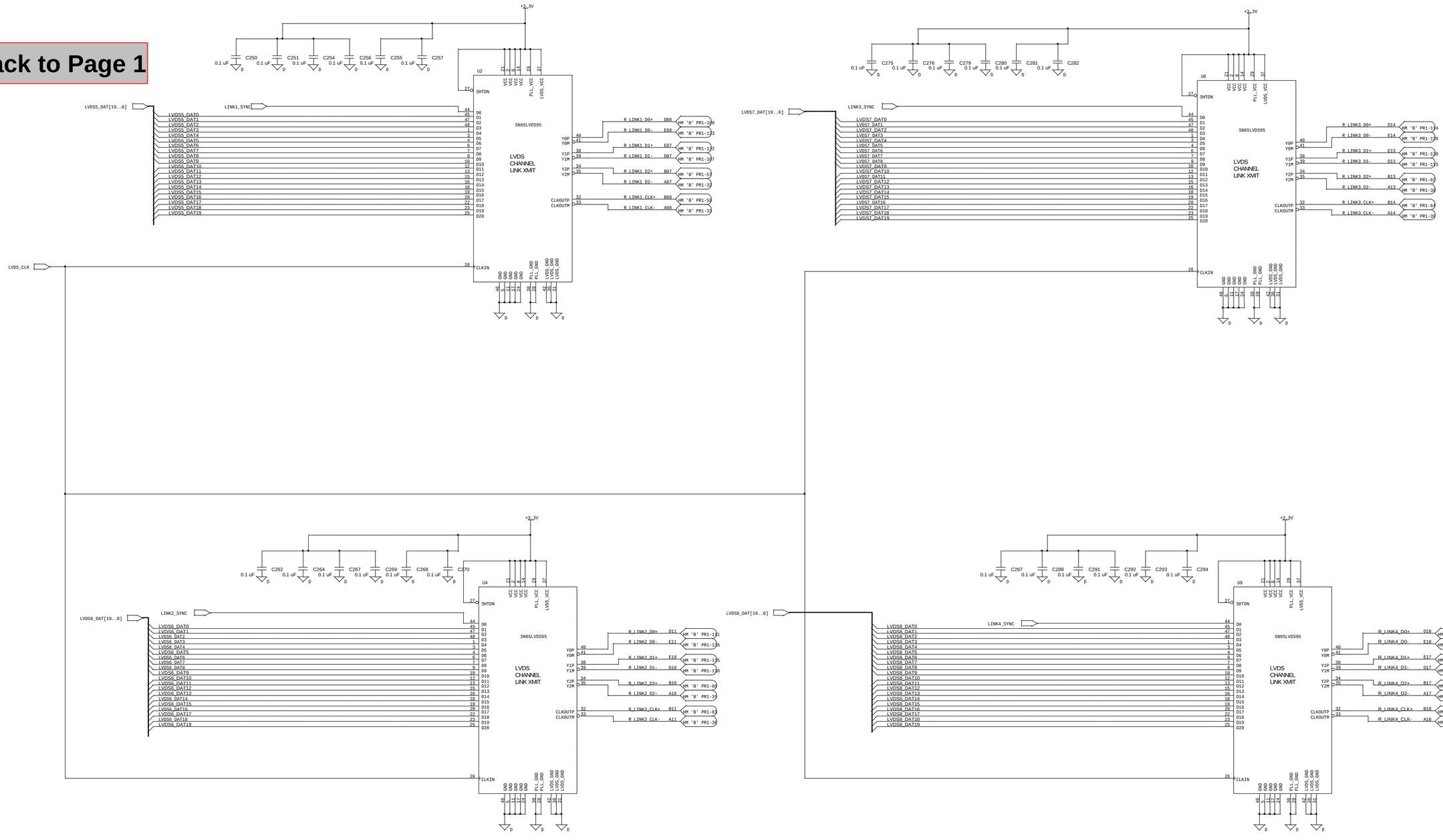
Scale

Sheet 36 of 42


Back to Page 1
Connector #7
J120
JP131
CYN:APSE Connector
BAYONET_IN
BAYONET_OUT
HEADER_3X1
Decoupling for diff amp
CRYO_5V_REF
U215
LT1167
R449
51.0K, 0.1%
R448
12.1K, 0.1%
R494
3.0K
C239
0.1 uF
U216A
LT1638
C238
0.1 uF
10 uA constant current source
R10062
10K
R266
10K
R274 10K
U188A
TLE2062D
C78
1 uF
HEATER7_DRV
C69
1 uF
X2 gain at DC
10K * 1uF = 10uS time constant
Heater 1 is driven by a DAC channel, local to board.
C809
0.001 uF
C808
0.001 uF
Decoupling for op279 amp
Cryostat heater resistor driver
U214
LT1167
TEMP_SENSE7
R470
2.7K, 0.1%
Internal temperature measurement amplifier
C953
0.001 uF
C1001
0.001 uF
Decoupling for diff amp
BIAS_READBACK7
U188B
TLE2062D
R337
51.0K, 0.1%
R336
51.0K, 0.1%
VLPC bias voltage driver + current draw sensor
C10605
0.1 uF
X4 gain
R496
10K
R495
30K
U216B
LT1638
C7_BIAS_DRIVE
R471
620
Gain = (49.4K/R)+1 = 50.4K (1K)
R472
1K
U217
LT1167
20 mV per voltREF
VLPC_CURRENT7
Current sensor
C970
0.001 uF
C1000
0.001 uF
Decoupling for diff amp
C972
0.001 uF
C971
0.001 uF
Decoupling for op495 amp
VLPC bias voltage generation for this flex cable.
AD620 measures current drawn by VLPC.
C7_F[64..1]
MCM7_Q[63..0]
MCM7_Q[63..0]
C6_VLPC_BIAS
R10200
R10201
R10210
R10211
R411 100K
R338 100K
R415 100K
R342 100K
R412 100K
R339 100K
R416 100K
R343 100K
R413 100K
R340 100K
R417 100K
R344 100K
R414 100K
R341 100K
R418 100K
R345 100K
C901 0.001 uF
C837 0.001 uF
C897 0.001 uF
C833 0.001 uF
C900 0.001 uF
C836 0.001 uF
C896 0.001 uF
C832 0.001 uF
C899 0.001 uF
C835 0.001 uF
C895 0.001 uF
C831 0.001 uF
C898 0.001 uF
C834 0.001 uF
C894 0.001 uF
C830 0.001 uF
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #7, MCM #7
Size D
CAGE Code
DWG NO 3823-113-ED-330238
Rev C
Monday, April 26, 2004
Scale
Sheet 37 of 42


Back to Page 1
Connector #8
J121
JP133
CYN:APSE Connector
HEADER_3X1
BAYONET_IN
R84
0
R10063
10K
R267
10K
R275
10K
U189A
TLE2062D
C72
1 uF
C71
1 uF
HEATER8_DRV
X2 gain at DC
10K * 1uF = 10uS time constant
Heater 1 is driven by a DAC channel, local to board.
C807
0.001 uF
C806
0.001 uF
Decoupling for op279 amp
Cryostat heater resistor driver
C950
0.001 uF
C969
0.001 uF
Decoupling for diff amp
CRYO_5V_REF
R450
12.1K, 0.1%
R451
51.0K, 0.1%
U219
LT1167
REF
R497
3.0K
C240
0.1 uF
U220A
LT1638
C232
0.1 uF
10 uA constant current source
U218
LT1167
TEMP_SENSE8
R473
2.7K, 0.1%
Internal temperature measurement amplifier
BIAS_READBACK8
U189B
TLE2062D
R347
51.0K, 0.1%
R346
51.0K, 0.1%
C951
0.001 uF
C999
0.001 uF
Decoupling for diff amp
VLPC bias voltage driver + current draw sensor
C10606
0.1 uF
X4 gain
R499
10K
R498
30K
Gain = (49.4K/R)+1 = 50.4K (1K)
C966
0.001 uF
C998
0.001 uF
Decoupling for diff amp
C8_BIAS_DRIVE
U220B
LT1638
R474
620
R475
1K
U221
20 ma per voltREF
LT1167
VLPC_CURRENT8
Current sensor
C968
0.001 uF
C967
0.001 uF
Decoupling for op495 amp
VLPC bias voltage generation for this flex cable.
AD620 measures current drawn by VLPC.
MCM8_Q[63..0]
R420
100K
R348
100K
R424
100K
R352
100K
R421
100K
R349
100K
R425
100K
R353
100K
R422
100K
R350
100K
R426
100K
R354
100K
R423
100K
R351
100K
R427
100K
R355
100K
Drawn: J.T. Anderson
Checked:
Approved:
D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End
Fermi National Accelerator Laboratory
P.O. Box 500 M/S 352
Batavia, IL 60510
Q input, Flex Cable #8, MCM #8
Size
D
CAGE Code
DWG NO
3823-113-ED-330238
Rev
C
Monday, April 26, 2004
Scale
Sheet
38 of 42

Back to Page 1



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LVDS Driver, Right-Handed Insertion

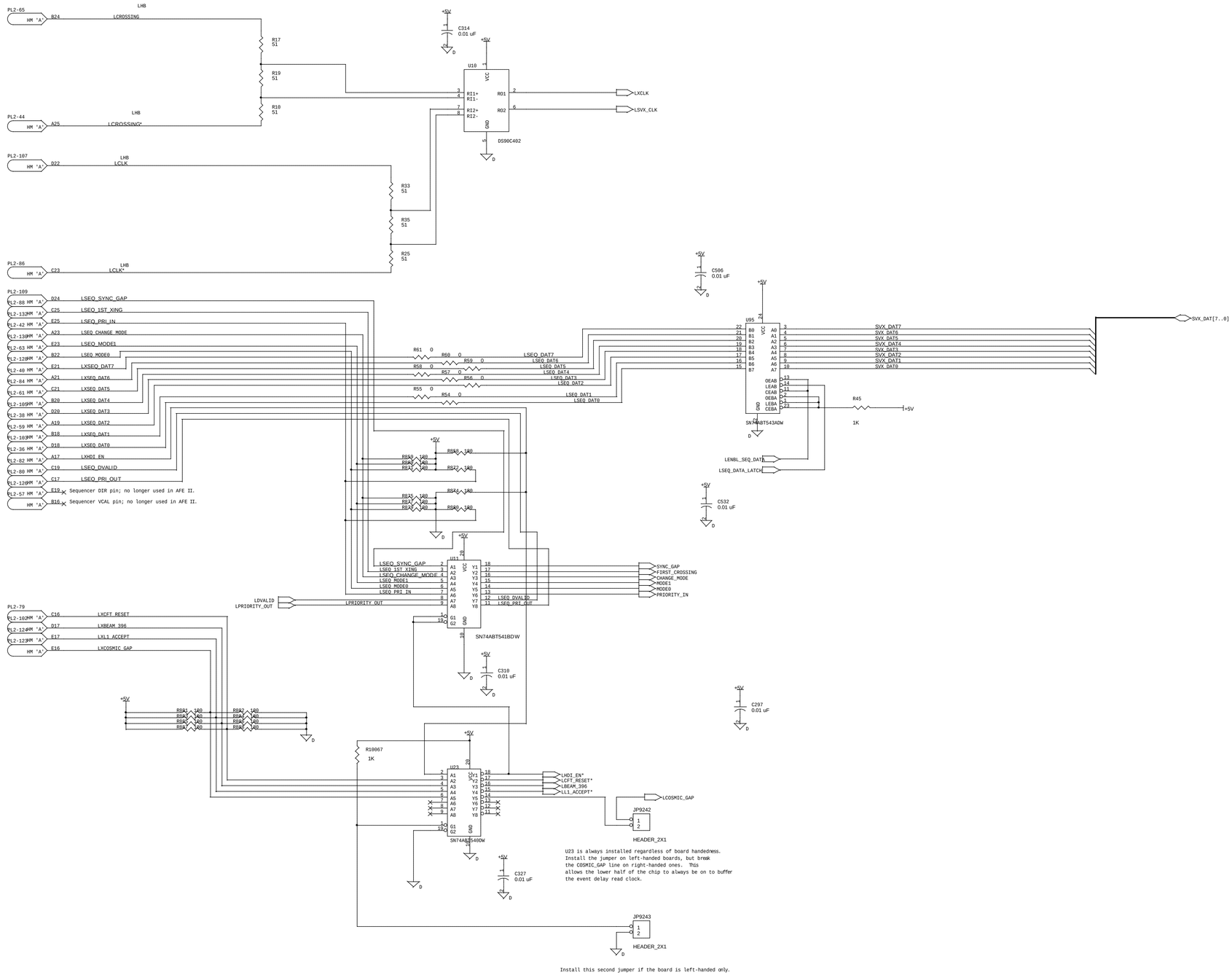
Size	CAGE Code	DWG NO	Rev
D	<Cage Code>	3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 39 of 42

Back to Page 1



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SVX Sequencer Connector - Left Handed Insertion

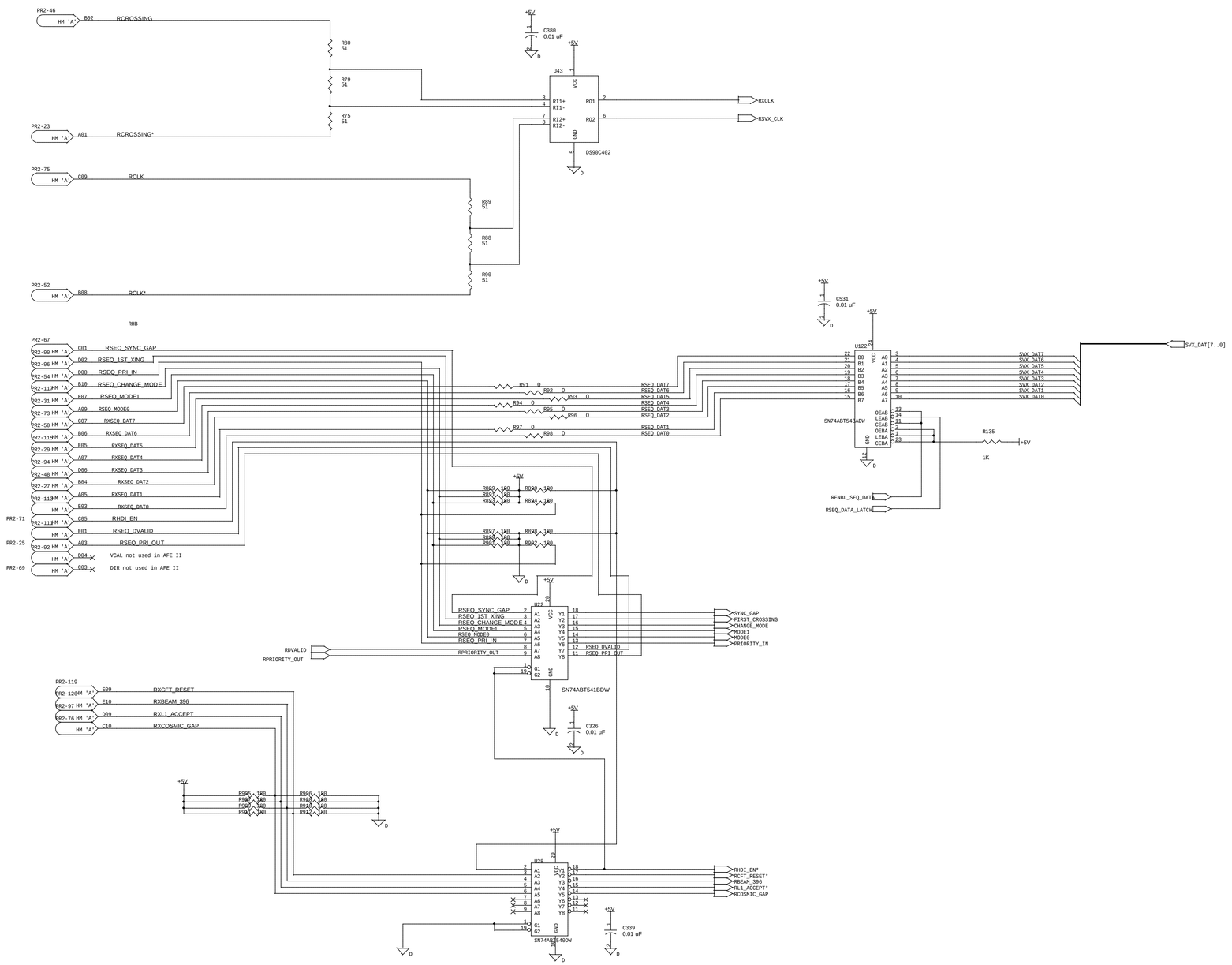
Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 40 of 42

Back to Page 1



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SVX Sequencer Connector - Right-Handed Insertion

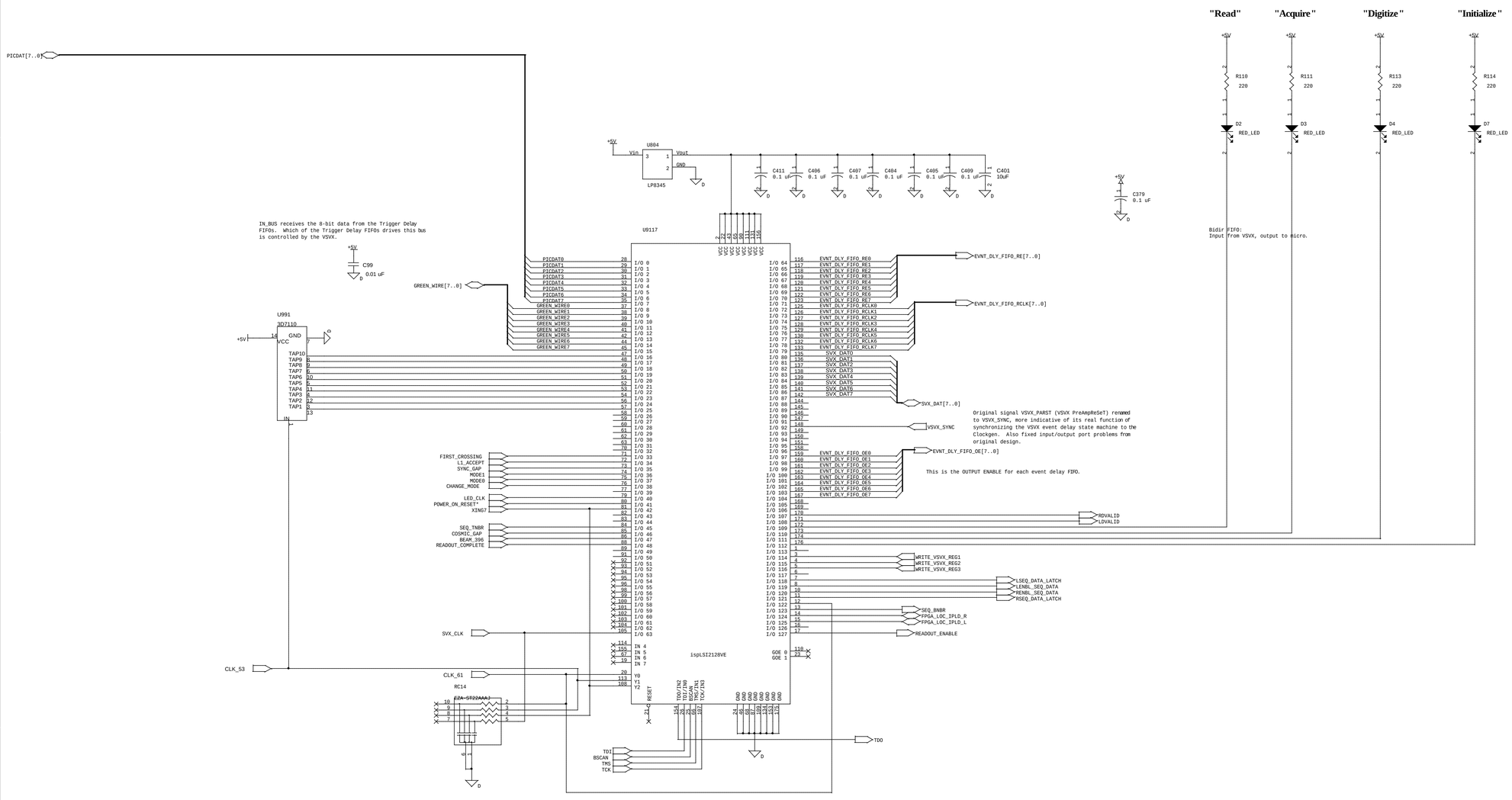
Size	CAGE Code	DWG NO	Rev
D		3823-113-ED-330238	C

Monday, April 26, 2004

Scale

Sheet 41 of 42

Back to Page 1



Drawn: Jamieson T. Olsen Checked: Approved:	D-Zero Experiment - Central Fiber Tracker - CFT Axial Analog Front End Fermi National Accelerator Laboratory P.O. Box 500 M/S 352 Batavia, IL 60510			
	Virtual SVX			
	Size D	CAGE Code	DWG NO 3823-113-ED-330238	Rev C
Monday, April 26, 2004	Scale		Sheet 42 of 42	